Volume 2
$2.95

Harris Linear & Data Acquisition Products

Harris Semiconductor Analog Products represent the state of the art in precision and high speed performance. Capitalizing on the advanced linear processing technologies developed over the past 15 years, Harris Semiconductor Analog Products offer high quality and unmatched performance.

This data book describes Harris Semiconductor's complete line of Linear and Data Acquisition products, and includes a complete set of product specifications and data sheets, application notes and a separate section describing our quality and high reliability program.

All specifications in this data book are applicable only to packaged products. Specifications for dice are obtainable in Harris Semiconductor's Chip Data Book.

Please fill out the registration card at the back of this data book and return it to us so we may keep you informed of our latest new product developments over the next year.

If you need more information on these and other Harris products, please contact the nearest Harris sales office listed in the back of this data book.

Harris Semiconductor's products are sold by description only. Harris reserves the right to make changes in circuit design, specifications and other information at any time without prior notice. Accordingly, the reader is cautioned to verify that data sheets and other information in this publication are current before placing orders. Information contained in application notes is intended solely for general guidance; use of the information for user's specific application is at user's risk. Reference to products of other manufacturers are solely for convenience of comparison and do not imply total equivalency of design, performance, or otherwise.

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Contents

Alpha-Numeric Product Index

Ordering Information

Harris Products are designated by "Product Code". When ordering please refer to products by the full code. Harris products will always begin with H. Specific device numbers will always be isolated by hyphens.

PRODUCT CODE EXAMPLE

H A 1 - 2425 - 5

PREFIX:
H (Harris)

FAMILY:
A – Analog
C – Communications
D – Digital
I – Interface
M – Memory

PACKAGE:
1– Dual-In-Line
2– TO-5 Type
3– Epoxy Package
4– Leadless Carriers
7– Mini DIP
9– Flat Pack
0– Chip Form

PART NUMBER

TEMPERATURE:
1 0°C to +200°C*
2 -55°C to +125°C
4 -25°C to +85°C
5 0°C to +75°C
6 100% 25°C Probe (Dice Only)
7 Dash-7 High Reliability Commercial Product. 0°C to +75°C.
8 Dash-8 Program MIL-STD-883 Class B HA2-2700-8 (Example Only)
9 -40°C to +85°C

* Special high temperature testing available on certain product types. Consult factory for availability.

HARRIS DASH 8 PROGRAM

As a service to users of High Rel products Harris makes readily available via the high reliability DASH 8 program many products from our product lines. Parts screened to MIL-STD-883 Method 5004 Class B are simply branded with the post-script "-8" to the appropriate Harris part numbers, in effect, offering "off the shelf" delivery. For details concerning this special Harris program for High Rel users, see the Dash 8 section of this Data Book.

HARRIS DASH 7 PROGRAM

The Harris DASH 7 High Reliability Commercial Products program extends HARRIS processing for Hi-Rel military components to standard commercial products to provide improved levels of quality and reliability. Details on DASH 7 are included in Section 8 of this Data Book.

SPECIAL ORDERS

For best availability and price, it is urged that standard "Product Code" devices be specified, which are available worldwide from authorized distributors. Where enhanced reliability is needed, note standard "Dash 8" screening described in this Data Book. Harris application engineers may be consulted for advice about suitability of a part for a given application.

If additional electrical parameter guarantees or reliability screening are absolutely required, a Request for Quotation and Source Control Drawing should be submitted through the local Harris Sales Office or Sales Representative. Since, many electrical parameters may be economically assured through design analysis, characterization, or correlation with other parameters, additionally desired parameters should be labeled, "Vendor will guarantee, but not necessarily test".

Harris reserves the right to decline to quote, or to request modification to special screening requirements.

I. C. Handling Procedures

Harris Analog I.C. processes produce circuits more rugged than similar ones. However, no semiconductor is immune from damage resulting from the sudden application of many thousands of volts of static electricity. While the phenomenon of catastrophic failure of devices containing MOS transistors or capacitors is well known, even bipolar circuits can be damaged by static discharge, with altered electrical properties and diminished reliability. None of the common I.C. internal protection networks operate quickly enough to positively prevent damage.

It is suggested that all semiconductors be handled, tested, and installed using standard "MOS handling techniques" of proper grounding of personnel and equipment. Parts and subassemblies should not be in contact with untreated plastic bags or wrapping material. High impedance I.C. inputs wired to a P.C. connector should have a path to ground on the card.

HANDLING RULES

Since the introduction of integrated circuits with MOS structures and high quality junctions, a safe and effective means of handling these devices has been of primary importance. One method employed to protect gate oxide structures is to incorporate input protection diodes directly on the monolithic chip. However, there is no completely foolproof system of chip input protection in existance in the industry. In addition most compensation networks in linear circuits are located at high impedance nodes, where protection networks would disturb normal circuit operation. If static discharge occurs at sufficient magnitude (2KV or more), some damage or degradation will usually occur. It has been found that handling equipment and personnel can generate static potentials in excess of 10KV in a low humidity environment; thus it becomes necessary for additional measures to be implemented to eliminate or reduce static charge. It is evident, therefore, that proper handling procedures or rules should be adopted.

Elimination or reduction of static charge can be accomplished as follows:

- Use conductive work stations. Metallic or conductive plastic* tops on work benches connected to ground help eliminate static build-up.
- Ground all handling equipment.
- Ground all handling personnel with a conductive bracelet through 1-M ohm to ground. The 1-M ohm resistor will prevent electroshock injury to personnel.
- Smocks, clothing, and especially shoes of certain insulating materials (notably nylon) should not be worn in areas where devices are handled. These materials, highly dielectric in nature, will hold, or aid, in the generation of a static change. Where they cannot be eliminated natural materials such as cotton etc. should be used to minimize charge generation capacity.
- Control relative humidity to as high as a level as practical. (RH 50%).
- Ionized air blowers reduce charge build-up in areas where grounding is not possible or desirable.
- Devices should be in conductive carriers during all phases of transport. Leads may be shorted by tubular metallic carriers, conductive foam or foil.
- In automated handling equipment, the belts, chutes, or other surfaces should be of conducting material. If this is not possible, ionized air blowers may be a good alternative.

* Supplier 3M Company "Velostat"

Harris Analog I. C. Technologies

JUNCTION ISOLATION (J.I.)

This is the most common integrated circuit process. Bipolar I.C.'s generally begin with a p-type wafer into which a buried layer pattern, if used, is first diffused. Then the n-type epitaxial layer is grown, and p-type isolation walls are diffused around each area which is to be electrically isolated from the other circuitry. These isolation walls must be diffused deeply into the wafer in order to contact the original p-substrate. In operation, the p-substrate and isolation walls are connected to the most negative circuit potential, so that each active area is surrounded on the sides and bottom by a reverse biased junction through which negligible current flows (Figure 1).

To complete the I.C., base and emitter diffusions are performed, the wafer is coated with aluminum and the conductor pattern is etched.

Representative Harris devices using this process are HA-2820, HA-4741 and HD-0165.

DIELECTRIC ISOLATION (D.I.)

A somewhat different process has been proven particularly advantageous for fabricating high performance analog I.C.'s. This is dielectric isolation (D.I.), where each active area is surrounded on the sides and bottom by an insulating layer of silicon dioxide, and for mechanical strength imbedded in polycrystalline silicon. This process for bipolar I.C.'s begins with a wafer of n-type silicon. The side of the wafer which will eventually be the bottom is deeply etched to form the sidewall pattern, then silicon dioxide and polycrystalline silicon are grown to fill the etched "moats". The opposite side of the wafer is then polished until the insulating sidewalls appear at the wafer surface (Figure 2). Conventional diffusion and metallization processes follow to complete the I.C. D.I. for analog I.C.'s has a number of advantages:

1. Almost all op amp designs require at least one PNP transistor in the signal path. Typical J.I. op amps must use a lateral PNP which inherently has very low frequency response, limiting typical compensated bandwidth to 1MHz. The D.I. process makes it practical to build a vertical PNP with much higher bandwidth making possible compensated op amp bandwidths of 12MHz or higher (Figure 3). Also, transistor collector to substrate capacitance is 2/3 less using D.I., further enhancing high frequency performance.
2. Other devices such as optimally specified MOS or JFET transistors may be fabricated on the same chip. Isolated diffused and thin film resistors are also practical.
3. The isolation removes the possibility of parasitic SCR's which might create latchup under certain sequences of power and signal application.
4. Leakage currents to the substrate under high temperature conditions are greatly reduced. While the circuits in this data book were not specifically designed for operating temperatures greater than +125°C, many have shown superior performance. For I.C.'s requiring the ultimate in radiation resistance, Harris Semiconductor Programs Division should be consulted.

DIELECTRIC ISOLATED CMOS

J.I. processed CMOS Analog I.C.'s, which are generally used in conjunction with several power supplies, are particularly prone to parasitic SCR latchup failures and failures due to input voltage spikes. The D.I. CMOS process, which is compared in detail in Harris Application Note 521, has proved to be the best solution.

Since analog multiplexers are often used at the input of a data acquisition system, particular attention must be paid to the possibility of damaging input overvoltage conditions. Harris has provided an effective answer in the HI-506A through HI-509A multiplexers with built-in overvoltage protection.

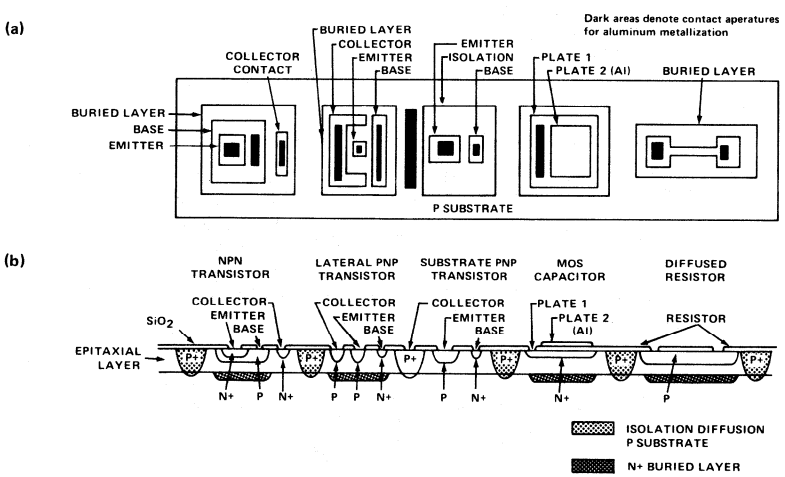


Figure 1 — Structures of various components formed in the junction-isolation process. (a) Topological view. (b) Cross-sectional view.

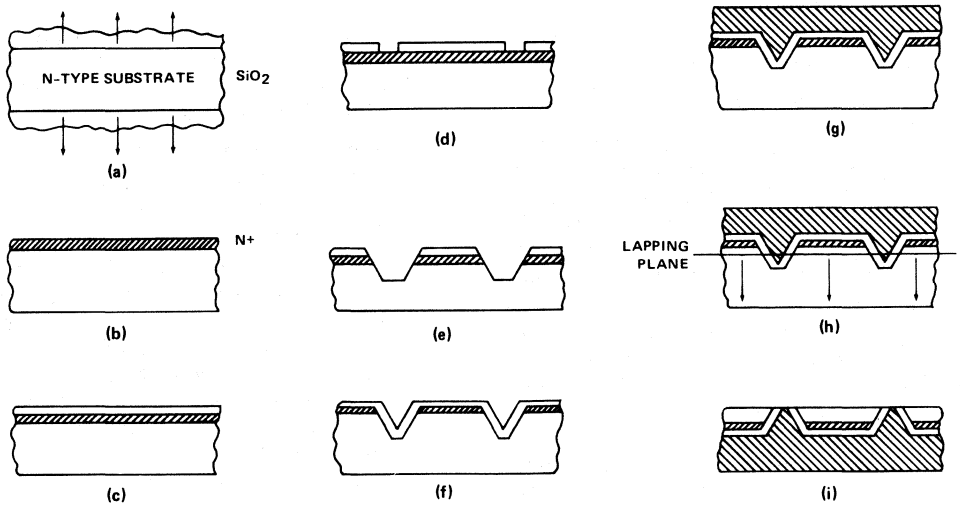


Figure 2 — Process steps for dielectric isolation. (a) Surface preparation, (b) N- buried layer diffusion, (c) masking oxide, (d) isolation pattern, (e) silicon etch, (f) dielectric oxide, (g) polycrystalline deposition, (h) backlap and polish, (i) finished slice.

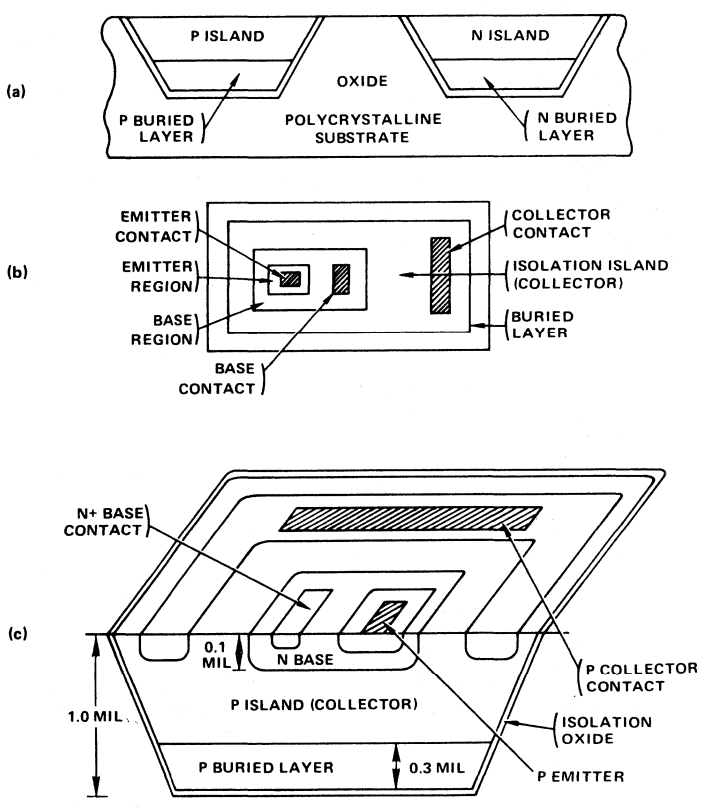


Figure 3 — The high-frequency process. (a) Cross-sectional view of P and N islands for PNP and NPN transistors. (b) Topological view showing relative placement of transistor regions. (c) Cross-sectional view of high-frequency PNP device formation in the D.I. process.

MANU-FACTURER	PART NUMBER	HARRIS PIN-FOR-PIN REPLACEMENT	HARRIS CLOSEST REPLACEMENT	SUGGESTED FOR NEW DESIGN
AMD	AM118/318			HA-2510/15
	AM715			HA-2520/25
	AM1660			HA-2500/05
				HA-2600/05
				HA-2700/05
ANALOG DEVICES	AD505		HA-2530/35	
	AD507JH*	HA2-2625-5		
	AD507SH	HA2-2620-2		
	AD509JH*	HA2-2525-5		
	AD509SH	HA2-2520-2		
	AD518		HA-2510/15	
	AD562		HI-562	
	AD582		HA-2420/25	
	AD583KS	HA1-2425-5		
	AD7501			HI-1818A
	AD7502			HI-1828A
	AD7503			HI-1818A
	AD7506TD*	HI1-506-2		
	AD7507TD*	HI1-507-2		
	AD7510			HI-201
	AD7511			HI-201
	AD7512			HI-5043
	AD7513TH*	HI2-200-2		
	AD2700U			HA-1600-2
	AD2700L			HA-1600-5
BURR BROWN	3500/3510A			HA-2605
	3500/3501R			HA-2600
	3503J	HA2-2505-5		
	3506J	HA2-2605-5		
	3507J	HA2-2525-2		
	3508J	HA2-2625-5		
	3553AM			HA-2630/35
	MPC4D	HI1-509A-5		
	MPC8S	HI1-508A-5		
	MPC8D	HI1-507A-5		
	MPC16S	HI1-506A-5		
DATEL	AM-450-2	HA2-2505-5		
	AM-452-2	HA2-2525-5		
	AM-460-2	HA2-2605-5		
	AM-462-1	HA1-2625-5		
	AM-462-2	HA2-2625-5		
	AM-464-2	HA2-2645-5		
	AM-490-2A	HA2-2905-5		
	MX-808	HI-508A-5		
	MX-1606	HI-506A-5		
	MXD-409	HI-509A-5		
	MXD-807	HI-507A-5		
	SHM-1C-1	HA1-2425-5		
	DAC-681	HI-562		

* "K" equivalent is either military or selected commercial

MANU-FACTURER	PART NUMBER	HARRIS PIN-FOR-PIN REPLACEMENT	HARRIS CLOSEST REPLACEMENT	SUGGESTED FOR NEW DESIGN
EXAR	XR4212		HA-4741	
FAIRCHILD	μA702			HA-2620/25
	μA709			HA-909/911
	μA715			HA-2520/25
	μA725		HA-2700/05	
	μA727			HA-2900/05
	μA740			HA-5100/5110
	μA741			HA-909/911
				HA-2600/05
				HA-2700/05
	μA747		HA-2640/45	HA-2650/55
	μA748			HA-2620/25
	μA772		HA-2510/15	
	μA776		HA-2720/25	
	μA791			HA-2630/35
	SH3002			HI-1800A
	1558/1458		HA-2650/55	
INTERSIL	IH201	HI-201		
	IH200	HI-201		
	4250		HA-2720	
	4250C		HA-2725	
	IH5040MDE	HI1-5040-2		
	IH5040CDE	HI1-5040-5		
	IH5041MDE	HI1-5041-2		
	IH5041CDE	HI1-5041-5		
	IH5042MDE	HI1-5042-2		
	IH5042CDE	HI1-5042-5		
	IH5043MDE	HI1-5043-2		
	IH5043CDE	HI1-5043-5		
	IH5044MDE	HI1-5044-2		
	IH5044CDE	HI1-5044-5		
	IH5045MDE	HI1-5045-2		
	IH5045CDE	HI1-5045-5		
	IH5046MDE	HI1-5046-2		
	IH5046CDE	HI1-5046-5		
	IH5047MDE	HI1-5047-2		
	IH5047CDE	HI1-5047-5		
	IH5048MDE	HI1-5049-2/HI1-5051-2		
	IH5048CDE	HI1-5049-5/HI1-5051-5		
	IH5049MDE	HI1-5049-2		
	IH5049CDE	HI1-5049-5		
	IH5050MDE	HI1-5050-2		
	IH5050CDE	HI1-5050-5		
	IH5051MDE	HI1-5051-2		
	IH5051CDE	HI1-5051-5		
	8017			HA-2520/25
	8021M		HA-2720	
	8021C		HA-2725	
	8022M			HA-2730
	8022C			HA-2735
	IH5110/5111			HA-2420/25

MANU-FACTURER	PART NUMBER	HARRIS PIN-FOR-PIN REPLACEMENT	HARRIS CLOSEST REPLACEMENT	SUGGESTED FOR NEW DESIGN
	IH5060		HI-506A	
	IH5070		HI-507A	
	HA-2500/02/05	HA-2500/02/05		
	HA-2510/12/15	HA-2510/12/15		
	HA-2520/22/25	HA-2520/22/25		
	HA-2600/02/05	HA-2600/02/05		
	HA-2620/22/25	HA-2620/22/25		
INTRONICS	A-560	HA2-2525-5		
	A-561	HA2-2625-5		
	A-570	HA2-2535-5		
	CA-580	HA2-2905-5		
MOTOROLA	MC1520/1420			HA-2600/05
	MC1530/1531/ 1430/31			HA-2600/05
	MC1533/1433			HA-2700/05
	MC1536/1436		HA-2640/45	
	MC1538/1438			HA-2620/2635
	MC1539/1439			HA-2620/25
	MC1545/1445			HA-2400/2505
	MC1554/1454			HA-2620/2635
	MC1556/1456			HA-2600/05
	MC1558/1458		HA-2650/55	
	MC3301/3401			HA-4741
	MC3302			HA-4900
	MC3403/3505		HA-4741	
	MX4741		HA-4741	
NATIONAL	LF11508/13508		HI-508A	
	LF11509/13509		HI-509A	
	LF11201/12201/13201		HI-201	
	LF155A/156A/157A		HA-5100-2	
	LF355A/356A/357A		HA-5105-5	
	LF198/398			HA-2420/25
	LH0001			HA-2700
	LH0002			HA-2630
	LH0003			HA-2520
	LH0004			HA-2640
	LH0005			HA-2620
	LH0022/42/52			HA-5100/5105
	LH0023/43			HA-2420/25
	LH0024			HA-2530/35
	LH0032			HA-5190/95
	LH0033/63			HA-2630/35
	LH0062		HA-5190/95	
	LH0070-2			HA-1600-5
	LM101/301/ 107/307			HA-909/911/ 2600/05/ 2700/05
	LM102/302			HA-2600/05
	LM108/208/308			HA-2700/04/05
	LM110/310			HA-2500/05

MANU-FACTURER	PART NUMBER	HARRIS PIN-FOR-PIN REPLACEMENT	HARRIS CLOSEST REPLACEMENT	SUGGESTED FOR NEW DESIGN
NATIONAL (Continued)	LM112/212/312			HA-2700/04/05
	LM118/318			HA-2510/15
	LM124/324		HA-4741	
	LM139/339			HA-4900/05
	LM143/343			
	LM144/344		HA-2640/45	
	LM148/348		HA-2640/45	
	LM149/349		HA-4741	
	LM199		HA-4602/05	HA-1600-2
				HA-1610-2
	LM199A			HA-1600-2
				HA-1610-2
	LM399A			HA-1610-5
PRECISION MONO.	MUX-08	HI-508A		
	MUX-09	HI-509A		
	OP-01			HA-2600/05
				2500/05
	SMP81	HA-2420/25		
	MUX-88	HI-508A		
	OP-15A		HA-5100-2	
	OP-15E		HA-5100-5	
	OP-15F		HA-5105-5	
	OP-17A		HA-5110-2	
	OP-17E		HA-5110-5	
	OP-17F		HA-5115-5	
	REF-01A		HA-1610-2	
	REF-01E		HA-1610-5	
	OP-05/07			HA-2900/05
	SSS1558/1458		HA-2650/55	
	DAC-12			HI-562
	SSS562	HI1-562-5		
RCA	CA3020			HA-2630/35
	CA3078			HA-2720/2730
	CA3100			HA-2520/25
	CA6078			HA-2720/2730
	CD4016			HI-201
RAYTHEON	RM/RC1556A			HA-2600/05
	RM/RC4131			HA-2600/05
	RM/RC4132			HA-2700/05
	RM/RC4136			HA-4741
	RM4156	HA1-4741-2		
	RC4156	HA1-4741-5		
	HA1-4741-2	HA1-4741-2		
	HA1-4741-5	HA1-4741-5		
	RM/RC4531			HA-2500/05
	RM/RC4558		HA-2650/55	
SIGNETICS	5537			HA-2420/25
	531			HA-2510/15
	5556			HA-2600/05
	5558		HA-2650/55	

MANU-FACTURER	PART NUMBER	HARRIS PIN-FOR-PIN REPLACEMENT	HARRIS CLOSEST REPLACEMENT	SUGGESTED FOR NEW DESIGN
SILICON GENERAL	SG741S SG741SG			HA-2500 HA-2505
SILICONIX	DG181* DG184 DG185 DG187 DG188 DG190 DG191 DG200AA DG200BA DG200AK DG200BK DG200CJ DG201AK DG201BK DG201CJ DG506AR DG506BR DG506CJ DG507AR DG507BR DG507CJ DG508 DG509 L140	 HI2-200-2 HI2-200-5 HI1-200-2 HI1-200-5 HI3-200-5 HI1-201-2 HI1-201-5 HI3-201-5 HI1-506-2 HI1-506-5 HI1-506-5 HI1-507-2 HI1-507-5 HI3-507-5	 HI-5049 HI-5045 HI-5051 HI-5043 HI-508A HI-509A	HI-5048 HI-5050 HI-5042 HA-2720/25
SOLITRON	CM4016A µc4000/4001C/ 4002C µc4250 µc4250c		 HA-2720 HA-2725	HI-201 HA-2605
SPRAQUE	µLS/ LN2139 µLS/ LN2151 µLS/ LN2156 µLS/ LN2157 µLS/ LN2158 µLS/ LN2171 µLS/ LN2172 µLS/ LN2173 µLS/ LN2174 µLS/ LN2175 µLS/ LN2176			HA-2600/05 HA-2600/05 HA-2600/05 HA-2650/55 HA-2650/55 HA-2600/05 HA-2620/25 HA-2600/05 HA-2620/25 HA-2600/05 HA-2600/05
TELEDYNE PHILBRICK	1321 1321-01 1322 1322-01 1323 1323-01 1323-02	HA2-2625-5 HA2-2620-2 HA2-2525-5 HA2-2520-2 HA2-2705-5 HA2-2700-2 HA2-2704-4		

MANU-FACTURER	PART NUMBER	HARRIS PIN-FOR-PIN REPLACEMENT	HARRIS CLOSEST REPLACEMENT	SUGGESTED FOR NEW DESIGN
TELEDYNE PHILBRICK (Continued)	1332	HA2-2645-5		
	1339			HA-2625
	1340	HA2-2905-5		
	4551	HI1-507A-5		
	4552	HI1-506A-5		
	4856	HA1-2425-5		
	1430			HA-5195
TI	TL022M/C			HA-2730/35
	TL044			HA-4741
	TL084		HA-4602	
	TL0891/089C		HA-2904/05	
	MC1558/1458		HA-2650/55	
TRANSITRON	TOA7709			HA-2600
	TOA8709			HA-2605

Advance Product Information

Advance Data Sheets

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

ADVANCE

HA-1620

Precision +5 Volt Reference

FEATURES

- MONOLITHIC CONSTRUCTION
- EXCELLENT TEMPERATURE STABILITY 0.3ppm/°C
- LOW NOISE 100 μVrms
- WIDE INPUT RANGE 11.4 - 35
- ADJUSTABLE OUTPUT ±0.5V

APPLICATIONS

- EXTERNAL VOLTAGE REFERENCE FOR DATA CONVERTERS
- COMPARATOR REFERENCE
- REGULATOR REFERENCE

DESCRIPTION

The Harris HA-1620 is a monolithic, temperature regulated +5V Precision Voltage Reference.

An on-chip heating element heats the chip to a predetermined point. Once this temperature is reached it is sensed and regulated.

Extremely low output temperature coefficients can be achieved by this method. Less than 1ppm/°C is typical for the HA-1620.

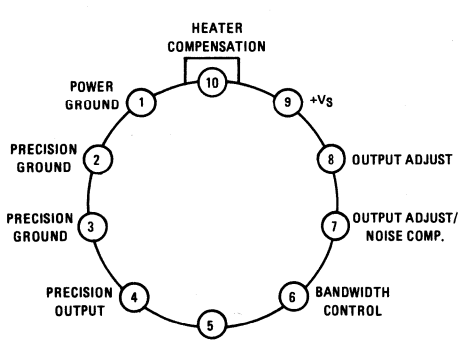
The HA-1620 will accept an input voltage of between 11.4 and 35 volts and provide a very stable +5V output, capable of delivering 10mA output current.

Nominally +5Volts, (±5mV) the output can be adjusted ±0.5V by external resistors.

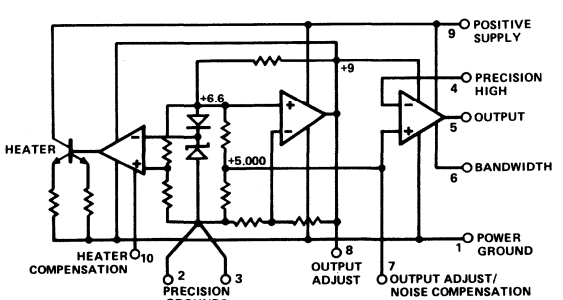
This reference is ideal for applications requiring precision and stability such as instrumentation and high resolution D/A converters.

PINOUT

TOP VIEW



FUNCTIONAL DIAGRAM



HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

ADVANCE

HA-5130

Precision Operational Amplifier

1

FEATURES

- ULTRA LOW OFFSET VOLTAGE $< 100\mu V$
- ULTRA LOW OFFSET VOLTAGE DRIFT $1\mu V/^{o}C$
- EXCELLENT STABILITY
- LOW NOISE $10nV/\sqrt{Hz}$

APPLICATIONS

- REPLACEMENT FOR CHOPPER AMPLIFIERS
- LOW LEVEL SIGNAL APPLICATION
- PRECISION SUMMING AMPLIFIERS

DESCRIPTION

The HA-5130 Precision Operational Amplifier offers an economical alternative to modular and monolithic chopper stabilized amplifiers.

It presents an excellent combination of low offset voltage, low offset voltage drift and low noise.

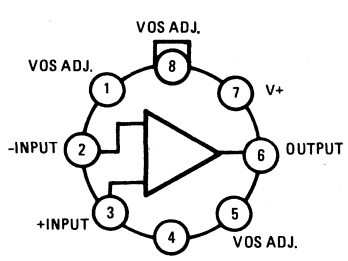
These characteristics coupled with its dynamic performance make this amplifier suitable for a wide range of applications in low level signal processing.

The HA-5130 is internally compensated for unity gain configurations and in addition should reduced offset voltage be required the trimpot can be connected to pins 1 and 5 or 1 and 8 for added versatility.

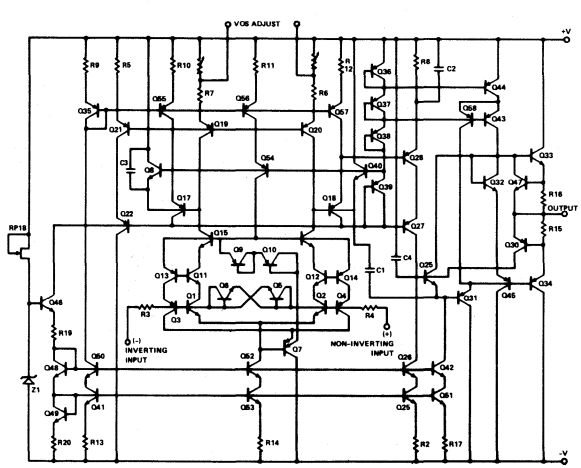
PINOUT

Package Code TO-99

TOP VIEW



FUNCTIONAL DIAGRAM



HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

ADVANCE

HA-5160

Wideband, High Slew Rate JFET Operational Amplifier

FEATURES

- HIGH SLEW RATE — 140V/μsec.
- UNITY GAIN BANDWIDTH — 120MHz
- LARGE VOLTAGE GAIN
- LOW OFFSET VOLTAGE — 2mV
- FAST SETTING TIME — <500nsecs.

APPLICATIONS

- HIGH SPEED DATA ACQUISITION SYSTEMS
- PULSE AMPLIFICATION
- VIDEO FREQUENCY APPLICATIONS

DESCRIPTION

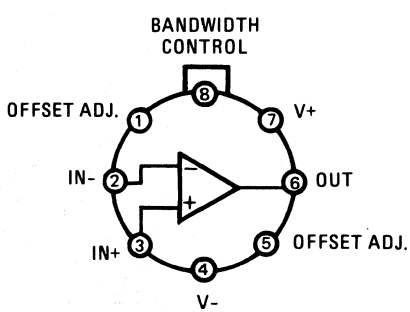
The HA-5160 is a monolithic wideband, high slew rate operational amplifier manufactured using JFET input and dielectric isolation.

Precision laser trimming of the input stage complements the amplifiers' dynamic capabilities with excellent input characteristics.

Outstanding features of this device are very high slew rate and wide bandwidth which make it suitable for a wide range of signal conditioning applications.

PINOUT

TOP VIEW



TO -99

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
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ADVANCE

HA-5310/5315

Precision Sample and Hold Amplifier

1

FEATURES

- ACCURACY (FULL TEMP) 0.01%
- ACQUISITION TIME (.005%) 6μs
- APERTURE TIME 2ns
- FEEDTHROUGH ERROR Less than 0.005%
- FULLY DIFFERENTIAL INPUT
- INTERNAL HOLD CAPACITORS
- TTL/CMOS COMPATIBLE

APPLICATIONS

- PRECISION DATA ACQUISITION SYSTEMS
- A/D CONVERTER FRONT END

DESCRIPTION

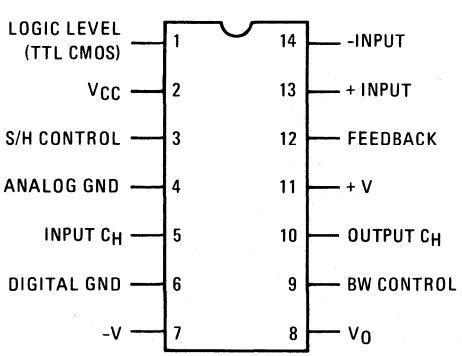
The HA-5310 is a high precision sample and hold, which is capable of tracking the signal appearing at its inputs while presenting the result of the previous hold operation at its output, making the circuit ideally suited to use in time multiplexed systems. The circuit contains a high impedance, fully differential input of the type traditionally employed in instrumentation amplifiers, which affords high common mode rejection , high noise insensitivity, and compatibility with optimized grounding schemes. External feedback networks allow the acquired signal to be amplified by a user-determined factor.

The acquisition process employs a technique which provides auto zeroed input operation. The sample/hold capacitor switching is accomplished with a novel bipolar switching technique which results in extremely low charge transfer errors. These provide the ability to hold total error to less than .01% over the military temp range.

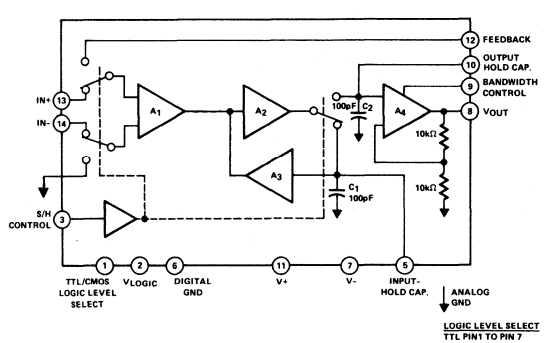
The device is composed of two monolithic bipolar chips, each featuring dielectric isolation. Package is a plastic or ceramic 14 pin DIP.

PINOUT

TOP VIEW



FUNCTIONAL DIAGRAM



HARRIS SEMICONDUCTOR PRODUCTS DIVISION
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ADVANCE

HI-300/301/ 302/303

CMOS Analog Switches

FEATURES

- WIDE ANALOG SIGNAL RANGE ±15V
- FAST SWITCHING SPEED (TYP) 100ns
- LOW ON RESISTANCE (MAX) 50Ω
- LOW STANDBY POWER (TYP) 0.06μW
- BREAK-BEFORE-MAKE SWITCHING
- TTL COMPATIBLE
- NO LATCH UP
- DIGITAL INPUT OVERVOLTAGE PROTECTION

APPLICATIONS

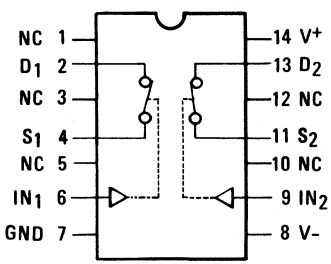
- HIGH FREQUENCY SWITCHING
- SAMPLE AND HOLD
- BATTERY OPERATED SYSTEMS
- DIGITAL FILTERS
- OP AMP GAIN SWITCHING

DESCRIPTION

The HI-300 through HI-303 family of monolithic CMOS analog switches offers low power operation combined with fast switching speeds and low ON resistance. These switches typically consume only 0.06 μW in a standby mode and only 7.5mW while operating. Switching speeds are typically 100 ns and the low ON resistance of 50Ωmaximum has little variation over temperature. Their specifications make these switches ideal for use where high performance switching is required over a wide analog signal range. These switches are fabricated with dielectric isolation processing, thereby eliminating latch-ups and reducing leakage currents. Break-before-make switching is insured and these devices are TTL compatible. The HI-300 through HI-303 are direct replacements for the DG 300 through DG 303. Duplications for these switches include signal path switching, sample and hold circuits, op amp gain switching, and battery powered circuits.

PINOUTS

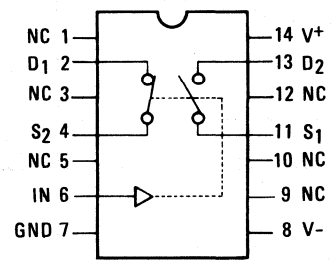
HI-300 DUAL SPST



LOGIC	SW1 SW2
0	OFF
1	ON

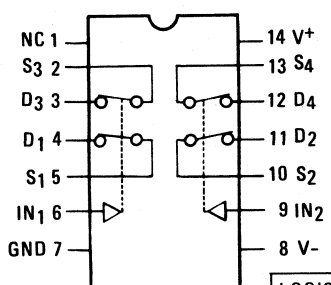
HI-301 SPDT

TOP VIEW



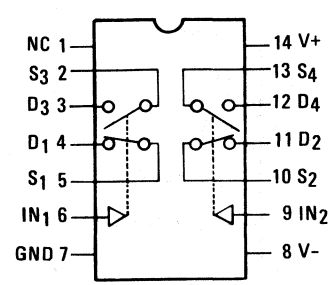
LOGIC	SW1	SW2
0	OFF	ON
1	ON	OFF

HI-302 DUAL DPST



LOGIC	SW1 SW2	SW3 SW4
0	OFF	OFF
1	ON	ON

HI-303 DUAL SPDT



LOGIC	SW1 SW2	SW3 SW4
0	OFF	ON
1	ON	OFF

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
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ADVANCE

HI-304/305/306/307

CMOS Analog Switches

1

FEATURES

- LOW OPERATING POWER (TYP) 0.06μW
- WIDE ANALOG SIGNAL RANGE ±15V
- LOW ON RESISTANCE (MAX) 50Ω
- FAST SWITCHING SPEED (TYP) 100ns
- BREAK-BEFORE-MAKE SWITCHING
- NO LATCH UP
- CMOS COMPATIBLE
- DIGITAL INPUT OVERVOLTAGE PROTECTION

APPLICATIONS

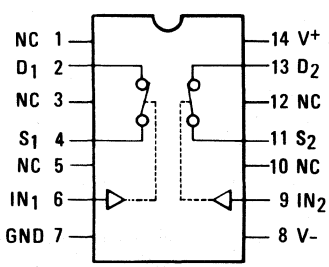
- BATTERY OPERATED SYSTEMS
- COMMUNICATION SYSTEMS
- HIGH FREQUENCY SWITCHING
- SAMPLE AND HOLD
- LOW LEVEL SWITCHING

DESCRIPTION

The HI-304 through HI-307 family of monolithic CMOS analog switches offers low power operation combined with fast switching speeds and low ON resistance. These switches typically consume only 0.06mW in both standby and operating modes. Switching speeds are typically 100 ns and the low ON resistance of 50Ω maximum varies little over temperature. These specifications make these switches ideal for use where high performance switching is required over a wide analog signal range. These switches are fabricated with dielectric isolated processing, thereby eliminating latch-ups and reducing leakage currents. Break-before-make switching is insured and these devices are CMOS compatible. The HI-304 through HI-307 are direct replacements for the DG 304 through DG 307 switches. Applications for these circuits include battery powered circuits, signal path switching, communication systems, and low level switching.

PINOUTS

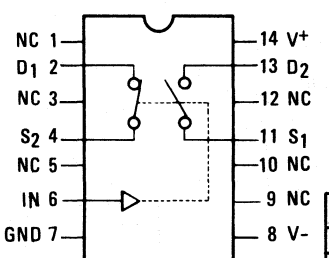
HI-304 DUAL SPST



LOGIC	SW1 SW2
0	OFF
1	ON

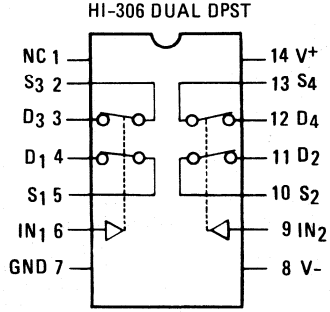
HI-305 SPDT

TOP VIEW



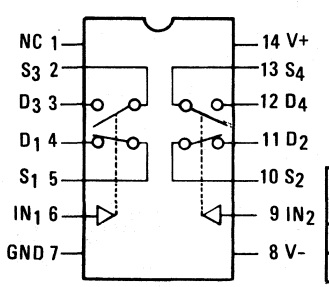
LOGIC	SW1	SW2
0	OFF	ON
1	ON	OFF

HI-306 DUAL DPST



LOGIC	SW1 SW2	SW3 SW4
0	OFF	OFF
1	ON	ON

HI-307 DUAL SPDT



LOGIC	SW1 SW2	SW3 SW4
0	OFF	ON
1	ON	OFF

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
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ADVANCE

HI-381/384/387/390

CMOS Analog Switches

1

FEATURES

- WIDE ANALOG SIGNAL RANGE ±15V
- FAST SWITCHING SPEED (TYP) 100ns
- LOW ON RESISTANCE (MAX) 50Ω
- LOW STANDBY POWER (TYP) 0.06μW
- NO LATCH UP
- BREAK-BEFORE-MAKE SWITCHING
- TTL/CMOS COMPATIBLE
- DIGITAL INPUT OVERVOLTAGE PROTECTION

APPLICATIONS

- HIGH FREQUENCY SWITCHING
- SAMPLE AND HOLD
- COMMUNICATION SYSTEMS
- MEMORY BLOCK SWITCHING
- BATTERY POWER SYSTEMS

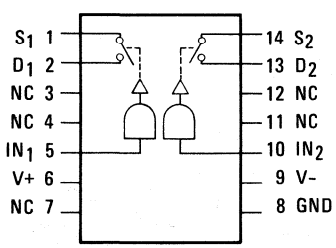
DESCRIPTION

The HI-381 through HI-390 family of monolithic CMOS analog switches offers low power operation combined with fast switching speeds and low ON resistance. These switches typically consume only 0.06 μW in a standby mode and only 7.5 mW while operating. Switching speeds are typically 100 ns and the low ON resistance of 50Ω maximum varies little over temperature. These specifications make these switches ideal for use where high performance switching is required over a wide analog signal range. The switches are fabricated with dielectric isolation processing, thereby eliminating latch-ups and reducing leakage currents. Break-before-make switching is insured and these devices are both TTL and CMOS compatible. The HI-381 through HI-390 are direct replacements for the DG 381 through DG 390, and are pin compatible with the DG 180 series switches. Applications for these switches include signal path switching, sample and hold circuits, op amp gain switching, and battery powered circuits.

PINOUTS

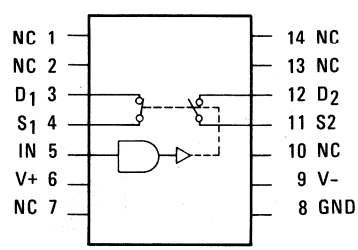
TOP VIEW

HI-381 DUAL SPST



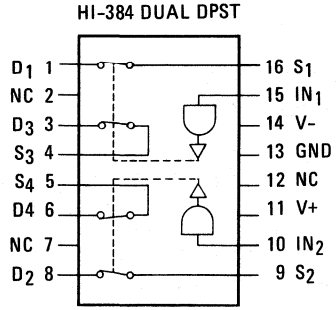
LOGIC	SW1 SW2
0	ON
1	OFF

HI-387 SPDT



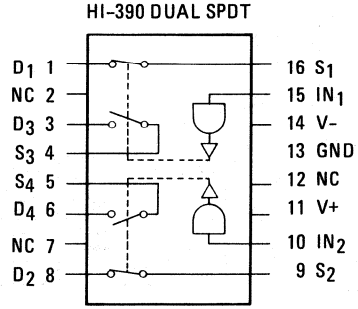
LOGIC	SW1	SW2
0	OFF	ON
1	ON	OFF

HI-384 DUAL DPST



LOGIC	SW 1-4
0	OFF
1	ON

HI-390 DUAL SPDT



LOGIC	SW1 SW2	SW3 SW4
0	OFF	ON
1	ON	OFF

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
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ADVANCE

HI-400/401

High Speed Analog Switches

1

FEATURES

- VERY FAST SWITCHING SPEED (MAX) 50ns
- LOW ON RESISTANCE (MAX) 50Ω
- WIDE ANALOG SIGNAL RANGE ±15V
- BREAK-BEFORE-MAKE SWITCHING
- NO LATCH UP
- TRUE TTL COMPATIBILITY
- PIN COMPATIBLE WITH HI-200/201

APPLICATIONS

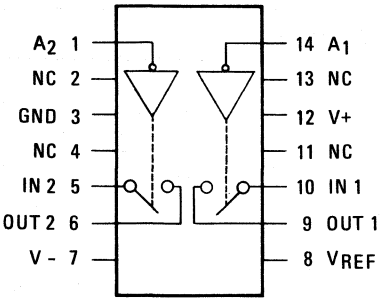
- HIGH FREQUENCY SWITCHING
- VIDEO DISPLAY SYSTEMS
- DIGITAL FILTERS
- SAMPLE AND HOLD
- ECM SYSTEMS

DESCRIPTION

The HI-400 and HI-401 are monolithic CMOS analog switches featuring very fast switching speed and low ON resistance. The HI-400 is a dual SPST switch, and the HI-401 is a quad SPST, with identical pinouts to the HI-200/201 switches. Switching speeds of 50ns max make these devices the fastest monolithic analog switches presently available. The HI-400 and HI-401 are ideal replacements for slower monolithic switches and for discrete devices. These switches also feature a low ON resistance of 50Ω and a wide analog signal range of ±15V, providing high performance switching at fast speeds. The HI-400 and HI-401 are fabricated with dielectric isolation processing, thereby eliminating latch-ups and reducing leakage currents.

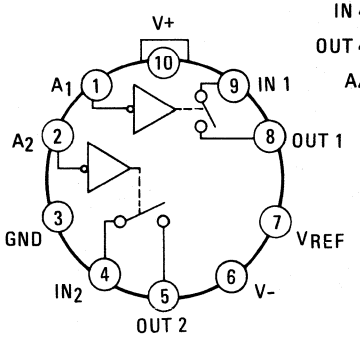
PINOUTS

TOP VIEW

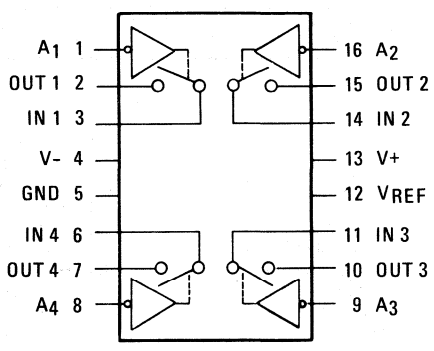


HI-400

TOP VIEW



TOP VIEW



HI-401

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
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ADVANCE

HI-5712

High Performance 12 Bit A/D Converter

FEATURES

- 8μs 12 BIT CONVERSION TIME
- 10ppm/°C GAIN TEMPCO
- TRI-STATE, SERIAL AND PARALLEL OUTPUTS
- INTERNAL CLOCK AND +10V REFERENCE
- MICROPROCESSOR COMPATIBLE
- TTL/CMOS COMPATIBLE
- NO MISSING CODES OVER TEMPERATURE.
- MIL-STD-883 PROCESSING AVAILABLE
- SHORT CYCLE CAPABILITY FOR 10,8, OR 6 BIT CONVERSIONS

APPLICATIONS

- MILITARY SYSTEMS
- HIGH PERFORMANCE DATA ACQUISITION

DESCRIPTION

The HI-5712 is a high speed 12 bit successive approximation A to D converter, featuring 8 μ s conversion time and 12 bit accuracy. Numerous functions can be software controlled or otherwise configured by the user to meet a variety of A to D converter requirements.

Also, Tri-State outputs and necessary signal lines are provided for interface with 8, 12, or 16 bit microprocessor systems.

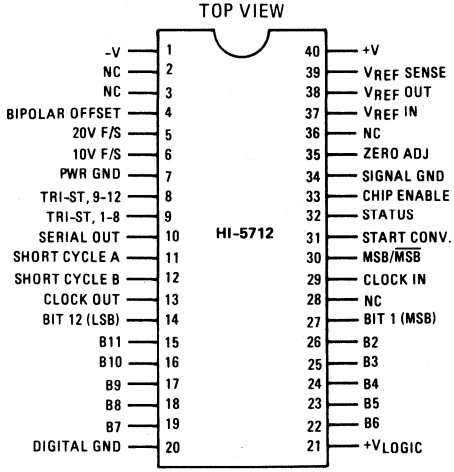
External pin connections prepare the analog input for unipolar or bipolar range, and 10V or 20V full scale. The internal 2MHz clock may be over-ridden by an external clock signal. The internal +10V reference offers 10mA output current and 5ppm/°C tempco. It may be left unconnected, jumpered to the internal DAC, or used as a reference elsewhere in the system. A remote sense terminal is provided for this purpose.

Programmable features include: Binary or 2's complement code select (MSB/$\overline{\text{MSB}}$); Short Cycle for 10, 8, or 6 bit conversion; independent control of the Tri-State function for bit groups 1-8 and 9-12.

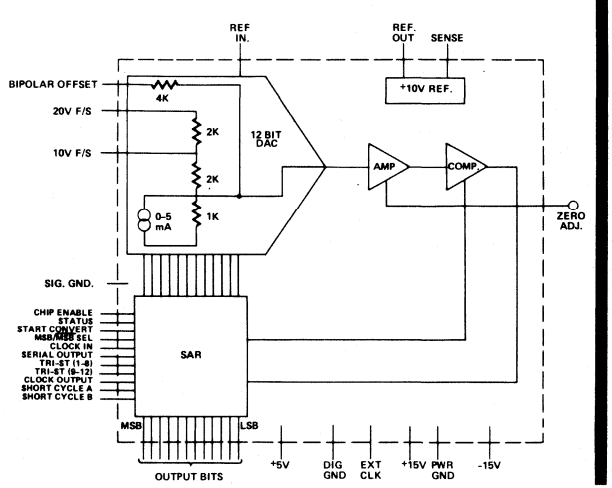
Monolithic chips comprising the converter are mounted in leadless chip carriers (LCC's) which are bonded to both sides of a multi-layer ceramic substrate resulting in a compact 40 pin dual-in-line package. Individual LCC's may be screened (to 883/Class B for example) before assembly on the HI-5712 substrate. The finished converter may then undergo further screening for very high levels of reliability.

PINOUT

TOP VIEW



FUNCTIONAL DIAGRAM



HARRIS SEMICONDUCTOR PRODUCTS DIVISION
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ADVANCE

HI-5812

12 Bit A to D Converter System

1

FEATURES

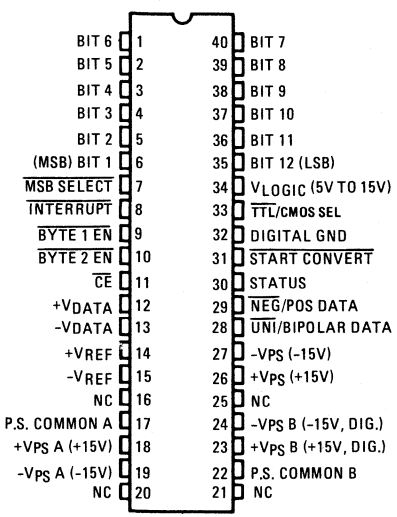
- 12 BIT ABSOLUTE ACCURACY OVER TEMP.
- 30μs CONVERSION TIME
- ADVANCED INTERFACE FOR μPROCESSORS
- SELF-CONTAINED TRACK/HOLD
- DIFFERENTIAL REFERENCE AND ANALOG DATA INPUTS
- UNIPOLAR POS/NEG OR BIPOLAR OPERATION
- THREE-STATE BYTE ORIENTED OUTPUTS
- STRAIGHT BINARY, OFFSET BINARY, OR 2's COMPLEMENT OUTPUT
- TTL/CMOS COMPATIBLE
- MIL-STD-883 SCREENING AVAILABLE

APPLICATIONS

- HIGH PERFORMANCE DATA ACQ. SYSTEMS
- MILITARY AND INDUSTRIAL SYSTEMS
- PRECISION INSTRUMENTATION

PINOUT

TOP VIEW



DESCRIPTION

The HI-5812 is a precision 12 bit A to D converter that is based on a conversion algorithm unique among integrated circuit converters. It offers an unprecedented 12 bit absolute accuracy over temperature, 30 microsecond conversion time, an advanced microprocessor interface, and an internal Track/Hold (T/H) amplifier.

Both the reference and analog voltage inputs offer the high impedance, fully differential configuration found in instrumentation amplifiers. These "floating" inputs allow the user to hookup the converter for optimum interference rejection in a variety of systems. Also, each input is auto-zeroed, which yields a maximum of ½ LSB error from all sources for both the Track/Hold and A/D conversion functions combined, over the operating temperature range. To realize this performance a precision 5V reference is required, such as Harris HA-1620.

Two identical analog processors are included in the HI-5812, each with its own Track/Hold amplifier. These processors alternately compute the relation $V_i = 2[V_{i-1} - V_r \text{ Sgn } (V_{i-1})]$, where V_{i-1} is the preceding result and V_r equals one half the (unipolar) input range. The sign of each computation determines one bit in the output code, beginning with the MSB.

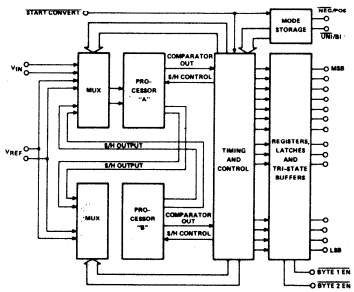
Because a Track/Hold function is inherent in the conversion process, the customary requirement of a T/H amplifier at the converter's input is eliminated. The START CONVERT command results in signal to HOLD and simultaneously initiates a conversion cycle. Before completion of the conversion the T/H has returned to TRACK and reacquired the analog input. This allows a new cycle to begin immediately, provided the user has selected the continuous conversion mode of operation.

INTERRUPT resets the converter at any point in the conversion cycle, and CHIP ENABLE disables all the digital control inputs to allow control of multiple converters by a single processor. Two more pins select positive or negative unipolar input, or bipolar input with the maximum code corresponding to top or bottom of the input range. The microprocessor interface circuitry includes a three state 12 bit parallel output, in which the 8 MSB's and the 4 LSB's are separately enabled to allow multiplexing over an 8 bit data bus.

Finally, the MSB SELECT input permits a choice of Offset Binary or 2's Complement for the bipolar output code. Any number of the above (8 digital inputs) may be changed from one conversion to the next when under software control via a microprocessor. A logic level select input is normally hardwired to accommodate either TTL or CMOS control signals.

The analog power requirements are ± 15V; digital is +5 to +15V. Package is a 40 pin ceramic DIP.

FUNCTIONAL DIAGRAM



HARRIS SEMICONDUCTOR PRODUCTS DIVISION
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ADVANCE

HC-55536

All-Digital Continuously Variable Slope Delta Demodulator (CVSD)

1

FEATURES

- REQUIRES FEWER EXTERNAL PARTS
- LOW POWER DRAIN: 6mW FROM SINGLE 5V-7V SUPPLY
- TIME CONSTANTS DETERMINED BY CLOCK FREQUENCY; NO CALIBRATION OR DRIFT PROBLEMS; AUTOMATIC OFFSET ADJUSTMENT
- FILTER RESET BY DIGITAL CONTROL
- AUTOMATIC OVERLOAD RECOVERY

DESCRIPTION

The HC-55536 is a CMOS integrated circuit used to convert serial NRZ digital data to an analog (voice) signal. Conversion is by delta demodulation, using the continuously variable slope (CVSD) method.

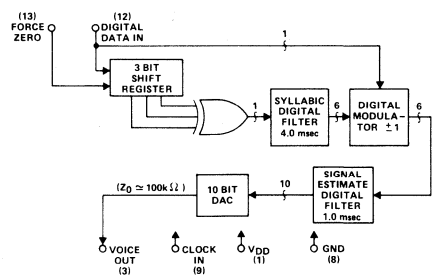
While signals are compatible with other CVSD circuits, the internal design is unique. The analog loop filters have been replaced by digital filters which use very low power and require no external timing components. This digital approach allows inclusion of many desirable features. which otherwise would be difficult to implement. Internal time constants are optimized for a 16K bit/sec data rate; the device is usable to 64K bits/sec.

The package is a 14 pin DIP, available in plastic (0°C to +70°C) or ceramic (-40°C to +85°C). Chips are available, probe tested at +25°C.

APPLICATIONS

- VOICE OUTPUT FOR DIGITAL SYSTEMS
- AUDIO MANIPULATIONS; DELAY LINES, ECHO GENERATION/SUPPRESSION, SPECIAL EFFECTS, ETC.

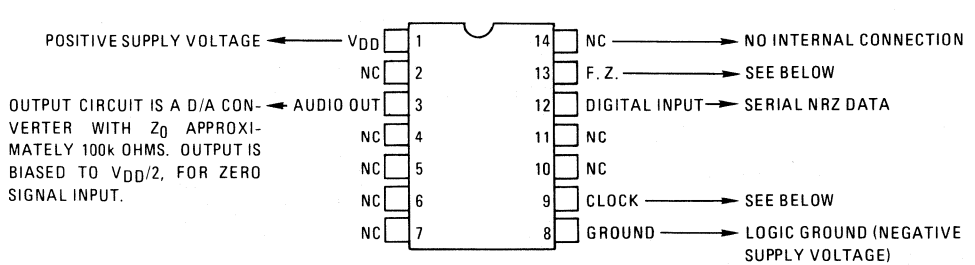
FUNCTIONAL DIAGRAM



PINOUT AND PIN DESCRIPTION

Package Codes: 3R, 4D, 4Y

TOP VIEW



F. Z. FORCED ZERO; NORMALLY HIGH. "LOW" FORCES THE AUDIO OUTPUT AND INTERNAL LOGIC INTO THE "QUIETING" PATTERN.

CLOCK CLOCK IS PHASED WITH DIGITAL INPUT DATA SO THAT LOW-TO-HIGH TRANSITIONS OCCUR NEAR THE MIDDLE OF EACH RECEIVED DATA BIT.

ABSOLUTE MAXIMUM RATINGS

Voltage at Any Pin	-3.0V to V_{DD} +0.3V	Operating Temperature (-5)	0°C to 70°C
Maximum V_{DD} Voltage	+7.0V	(-9)	-40°C to +85°C
Operating V_{DD} Range	+5.0V to +7.0V	Storage Temperature Range	-65°C to +150°C

ELECTRICAL CHARACTERISTICS V_{DD} = +6.0V; Bit Rate = 16K Bits/Sec; t_A = +25°C.

PARAMETER	MIN	TYP	MAX	UNIT
Clock Bit Rate (Note 1)	0		64	K Bits/Sec
Clock Duty Cycle	30		70	%
Supply Voltage	+5.0		+7.0	V
Supply Current		1.0		mA
Digital "1" Input (Note 2)		4.5		V
Digital "0" Input (Note 2)		1.5		V
Audio Output Voltage (Note 3)		0.5		V_{RMS}
Audio Output Impedance (Note 4)		100		kΩ
Syllabic Filter Time Constant (Note 5)		4.0		ms
L. P. Filter Time Constant (Note 5)		0.94		ms
Step Size Ratio (Note 6)		24		dB
Resolution (Note 7)		0.1		%
Minimum Step Size (Note 8)		0.2		%
Slope Overload (Note 9)		Fig. 1		–
Signal/Noise Ratio (Note 10)			Table I	–
Quieting Pattern Amplitude (Note 11)		12		mV_{p-p}
Clamping Threshold (Note 12)		0.75		F.S.

NOTES:

1. There is one NRZ data bit per clock period. Clock must be phased with digital data such that a positive clock transition occurs in the middle of each received data bit.
2. Logic inputs are CMOS compatible at supply voltage and are diode protected. Digital data input is NRZ at clock rate.
3. As mentioned elsewhere, this output includes a DC bias of VDD/2. Therefore an AC coupling capacitor (min. 4.7 μf) is required unless the output filter also includes this bias (as does the circuit in Fig. 2.)
4. Presents 100 kilohms in series with recovered audio voltage. Zero-signal reference is VDD/2.
5. Note that filter time constants are inversely proportional to clock rate.
6. Step size compression ratio of the syllabic filter is defined as the ratio of the filter output, with an equal 1-0 bit density input to the filter, to its minimum output.
7. Minimum quantization voltage level expressed as a percentage of supply voltage.
8. The minimum step size between levels is twice the resolution.
9. For large signal amplitudes or high frequencies, the encoder may become slope-overloaded. Figure 1 shows the frequency response at various signal levels, measured with a 3kHz low-pass filter having a 130dB/octave roll-off to -50dB. See Figure 2.
10. Table I shows the SNR under various conditions, using the output filter described in Note 9 at a bit rate of 16K bits/sec. See Figure 2.
11. The "quieting" pattern or idle-channel audio output steps at 1/2 the bit rate, changing state on negative clock transitions.
12. The recovered signal will be clamped, and the computation will be inhibited, when the recovered signal reaches three-quarters of full-scale value, and will unclamp when it falls below this value (positive or negative).

TABLE I

INPUT FREQUENCY Hz	INPUT AMPLITUDE mV RMS	OUTPUT SNR dB MIN.
300	1400	20
300	45	15
1000	500	14
1000	16	9

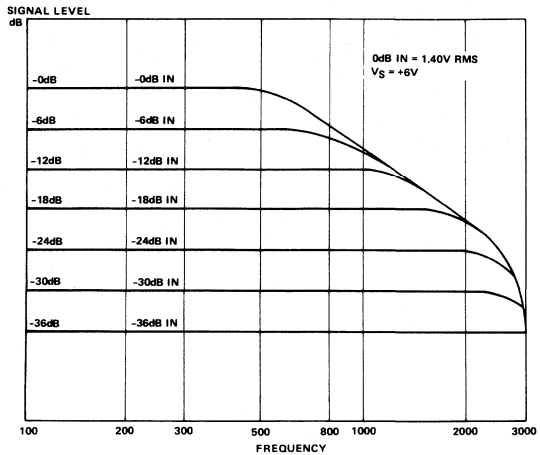
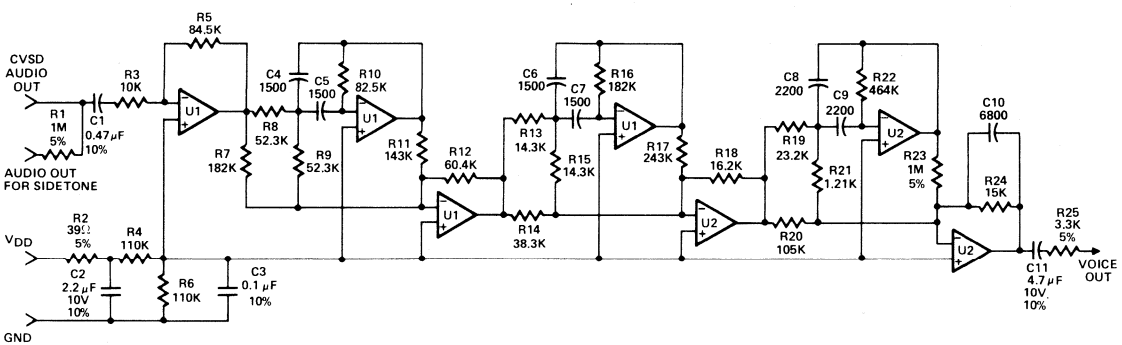


Figure 1. Transfer Function for CVSD at 16K Bits/Sec.



U1, U2 HARRIS HA-4741 QUAD OP AMP
CAPACITORS IN pF UNLESS OTHERWISE STATED

RESISTORS 1/20 WATT

CAP. TOL. 1% UNLESS OTHERWISE STATED

RES. TOL. 1% UNLESS OTHERWISE STATED

FILTER FREQUENCY RESPONSE	
FREQUENCY	RELATIVE OUTPUT
100Hz to 1500Hz	0 ± 1.5dB
1500Hz to 3000Hz	0 ± 2.5dB
3800Hz to 100kHz	Less Than -45dB

Figure 2. Suggested Output Filter for SNR Measurement

High Temperature Electronics

To serve the growing need for electronics that will operate in severe high temperature environments, Harris will offer integrated circuits that have been characterized over elevated temperatures and that have electrical characteristics guaranteed at 200°C.

Typical applications include:

- Well Logging
- Industrial Process Control
- Engine Control and Testing
- High Temperature Data Acquisition Systems

It is the intention of Harris Semiconductor to make available in the high temperature series (identified by the -1 suffix following the device part number) all the basic elements required for the designer to build a data acquisition system that will function to specified limits at 200°C.

The devices to be offered:

- Operational Amplifiers
- Comparators
- Analog Switches
- Analog Multiplexers
- Precision Voltage Reference
- 12 Bit Digital to Analog Converter

All parts offered in the -1 series have had their electrical performance parameters characterized up to 250°C.

Production flow of -1 parts includes screening to MIL-STD-883B, 160 hours burn-in and final electrical test at 200°C.

Devices available Now:

- HA-2600-1 Operational Amplifier
- HA-2620-1 Operational Amplifier
- HA-4920-1 Quad Comparator
- HI-200-1 Analog Switch
- HI-201A-1 Analog Switch
- HI-508A-1 Analog Multiplexer

Devices in Process:

- HA-1610-1 Precision 10V Reference
- HI-562-1 12 Bit Digital to Analog Converter

Consult factory for price and availability information.

Advanced Packaging Techniques

Harris Semiconductor is now offering Leadless Chip Carriers (LCC) as a packaging option on various Analog integrated circuits. An LCC is a square or rectangular package for an Integrated Circuit (IC) that is manufactured in the same manner as a conventional side-braze dual-in-line package (DIP). The LCC is essentially comprised of the cavity and seal ring section of a standard DIP. It offers the user a means of achieving high density system configurations while retaining the reliability benefits of hermetic IC packaging. Figure 1 provides a comparison of the construction of an LCC and a conventional side-braze DIP.

The LCC's two principle advantages over conventional side braze DIPs are packaging density and electrical performance. Packaging density is the number one advantage to an LCC over a side braze DIP. The size of a DIP is governed primarily by the number of leads required and not by the size of the IC. As pin count increases, more and more of the DIP package is used only to provide an electrical trace path to the external leads. The size of an LCC is dependant on the size of the die not on the number of leads. As pin count increases, overall size increases but at a much slower rate. Table 1 provides a comparison between the areas of 18, 28, and 48 lead LCCs to 18, 28, and 48 lead side braze DIPs. The chart indicates a 270% improvement in packaging area for the 18 lead LCC, and 542% improvement for the 48 lead LCC. Obviously, sizable savings in circuit board area can be achieved with this packaging option. The second major advantage of the LCC is in electrical performance. The package size and geometry also dictates trace length and uniformity. Figure 2 provides a comparison between the trace lengths for various LCCs and side braze DIPs. As pin

count goes up, trace lengths get longer, adding resistance and capacitance unequally around the package. As ICs get faster and more complex, these factors start to become a limiting factor on performance. LCCs minimize this effect by maintaining, as close as possible, uniform trace length so that the package is significantly smaller determinant of system performance.

The LCC also offers environmental advantages over "chip-and-wire" manufacturing techniques used in high density hybrid circuits. An IC can be fully tested, burned-in and processed to MIL-STD-883B in an LCC, thereby guaranteeing its performance. The IC is further protected by small hermetic package in which internal water vapor content can be carefully controlled during production.

In summary, Harris Semiconductor Leadless Chip Carriers use a proven technology to provide a reliable high density, high performance packaging option for today's systems.

A list of products available in LCC form is provided in the Packaging Section on page 9-2. Consult the factory or your Harris sales representative for pricing and availability.

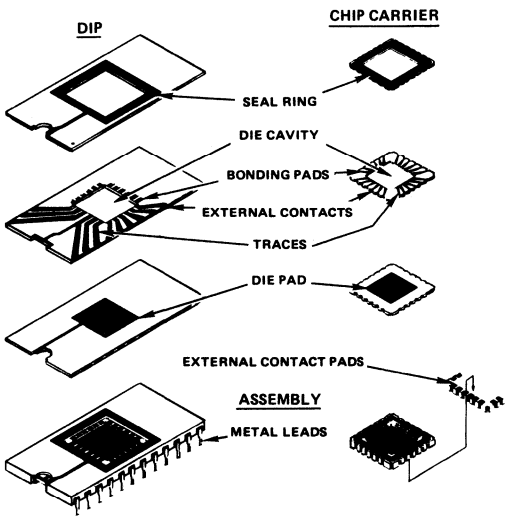
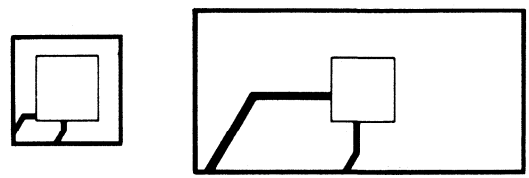


FIGURE 1. Exploded view of Chip Carrier and DIP.



LEAD COUNT	LONGEST TRACE DIP LONGEST TRACE CC	LONGEST TRACE SHORTEST TRACE	
		CC	DIP
18	2:1	1.5:1	6:1
24	4:1	1.5:1	3:1
40	5:1	1.5:1	6:1
54	6:1	1.5:1	7:1

FIGURE 2. Electrical Performance (Resistance and Speed)

TABLE I

	LCC	DIP	DIP AREA LCC AREA
18 Lead	0.10	0.22	270
28 Lead	0.20	0.84	420
48 Lead	0.31	1.68	542

(All units in square inches)

Operational Amplifiers and Comparators

2

ABSOLUTE MAXIMUM RATINGS

As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Characteristics" are the only conditions recommended for satisfactory operation.

Operational Amplifiers Selection Guide

QUAD OPERATIONAL AMPLIFIERS

PARAMETER	HA-2400	HA-2404	HA-2405	HA-4602	HA-4605	HA-4622	HA-4625	HA-4741	HA-4741	UNITS
INPUT CHARACTERISTICS										
Offset Voltage	7	7	11	3.0	4.0	3.0	4.0	5.0	6.5	mV
Drift (Typ)	20	20	30	2	2	2	2	5	5	µV/°C
Bias Current	400	400	500	325	400	325	400	325	400	nA
Offset Current	100	100	100	125	120	125	120	75	100	nA
Common Mode Range	± 9.0	± 9.0	± 9.0	±12	±12	±12	±12	±12	±12	V
TRANSFER CHARACTERISTICS										
Large Signal Voltage Gain	25k	25k	25k	100k	75k	100k	75k	25k	15k	V/V
CommonModeRejection Ratio	80	80	74	86	80	86	80	74	74	dB
Bandwidth (Typ) (1)	40	40	40	8	8	70	70	3.5	3.5	MHz
OUTPUT CHARACTERISTICS										
Output Voltage Swing	±10	±10	±10	±10	±10	±10	±10	±10	±10	V
Output Current (1)	± 10	± 10	± 10	±10	±8	±10	±8	±5	±5	mA
Full Power Bandwidth (Typ) (1)	500	500	500	60	60	150	130	25	25	kHz
TRANSIENT RESPONSE										
Rise Time (1) (Typ)	20	20	20	50	50	38	38	75	75	ns
Overshoot (1) (Typ)	25	25	25	30	30	45	45	25	25	%
Slew Rate (1) (Typ)	±30	±30	±30	±4	±4	±12	±11	±1.6	±1.6	V/µs
Settling Time (Typ) (1)	1.5	1.5	1.5	4.2	4.2	2.5	2.5	12	12	µs
POWER SUPPLY CHARACTERISTICS										
Supply Current (1)	6.0	6.0	6.0	5.5	6.5	4.6	5.0	5	7	mA
Power Supply Rejection Ratio	74	74	74	86	80	86	80	80	80	dB
FUNCTIONAL CHARACTERISTICS										
Offset Adjustment	NO	NO	NO	NO	NO	NO	NO	NO	NO	
Compensation Components	0AV>10	0AV>10	0AV>10	0	0	0AV>10	0AV>10	0	0	
Output Protection	YES	YES	YES	YES	YES	YES	YES	YES	YES	
Temperature Range*	(A)	(C)	(B)	(A)	(B)	(A)	(B)	(A)	(B)	

FOOTNOTES: (1) At +25°C. (2) Not applicable or not specified. (3) Dependent upon I_{SET} value.
* Temperature Range: (A) −55°C to +125°C (B) 0°C to +75°C (C) −25°C to +85°C

Note: Parameters are minimum or maximum over temperature unless otherwise noted.

SPECIAL-PURPOSE AMPLIFIERS

PARAMETER	HA-2530	HA-2535	HA-2630	HA-2635	HA-2640	HA-2645	HA-2720	HA-2725	HA-2900	HA-2904	HA-2905	UNITS
INPUT CHARACTERISTICS							(3)	(3)				
Offset Voltage	3	5	300	300	6	7	5	7	.06	.05	.08	mV
Drift (Typ)	5	5	(2)	(2)	15	15	8 to 10	8 to 10	0.3	0.2	0.2	µV/°C
Bias Current	100	200	200	200	50	50	10 to 40	10 to 40	1	1	1	nA
Offset Current	20	20	(2)	(2)	35	50	7.5 to 20	7.5 to 20	0.5	0.5	0.5	nA
Common Mode Range	±0.5	±0.5	(2)	(2)	±35	±35	±10	±10	±10	±10	±10	V
TRANSFER CHARACTERISTICS							(3)	(3)				
Large Signal Voltage Gain	100k	100k	0.85	0.85	75k	75k	25k	20k	10^6	10^6	10^6	V/V
Common Mode Rejection Ratio	86	80	(2)	(2)	80	74	80	74	120	130	120	dB
Bandwidth (Typ) (1)	20	20	8	8	4	4	.01 to 10	.01 to 10	3	3	3	MHz
OUTPUT CHARACTERISTICS							(3)	(3)				
Output Voltage Swing	±10	±10	±10	±10	±35	±35	±13.5	±13.5	±10	±10	±10	V
Output Current (1)	±25	±25	±400	±300	±12	±10	±0.5 to 5	±0.5 to 5	±10	±10	±7	mA
Full Power Bandwidth (Typ) (1)	5,000	5,000	8,000	8,000	23	23	1.5 to 80	1.5 to 80	40	40	40	kHz
TRANSIENT RESPONSE							(3)	(3)				
Rise Time (1)	40	40	30	30	60	60	200 to 2,000	200 to 2,000	200	200	200	ns
Overshoot (1)	45	50	25	25	15	15	5 to 15	5 to 15	20	20	20	%
Slew Rate (1)	±280	±250	±200	±200	5	5	0.1 to 0.8	0.1 to 0.8	2.5	2.5	2.5	V/µs
Settling Time (Typ) (1)	0.5	0.5	0.5	0.5	1.5	1.5	(2)	(2)	(2)	(2)	(2)	µs
POWER SUPPLY CHARACTERISTICS							(3)	(3)				
Supply Current (1)	6	6	20	23	3.8	4.5	.02 to 0.2	.02 to 0.2	5	5	5	mA
Power Supply Rejection Ratio	86	80	66	66	80	74	80	76	120	130	120	dB
FUNCTIONAL CHARACTERISTICS												
Offset Adjustment	NO	NO	NO	NO	YES	YES	YES	YES	NO	NO	NO	
Compensation Components	1	1	0	0	0	0	0	0	3	3	3	
Output Protection	NO	NO	External	External	YES	YES	YES	YES	YES	YES	YES	
Temperature Range*	(A)	(B)	(A)	(B)	(A)	(B)	(A)	(B)	(A)	(C)	(B)	

FOOTNOTES: (1) At +25°C. (2) Not applicable or not specified. (3) Dependent upon I_{SET} value.
* Temperature Range: (A) −55°C to +125°C (B) 0°C to +75°C (C) −25°C to +85°C

Operational Amplifiers Selection Guide

	FET INPUT AMPLIFIERS						FAST SETTLING AMPLIFIER		
PARAMETER	HA-5100	HA-5105	HA-5110	HA-5115	HA-5150†	HA-5160†	HA-5190	HA-5195	UNITS
INPUT CHARACTERISTICS									
Offset Voltage	2.0	3.5	2.0	3.5	2.0	2.0	10	10	mV
Drift (Typ)	10	15	10	15	10	10	20	20	µV/°C
Bias Current	10	20	10	20	10	10	20 µA	20 µA	nA
Offset Current	5	10	5	10	5	5	6 µA	6 µA	nA
Common Mode Range	±10	±10	±10	±10	±10	±10	±5	±5	V
TRANSFER CHARACTERISTICS									
Large Signal Voltage Gain	60k	40k	60k	40k	50k	50k	5k	5k	V/V
Common Mode Rejection Ratio	86	80	86	80	86	86	74	74	dB
Bandwidth (Typ) (1)	18	18	60	50	50	100	150	150	MHz
OUTPUT CHARACTERISTICS									
Output Voltage Swing	±12	±11	±12	±11	±10	±10	±5	±5	V
Output Current (1)	±10	±8	±10	±8	±10	±10	±25	±25	mA
Full Power Bandwidth (Typ)(1)	100	80	800	625	750	5,000	6,500	6,500	kHz
TRANSIENT RESPONSE									
Rise Time (1) (Typ)	15	20	20	20	15	15	13	13	ns
Overshoot (1) (Typ)							8	8	%
Slew Rate (1) (Typ)	±6	±5	±35	±35	±60	±120	±200	±200	v/µs
Settling Time (Typ) (1)	1.7	2.0	0.85	1.0	0.7	0.5	0.1	0.1	µs
POWER SUPPLY CHARACTERISTICS									
Supply Current (1)	7	8	7	8	7	7	28	28	mA
Power Supply Rejection Ratio	86	80	86	80	86	86	70	70	dB
FUNCTIONAL CHARACTERISTICS									
Offset Adjustment	YES	YES	YES	YES	YES	YES			
Compensation Components	0	0	0AV>10	0AV>10	0	0AV>10	0AV>5	0AV>5	
Output Protection	YES	YES	YES	YES	YES	YES	NO	NO	
Temperature Range*	(A) (B)	(B)	(A) (B)	(B)	(A)	(B)	(A)	(B)	

FOOTNOTES: (1) At +25°C. (2) Not applicable or not specified. (3) Dependent upon I_{SET} value.
* Temperature Range: (A) −55°C to +125°C (B) 0°C to +75°C (C) −25°C to +85°C
† To be introduced.

	LOW POWER AMPLIFIER			DUAL HIGH PERFORMANCE AMPLIFIERS				
PARAMETER	HA-2700	HA-2704	HA-2705	HA-2650	HA-2655	HA-2730	HA-2735	UNITS
INPUT CHARACTERISTICS						(3)	(3)	
Offset Voltage	5	6	7	5	7	5	7	mV
Drift (Typ)	5	5	5	8	8	8 to 10	8 to 10	µV/°C
Bias Current	50	50	70	200	300	10 to 40	10 to 40	nA
Offset Current	30	30	40	60	100	7.5 to 20	7.5 to 20	nA
Common Mode Range	±11	±11	±11	±13	±13	±10	±10	V
TRANSFER CHARACTERISTICS						(3)	(3)	
Large Signal Voltage Gain	100k	100k	100k	20k	15k	25k	20k	V/V
Common Mode Rejection Ratio	86	86	80	80	74	80	74	dB
Bandwidth (Typ) (1)	1	1	1	8	8	.01 to 10	.01 to 10	MHz
OUTPUT CHARACTERISTICS						(3)	(3)	
Output Voltage Swing	±11	±11	±11	±13	±13	±13.5	±13.5	V
Output Current (1)	+15	+15	+15	±20	±18	±0.5 to 5	±0.5 to 5	mA
Full Power Bandwidth (Typ)(1)	50	50	50	30	30	1.5 to 80	1.5 to 80	kHz
TRANSIENT RESPONSE								
Rise Time (1)	(2)	(2)	(2)	40	40	200 to 2,000	200 to 2,000	ns
Overshoot (1)	(2)	(2)	(2)	15	15	5 to 15	5 to 15	%
Slew Rate (1)	±10	±10	±10	±2	±2	0.1 to 0.8	0.1 to 0.8	V/µs
Settling Time (Typ) (1)	5.0	5.0	5.0	1.5	1.5	(2)	(2)	µs
POWER SUPPLY CHARACTERISTICS						(3)	(3)	
Supply Current (1)	0.15	0.15	0.15	3	4	0.02 to 0.2	0.02 to 0.2	mA
Power Supply Rejection Ratio	86	86	80	80	74	80	76	dB
FUNCTIONAL CHARACTERISTICS								
Offset Adjustment	YES	YES	YES	DIP Only	DIP Only	YES	YES	
Compensation Components	0	0	0	0	0	0	0	
Output Protection	YES	YES	YES	YES	YES	YES	YES	
Temperature Range*	(A)	(C)	(B)	(A)	(B)	(A)	(B)	

FOOTNOTES: (1) At +25°C. (2) Not applicable or not specified. (3) Dependent upon I_{SET} value.
* Temperature Range: (A) −55°C to +125°C (B) 0°C to +75°C (C) −25°C to +85°C

Note: Parameters are minimum or maximum over temperature unless otherwise noted.

2

Operational Amplifiers Selection Guide

HIGH SLEW RATE AMPLIFIERS

PARAMETER	HA-2500	HA-2502	HA-2505	HA-2507	HA-2510	HA-2512	HA-2515	HA-2517	HA-2520	HA-2522	HA-2525	HA-2527	UNITS
INPUT CHARACTERISTICS													
Offset Voltage	8	10	10	10	11	14	14	14	11	14	14	14	mV
Drift (Typ)	20	20	20	25	20	25	30	30	20	25	20	30	µV/°C
Bias Current	400	500	500	500	400	500	500	500	400	500	500	500	nA
Offset Current	50	100	100	100	50	100	100	100	50	100	100	100	nA
Common Mode Range	±10	±10	±10	±10	±10	±10	±10	±10	±10	±10	±10	±10	V
TRANSFER CHARACTERISTICS													
Large Signal Voltage Gain	15k	10k	10k	10k	7.5k	5k	5k	5k	7.5k	5k	5k	5k	V/V
Common Mode Rejection Ratio	80	74	74	74	80	74	74	74	80	74	74	74	dB
Bandwidth (Typ) (1)	12	12	12	12	12	12	12	12	25	25	25	20	MHz
OUTPUT CHARACTERISTICS													
Output Voltage Swing	±10	±10	±10	±10	±10	±10	±10	±10	±10	±10	±10	±10	V
Output Current (1)	±10	±10	±10	±10	±10	±10	±10	±10	±10	±10	±10	±10	mA
Full Power Bandwidth (Typ) (1)	500	500	500	500	1000	1000	1000	1000	1500	1200	1200	1200	kHz
TRANSIENT RESPONSE													
Rise Time (1)	50	50	50	50	50	50	50	50	50	50	50	50	ns
Overshoot (1)	40	50	50	50	40	50	50	50	40	50	50	50	%
Slew Rate (1)	±25	±20	±20	±15	±50	±40	±40	±30	±100	±80	±80	±60	V/µs
Settling Time (Typ) (1)	0.33	0.33	0.33	0.33	0.25	0.25	0.25	0.25	0.70	0.70	0.70	0.70	µs
POWER SUPPLY CHARACTERISTICS													
Supply Current (1)	6.0	6.0	6.0	6.0	6.0	6.0	6.0	6.0	6.0	6.0	6.0	6.0	mA
Power Supply Rejection Ratio	80	74	74	74	80	74	74	74	80	74	74	74	dB
FUNCTIONAL CHARACTERISTICS													
Offset Adjustment	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	
Compensation Components	0	0	0	0	0	0	0	0	0AV>3	0AV>3	0AV>3	0AV>3	
Output Protection	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO	
Temperature Range*	(A)	(A)	(B)	(B)	(A)	(A)	(B)	(B)	(A)	(A)	(B)	(B)	

FOOTNOTES: (1) At +25°C. (2) Not applicable or not specified. (3) Dependent upon I_{SET} value.
*Temperature Range: (A) −55°C to +125°C (B) 0°C to +75°C (C) −25°C to +85°C

WIDE BANDWIDTH AMPLIFIERS

PARAMETER	HA-2600	HA-2602	HA-2605	HA-2607	HA-2620	HA-2622	HA-2625	HA-2627	UNITS
INPUT CHARACTERISTICS									
Offset Voltage	6	7	7	8	6	7	7	8	mV
Drift (Typ)	5	5	5	5	5	5	5	5	µV/°C
Bias Current	30	60	40	50	35	60	40	50	nA
Offset Current	30	60	40	50	35	60	40	50	nA
Common Mode Range	±11	±11	±11	±10	±11	±11	±11	±10	V
TRANSFER CHARACTERISTICS									
Large Signal Voltage Gain	70k	60k	70k	60k	70k	60k	70k	60k	V/V
Common Mode Rejection Ratio	80	74	74	74	80	74	74	74	dB
Bandwidth (Typ) (1)	12	12	12	12	100	100	100	100	MHz
OUTPUT CHARACTERISTICS									
Output Voltage Swing	±10	±10	±10	±10	±10	±10	±10	±10	V
Output Current (1)	±15	±10	±10	±10	±10	±10	±10	±10	mA
Full Power Bandwidth (Typ) (1)	75	75	75	75	600	600	600	600	kHz
TRANSIENT RESPONSE									
Rise Time (1)	60	60	60	60	45	45	45	45	ns
Overshoot (1)	40	40	40	40	40	40	40	40	%
Slew Rate (1)	±4	±4	±4	±4	±25	±20	±20	±17	V/µs
Setting Time (Typ) (1)	1.5	1.5	1.5	1.5	0.30	0.30	0.30	0.30	µs
POWER SUPPLY CHARACTERISTICS									
Supply Current (1)	3.7	4.0	4.0	4.0	3.7	4.0	4.0	4.0	mA
Power Supply Rejection Ratio	80	74	74	74	80	74	74	74	dB
FUNCTIONAL CHARACTERISTICS									
Offset Adjustment	YES	YES	YES	YES	YES	YES	YES	YES	
Compensation Components	0	0	0	0	0AV>5	0AV>5	0AV>5	0AV>5	
Output Protection	YES	YES	YES	YES	YES	YES	YES	YES	
Temperature Range*	(A)	(A)	(B)	(B)	(A)	(A)	(B)	(B)	

FOOTNOTES: (1) At +25°C (2) Not applicable or not specified. (3) Dependent upon I_{SET} value.
*Temperature Range: (A) −55°C to +125°C (B) 0°C to +75°C (C) −25°C to +85°C

Note: Parameters are minimum or maximum over temperature unless otherwise noted.

Comparators Selection Guide

Harris presently manufactures three different comparators:

HA-4900	General Purpose Quad
HA-4920	High Speed Quad
HA-4950	Precision, High Speed Single

The basic characteristics of these devices are shown tabulated below. For complete details refer to individual device specifications.

Parameter	-55°C to +125°C			0°C to +125°C			Units
	HA-4900	HA-4920	HA-4950	HA-4900	HA-4920	HA-4950	
Input Offset Voltage	4.0	4.0	2.8	10.0	8.0	2.8	mV
Input Sensitivity (Note 1)	0.7	0.6	0.1	0.7	0.6	0.1	mV
Input Bias Current	150	8	7	75	10	7	μA
Response Time (At T = +25°C)							
Tpd 0	130	45	40	130	45	40	ns
Tpd 1	180	40	20	180	40	20	ns

Note 1. Input sensitivity is the differential voltage required at the input to make the output change state, after the offset has been nulled.

PRAM PROGRAMMABLE AMPLIFIER HA-2400/2404/2405

One of four op amp input stages may be digitally selected to be connected to a single output. Replaces 5 op amps and a four channel multiplexer to obtain programmable gain, signal selection or countless other functions.

CURRENT BOOSTER AMPLIFIER HA-2630/2635

A unity gain amplifier with output current up to ±400mA, and 600V/μ s slew rate, designed for use in series with any op amp output. For Coax line drivers, servo amps, audio amps, clock drivers etc.

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HA-909/911

Wideband, Low Noise, Operational Amplifiers

2

FEATURES

- LOW BROADBAND NOISE — 1μV R.M.S.
- LOW NOISE VOLTAGE — 7nV/$\sqrt{Hz}$
- LOW OFFSET VOLTAGE — 2mV
- WIDE BANDWIDTH — 7MHz
- POWER BANDWIDTH — 20kHz
- SUPPLY RANGE — ±5V TO ±20V
- INTERNALLY COMPENSATED

APPLICATIONS

- HIGH Q, WIDEBAND FILTERS
- AUDIO AMPLIFIERS
- SIGNAL GENERATORS

DESCRIPTION

HA-909 and HA-911 are monolithic ampliifers delivering very low noise and excellent bandwidth specifications without the need for external compensation. Additional features of these dielectrically isolated devices include low offset voltage, offset trim capabitlity (14-pin flat package only), and high output current drive capabitlity.

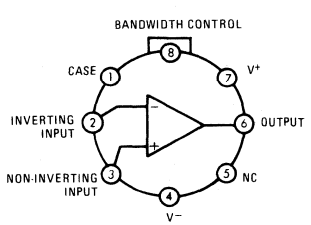
With 7MHz bandwidth and internal compensation these amplifiers are extremely useful in many active filter designs. In audio circuitry requiring quiet operation these devices offer 1 μ V typical broadband noise (10Hz to 1kHz) and 20kHz power bandwidth. 2mV typical offset voltage, offset trim capability, and 20mA output current drive capability (±10.0V swing) make these amplifiers useful in signal conditioning circuits.

HA-909 and HA-911 are available in metal can (TO-99) and 14-pin flat packages. HA-909 is specified over the -55°C to +125°C range. HA-911 is specified from 0°C to +75°C.

PINOUT

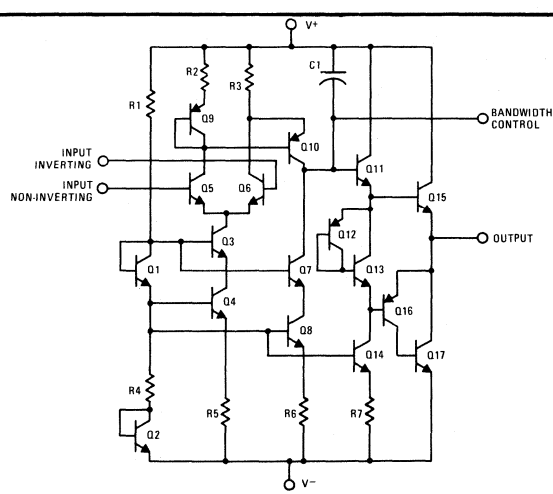
Package Code 2A

TO-99 TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	50.0V
Differential Input Voltage	±7.0V
Peak Output Current	±50mA
Internal Power Dissipation (Note 10)	300mW
Operating Temperature Range – HA-909	$-55^oC \leq T_A \leq +125^oC$
HA-911	$0^oC \leq T_A \leq +75^oC$
Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: $V_{Supply} = \pm 15.0V$ unless otherwise specified.

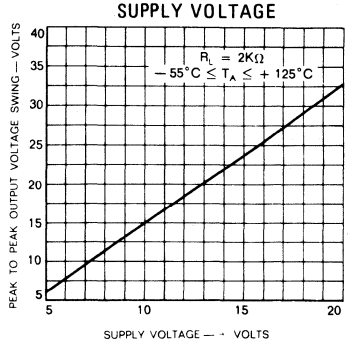
PARAMETER	TEMP.	HA-909 -55°C to +125°C MIN.	HA-909 TYP.	HA-909 MAX.	HA-911 0°C to +75°C MIN.	HA-911 TYP.	HA-911 MAX.	UNITS
INPUT CHARACTERISTICS								
* Offset Voltage	+25°C		2.0	5.0		2.0	6.0	mV
	Full			6.0			7.5	mV
Equivalent Input Noise (Note 9)	+25°C		1.0	5.0		1.0		μV
Input Noise Voltage	+25°C		7			7		$nV/\sqrt{Hz}$
* Bias Current	+25°C		87	300		200	500	nA
	Full			750		300	750	nA
* Offset Current	+25°C		25	150		100	300	nA
	Full		50	300		150	450	nA
Offset Current Average Drift	Full		1.0			1.0		nA/°C
Input Resistance (Note 12)	+25°C	200	600		100	250		KΩ
	Full	100	300					KΩ
Common Mode Range	Full	+12.0			+12.0			V
TRANSFER CHARACTERISTICS								
* Large Signal Voltage Gain (Notes 1, 4)	+25°C	25K	45K		20K	45K		V/V
	Full	25K	45K		15K	45K		V/V
Full Power BW	+25°C		20			20		KHz
* Common Mode Rejection Ratio (Note 2)	Full	80	96		74	90		dB
Unity Gain Bandwidth (Note 3)	+25°C		7			7		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 1)	Full	+12.0			+11.0			V
* Output Current (Note 4)	+25°C	+20			+15			mA
Output Resistance	+25°C		150			500		Ohms
TRANSIENT RESPONSE								
Rise Time (Notes 1, 5, 6, 8 & 11)	+25°C		40	75		40	75	ns
Overshoot (Notes 1, 5, 6, 8 & 11)	+25°C		15	40		15	40	%
* Slew Rate (Notes 1, 5 & 8)	+25°C	+3.5	+5.0			+5.0		V/μs
		-1.2	-2.0			-2.0		
POWER SUPPLY CHARACTERISTICS								
* Supply Current	+25°C		1.8	2.5		1.8	2.5	mA
* Power Supply Rejection Ratio (Note 7)	Full	80	92		74	90		dB

NOTES:
1. $R_L = 2K\Omega$
2. $V_{CM} = \pm 10V$
3. $V_O < 90mV$
4. $V_O = \pm 10.0V$
5. $C_L = 100pF$
6. $V_O = +200mV$
7. $\Delta V_{Sup} = \pm 5V$
8. See Transient Response test circuits and waveforms
9. 10 - 1000Hz, $R_S = 10K$
10. Derate by 6.6mW/°C above 105°C
11. Positive Transitions only.
12. This parameter based on design calculation.

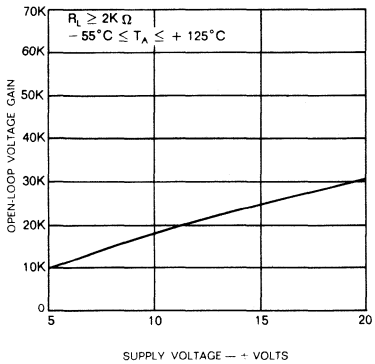
*100% Tested For DASH 8

GUARANTEED ELECTRICAL CHARACTERISTICS

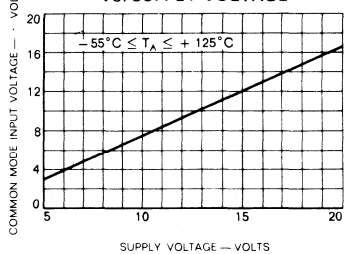
OUTPUT VOLTAGE SWING VS. SUPPLY VOLTAGE



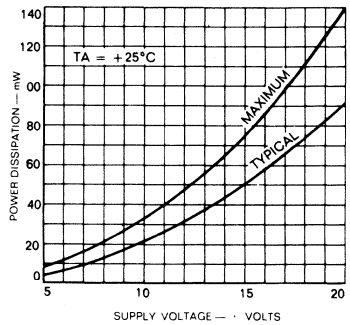
OPEN LOOP VOLTAGE GAIN VS. SUPPLY VOLTAGE



COMMON MODE INPUT VOLTAGE VS. SUPPLY VOLTAGE

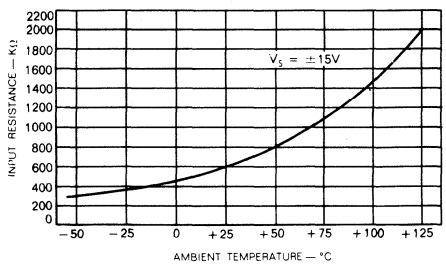


POWER DISSIPATION VS. SUPPLY VOLTAGE

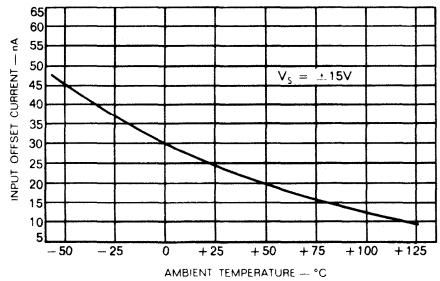


TYPICAL PERFORMANCE CURVES

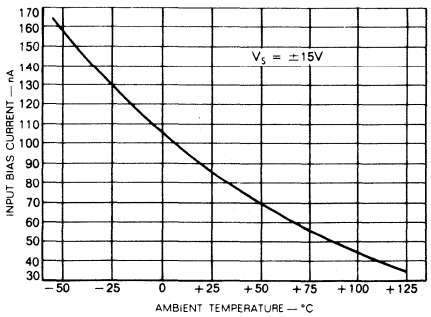
INPUT RESISTANCE VS. AMBIENT TEMPERATURE



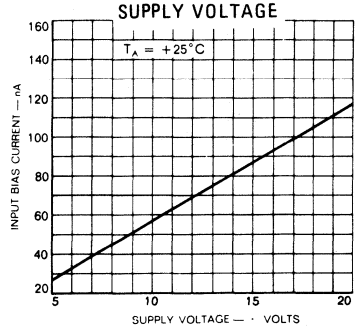
INPUT OFFSET CURRENT VS. AMBIENT TEMPERATURE



INPUT BIAS CURRENT VS. AMBIENT TEMPERATURE

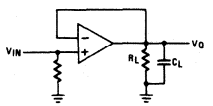


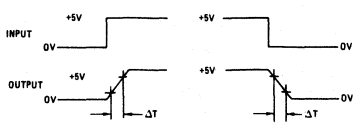
INPUT BIAS CURRENT VS. SUPPLY VOLTAGE



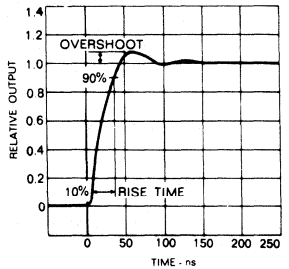
TYPICAL PERFORMANCE CURVES(continued)

SLEW RATE TEST CIRCUIT

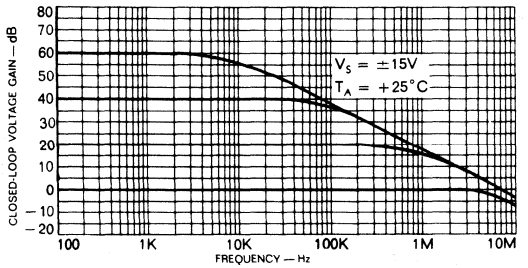




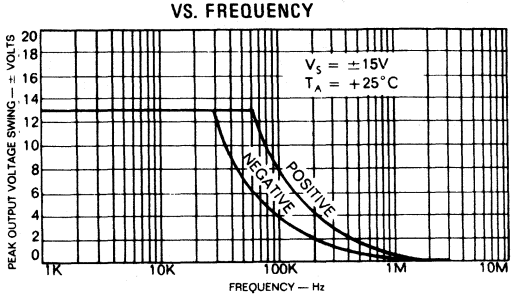
TRANSIENT RESPONSE



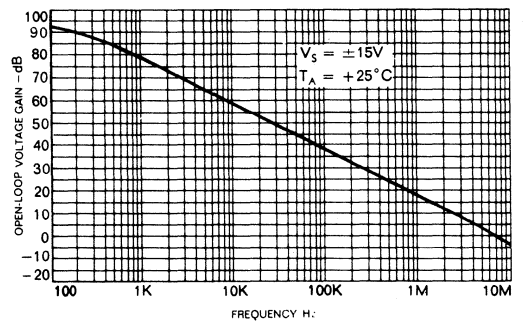
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS



OUTPUT VOLTAGE SWING VS. FREQUENCY



OPEN LOOP FREQUENCY RESPONSE



2

DEFINITIONS

INPUT OFFSET VOLTAGE – That voltage which must be applied between the input terminals through two equal resistances to force the output voltage to zero.

INPUT OFFSET CURRENT – The difference in the currents into the two input terminals when the output is at zero voltage.

INPUT BIAS CURRENT – The average of the currents flowing into the input terminals when the output is at zero voltage.

INPUT COMMON MODE VOLTAGE – The average referred to ground of the voltages at the two input terminals.

COMMON MODE RANGE – The range of voltages which is exceeded at either input terminal will cause the amplifier to cease operating.

COMMON MODE REJECTION RATIO – The ratio of a specified range of input common mode voltage to the peak-to-peak change in input offset voltage over this range.

OUTPUT VOLTAGE SWING – The peak symmetrical output voltage swing, referred to ground, that can be obtained without clipping.

INPUT RESISTANCE – The ratio of the change in input voltage to the change in input current.

OUTPUT RESISTANCE – The ratio of the change in output voltage to the change in output current.

POSITIVE OUTPUT VOLTAGE SWING – The peak positive output voltage swing, referred to ground, that can be obtained without clipping.

NEGATIVE OUTPUT VOLTAGE SWING – The peak negative output voltage swing, referred to ground, that can be obtained without clipping.

VOLTAGE GAIN – The ratio of the change in output voltage to the change in input voltage producing it.

BANDWIDTH – The frequency at which the voltage gain is 3dB below its low frequency value.

UNITY GAIN BANDWIDTH – The frequency at which the voltage gain of the amplifier is unity.

POWER SUPPLY REJECTION RATIO – The ratio of the change in input offset voltage to the change in power supply voltage producing it.

TRANSIENT RESPONSE – The closed loop step function response of the amplifier under small signal conditions.

PHASE MARGIN – $(180^o - (\phi_1 - \phi_2))$ where ϕ_1 is the phase shift at the frequency where the absolute magnitude of gain is unity ϕ_2 is the phase shift at a frequency much lower than the open loop bandwidth.

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HA-2400/2404/2405

PRAM Four Channel Programmable Amplifier

2

FEATURES

- PROGRAMMABILITY
- HIGH SLEW RATE 30V/μs
- WIDE GAIN BANDWIDTH 40MHz
- HIGH GAIN 150,000
- LOW OFFSET CURRENT 5nA
- HIGH INPUT IMPEDANCE 30MΩ
- SINGLE CAPACITOR COMPENSATION
- DTL/TTL COMPATIBLE INPUTS

APPLICATIONS

- THOUSANDS OF NEW APPLICATIONS; PROGRAM
  - SIGNAL SELECTION/MULTIPLEXING
  - OP AMP GAIN
  - OSCILLATOR FREQUENCY
  - FILTER CHARACTERISTICS
  - ADD-SUBTRACT FUNCTIONS
  - INTEGRATOR CHARACTERISTICS
  - COMPARATOR LEVELS

DESCRIPTION

HA-2400/2404/2405 comprise a series of four-channel programmable amplifiers providing a level of versatility unsurpassed by any other monolithic operational amplifier. Versatility is achieved by employing four input amplifier channels, any one (or none) of which may be electronically selected and connected to a single output stage through DTL/TTL compatible address inputs. The device formed by the output and the selected pair of inputs is an op amp which delivers excellent slew rate, gain bandwidth and power bandwidth performance. Other advantageous features for these dielectrically isolated amplifiers include high voltage gain and input impedance coupled with low input offset voltage and offset current. External compensation is not required on this device at closed loop gains greater than 10.

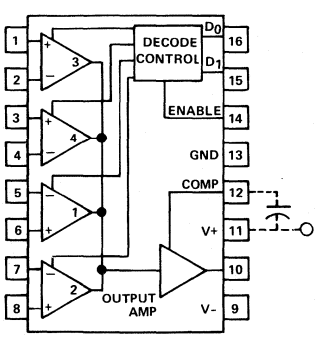
Each channel of the HA-2400/2404/2405 can be controlled and operated with suitable feedback networks in any of the standard op amp configurations. This specialization makes these amplifiers excellent components for multiplexing, signal selection, and mathematical function designs. With 30V/μs slew rate, 40MHz gain bandwidth, and 30M ohms input impedance these devices are ideal building blocks for signal generators, active filters, and data acquisition designs. Programmability coupled with 2mV typical offset voltage and 5nA offset current makes these amplifiers outstanding components for signal conditioning circuits.

HA-2400/2404/2405 are available in a 16 pin dual-in-line package. HA-2400 is specified from -55°C to +125°C. HA-2404 is specified over the -25°C to +85°C range, while HA-2405 operates from 0°C to +75°C.

PINOUT

TOP VIEW

Package Code 5X



TRUTH TABLE

D_1	D_0	EN	SELECTED CHANNEL
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4
X	X	L	NONE

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

SCHEMATIC

Condensed circuit diagram for a programmable amplifier (PRAM HA-2400)

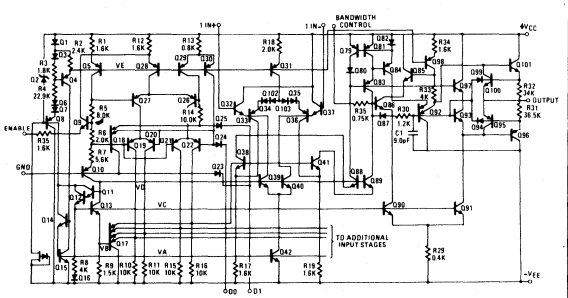


Diagram includes: ONE INPUT STAGE, DECODE CONTROL, BIAS NETWORK AND OUTPUT STAGE

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V− Terminals	45.0V	Internal Power Dissipation (Note 13)	300mW
Differential Input Voltage	$\pm V_{Supply}$	Operating Temperature Range	$-55^oC \leq T_A \leq +125^oC$ (HA-2400)
Digital Input Voltage	−0.76V to +10.0V		$-25^oC \leq T_A \leq +85^oC$ (HA-2404)
Output Current	Short Circuit Protected ($I_{SC} \leq \pm 33mA$)		$0^oC \leq T_A \leq +75^oC$ (HA-2405)
		Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$

ELECTRICAL CHARACTERISTICS

Test Conditions: $V_{Supply} = \pm 15.0V$ unless otherwise specified.

Digital inputs: $V_{IL} = +0.5V$, $V_{IH} = +2.4V$
Limits apply to each of the four channels, when addressed.

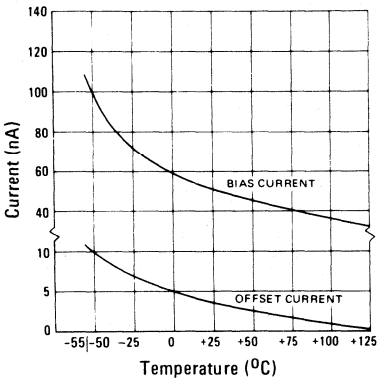
PARAMETER	TEMP.	HA-2400/HA-2404 LIMITS MIN.	TYP.	MAX.	HA-2405 LIMITS MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS								
* Offset Voltage	+25°C		2	5		4	9	mV
	Full			7			11	mV
* Bias Current (Note 12)	+25°C		50	200		50	250	nA
	Full			400			500	nA
* Offset Current (Note 12)	+25°C		5	50		5	50	nA
	Full			100			100	nA
Input Resistance (Note 12)	+25°C		30			30		MΩ
Common Mode Range	Full	±9.0			±9.0			V
TRANSFER CHARACTERISTICS								
* Large Signal Voltage Gain (Note 1,5)	+25°C	50K	150K		50K	150K		V/V
	Full	25K			25K			V/V
* Common Mode Rejection Ratio (Note 2)	Full	80	100		74	100		dB
Gain Bandwidth (Note 3)	+25°C	20	40		20	40		MHz
(Note 4)	+25°C	4	8		4	8		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		V
Output Current	+25°C	10	20		10	20		mA
Full Power Bandwidth (Notes 3, 5)	+25°C	200	500		200	500		kHz
(Notes 4,5)	+25°C	100	200		100	200		kHz
TRANSIENT RESPONSE								
Rise Time (Notes 4,6)	+25°C		20	45		20	50	ns
Overshoot (Notes 4,6)	+25°C		25	40		25	40	%
Slew Rate (Notes 3,7)	+25°C	20	30		20	30		V/μs
(Notes 4,7)	+25°C	6	8		6	8		V/μs
Settling Time (Notes 4, 7, 8)	+25°C		1.5	2.5		1.5	2.5	μs
CHANNEL SELECT CHARACTERISTICS								
Digital Input Current ($V_{IN} = 0V$)	Full		1	1.5		1	1.5	mA
Digital Input Current ($V_{IN} = +5.0V$)	Full		5			5		nA
Output Delay (Note 9)	+25°C		100	250		100	250	ns
Crosstalk (Note 10)	+25°C	-80	-110		-74	-110		dB
POWER SUPPLY CHARACTERISTICS								
* Supply Current	+25°C		4.8	6.0		4.8	6.0	mA
* Power Supply Rejection Ratio (Note 11)	Full	74	90		74	90		dB

NOTES:
1. $R_L = 2K\Omega$
2. $V_{CM} = \pm 5V$.D.C.
3. $A_V = +10$, $C_{COMP} = 0$, $R_L = 2K\Omega$, $C_L = 50pF$
4. $A_V = +1$, $C_{COMP} = 15pF$, $R_L = 2K\Omega$, $C_L = 50pF$
5. $V_{OUT} = 20V$ peak-to-peak
6. $V_{OUT} = 200mV$ peak-to-peak
7. $V_{OUT} = 10.0V$ peak-to-peak
8. To 0.1% of final value
9. To 10% of final value; output then slews at normal rate to final value.
10. Unselected input to output; $V_{IN} = \pm 10$ V.D.C.
11. $V_{SUPP} = \pm 10V$.D.C. to $\pm 20V$.D.C.
12. Unselected channels have approximately the same input parameters.
13. Derate by 4.3mW/°C above 105°C

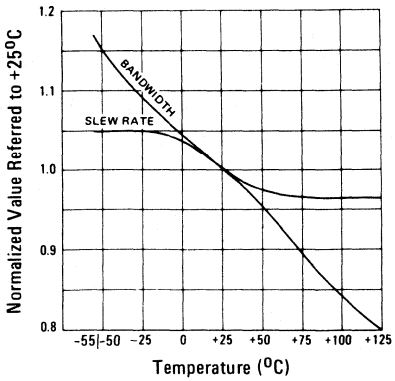
*100% Tested For DASH 8

V+ = 15VDC, V- = 15VDC, T_A = 25°C UNLESS OTHERWISE STATED.

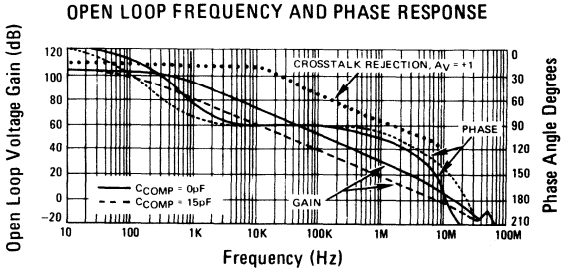
INPUT BIAS CURRENT AND OFFSET CURRENT AS A FUNCTION OF TEMPERATURE



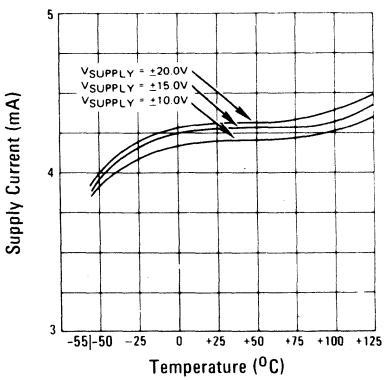
NORMALIZED A.C. PARAMETERS VS. TEMPERATURE



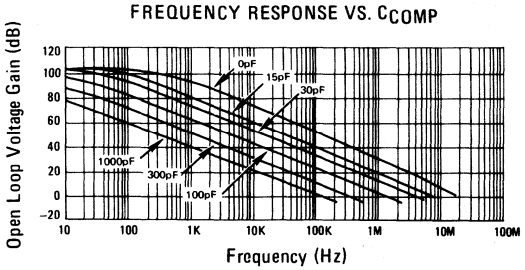
OPEN LOOP FREQUENCY AND PHASE RESPONSE



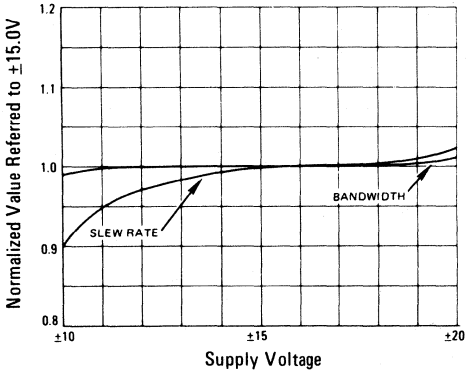
POWER SUPPLY CURRENT DRAIN AS A FUNCTION OF TEMPERATURE



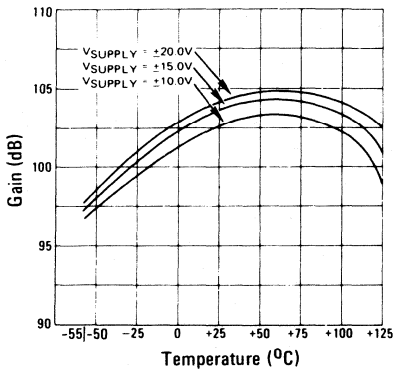
FREQUENCY RESPONSE VS. C_{COMP}



NORMALIZED A.C. PARAMETERS VS. SUPPLY VOLTAGE

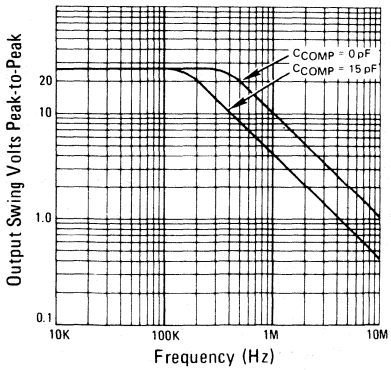


OPEN LOOP VOLTAGE GAIN VS. TEMPERATURE

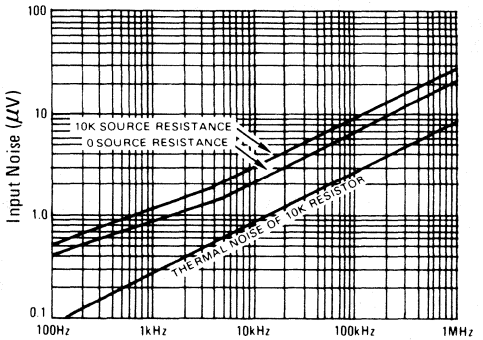


CHARACTERISTIC CURVES (continued)

OUTPUT VOLTAGE SWING VS. FREQUENCY

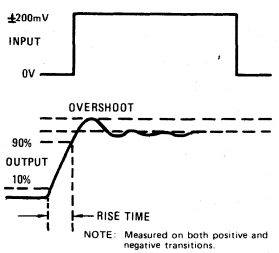


EQUIVALENT INPUT NOISE VS. BANDWIDTH

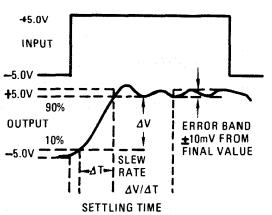


Upper 3dB Frequency
Lower 3dB Frequency - 10Hz
Broadband Noise Characteristics

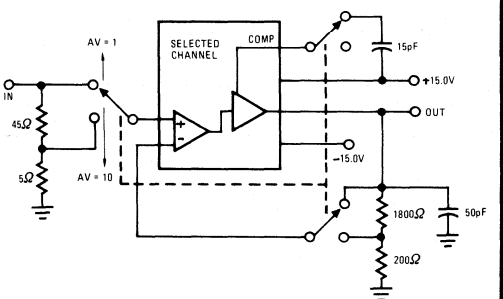
TRANSIENT RESPONSE



SLEW RATE AND SETTLING

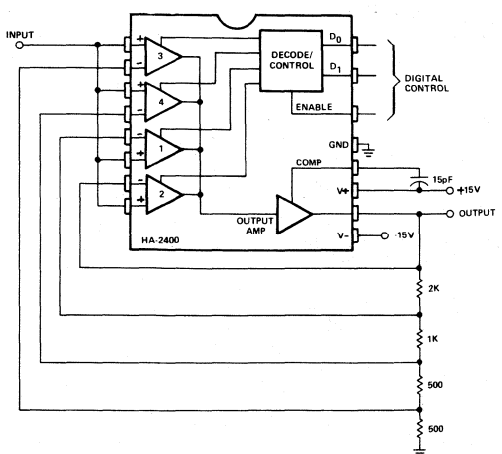


SLEW RATE AND TRANSIENT RESPONSE

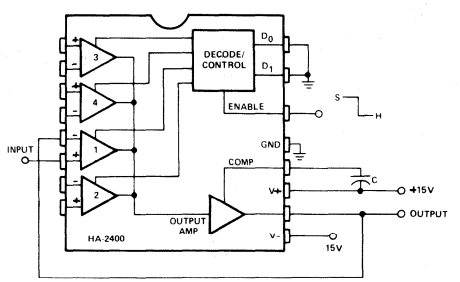


TYPICAL APPLICATIONS

AMPLIFIER, NON-INVERTING PROGRAMMABLE GAIN



SAMPLE AND HOLD



Sample charging rate = $\frac{I_1}{C}$ V/sec.

Hold drift rate = $\frac{I_2}{C}$ V/sec.

Switch pedistal error = $\frac{Q}{C}$ Volts

$I_1 \approx 150 \times 10^{-6}$ A

$I_2 \approx 200 \times 10^{-9}$ A @ +25°C

$\approx 600 \times 10^{-9}$ A @ -55°C

$\approx 100 \times 10^{-9}$ A @ +125°C

$Q \approx 2 \times 10^{-12}$ Coul.

FOR MORE EXAMPLES, SEE HARRIS APPLICATION NOTE 514

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HA-2500/02/05

Precision High Slew Rate Operational Amplifiers

2

FEATURES

- HIGH SLEW RATE — 30V/μS
- FAST SETTLING — 330ns
- WIDE POWER BANDWIDTH — 500kHz
- HIGH GAIN BANDWIDTH — 12MHz
- HIGH INPUT IMPEDANCE — 100MΩ
- LOW OFFSET CURRENT — 10nA
- INTERNALLY COMPENSATED

APPLICATIONS

- DATA ACQUISTION SYSTEMS
- R.F. AMPLIFIERS
- VIDEO AMPLIFIERS
- SIGNAL GENERATORS
- PULSE AMPLIFICATION

DESCRIPTION

HA-2500/2502/2505 comprise a series of monolithic operational amplifiers whose designs are optimized to deliver excellent slew rate, bandwidth, and settling time specifications. The outstanding dynamic features of this internally compensated device are complemented with low offset voltage and offset current.

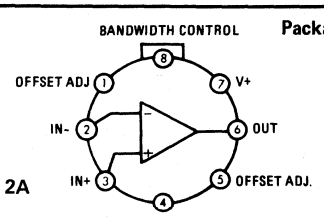
These dielectrically isolated amplifiers are ideally suited for applications such as data acquisition, R.F., video, and pulse conditioning circuits. Slew rate of ±25V/μs and 330ns (0.1%) settling time make these devices excellent components in fast, accurate data acquisition and pulse amplification designs. 12 MHz bandwidth and 500kHz power bandwidth make these devices well suited to R.F. and video applications. With 2mV typical offset voltage plus offset trim capability and 10nA offset current, HA-2500/2502/2505 are particularly useful components in signal conditioning designs.

The gain and offset voltage figures of the HA-2500 series are optimized by internal component value changes while the similar design of the HA-2510 series is maximized for slew rate.

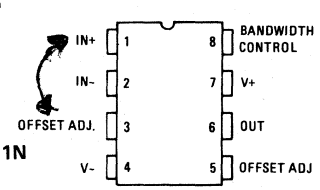
HA-2500/2502/2505 are available in metal can (TO-99) packages. HA-2500 and HA-2502 are specified over the -55°C to +125°C range. HA-2505 is specified from 0°C to +75°C.

PINOUT

TO-99 — Package Code 2A, 1N, LA

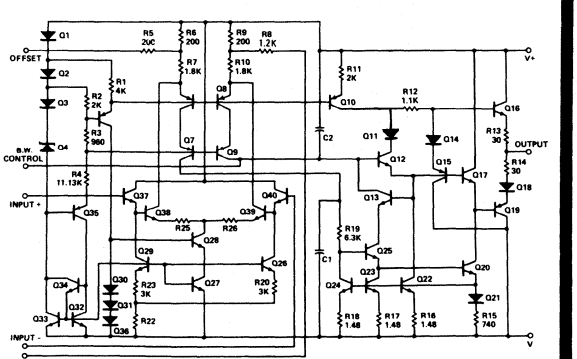


TOP VIEWS



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	40.0V	Operating Temperature Range –	HA-2500/HA-2502	$-55^oC \leq T_A \leq +125^oC$
Differential Input Voltage	±15.0V		HA-2505	$0^oC \leq T_A \leq +75^oC$
Peak Output Current	50mA	Storage Temperature Range		$-65^oC \leq T_A \leq +150^oC$
Internal Power Dissipation	300mW			

ELECTRICAL CHARACTERISTICS

V+ = +15V D.C., V- = -15V D.C.

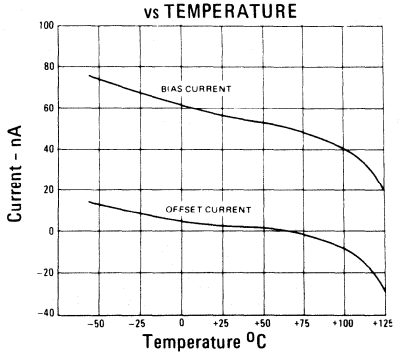
		HA-2500 -55°C to +125°C			HA-2502 -55°C to +125°C			HA-2505 0°C to +75°C			
		LIMITS			LIMITS			LIMITS			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS											
* Offset Voltage	+25°C Full		2	5 8		4	8 10		4	8 10	mV mV
Offset Voltage Average Drift	Full		20			20			20		µV/°C
* Bias Current	+25°C Full		100	200 400		125	250 500		125	250 500	nA nA
* Offset Current	+25°C Full		10	25 50		20	50 100		20	50 100	nA nA
Input Resistance (Note 10)	+25°C	25	50		20	50		20	50		MΩ
Common Mode Range	Full	±10.0			±10.0			±10.0			V
TRANSFER CHARACTERISTICS											
* Large Signal Voltage Gain (Note 1,4)	+25°C Full	20K 15K	30K		15K 10K	25K		15K 10K	25K		V/V V/V
* Common Mode Rejection Ratio (Note 2)	Full	80	90		74	90		74	90		dB
Gain Bandwidth Product (Note 3)	+25°C		12			12			12		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		±10.0	±12.0		V
* Output Current (Note 4)	+25°C	±10	±20		±10	±20		±10	±20		mA
Full Power Bandwidth (Note 4)	+25°C	350	500		300	500		300	500		kHz
TRANSIENT RESPONSE											
Rise Time (Notes 1, 5, 6 & 8)	+25°C		25	50		25	50		25	50	ns
Overshoot (Notes 1, 5, 7 & 8)	+25°C		25	40		25	50		25	50	%
* Slew Rate (Notes 1,5,8 & 12)	+25°C	±25	±30		±20	±30		±20	±30		V/µs
Settling Time to 0.1% (Notes 1,5,8 & 12)	+25°C		0.33			0.33			0.33		µs
POWER SUPPLY CHARACTERISTICS											
* Supply Current	+25°C		4	6		4	6		4	6	mA
* Power Supply Rejection Ratio (Note 9)	Full	80	90		74	90		74	90		dB

NOTES:
1. R_L = 2K
2. $V_{CM} = \pm 10V$
3. $A_V > 10$
4. $V_O = \pm 10.0V$
5. C_L = 50pF
6. $V_O = \pm 200mV$
7. $V_O \pm 200mV$
8. See transient response test circuits and waveforms page four.
9. $\Delta V = \pm 5.0V$
10. This parameter value is based on design calculations.
11. Full power bandwidth guaranteed based on slew rate measurement using $FPBW = S.R./2\pi V_{peak}$
12. $V_{OUT} = \pm 5V$

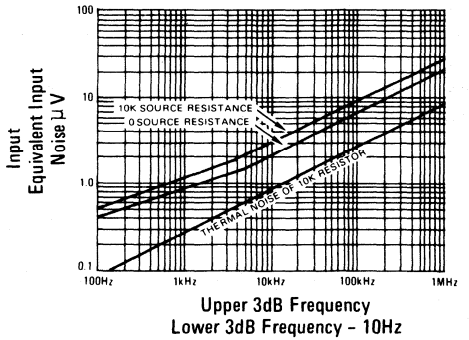
* 100% Tested For DASH 8

V+ = 15VDC, V- = 15VDC, T_A = 25°C UNLESS OTHERWISE STATED

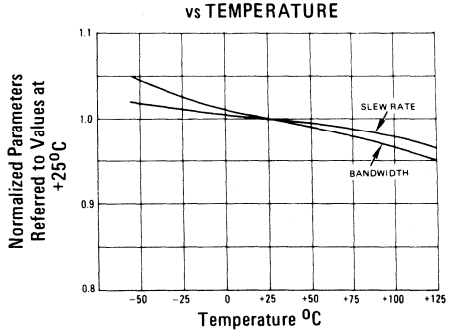
INPUT BIAS AND OFFSET CURRENT vs TEMPERATURE



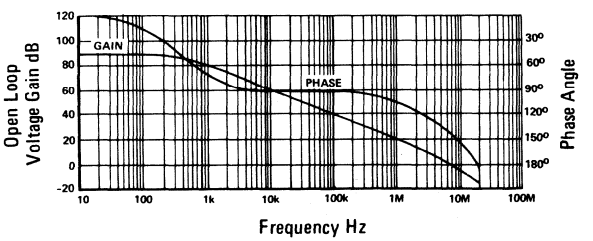
EQUIVALENT INPUT NOISE vs BANDWIDTH



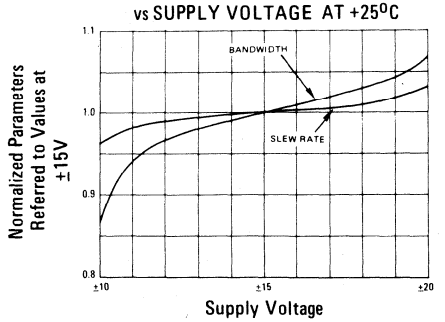
NORMALIZED AC PARAMETERS vs TEMPERATURE



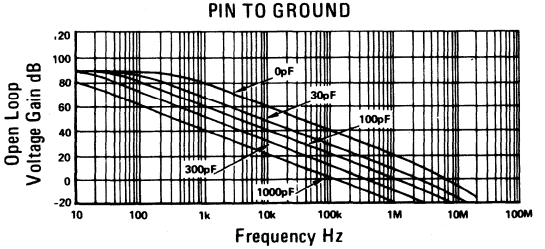
OPEN-LOOP FREQUENCY AND PHASE RESPONSE



NORMALIZED AC PARAMETERS vs SUPPLY VOLTAGE AT +25°C

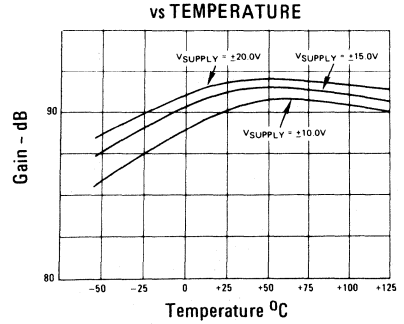


OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM BANDWIDTH CONTROL PIN TO GROUND

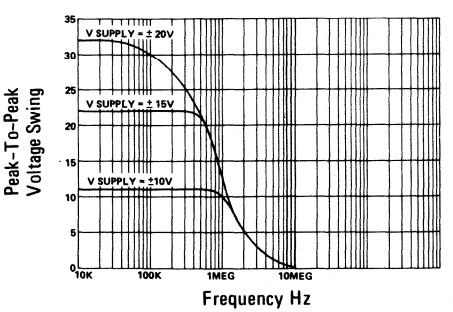


NOTE: External compensation components are not required for stability, but may be added to reduce bandwidth if desired.

OPEN LOOP VOLTAGE GAIN vs TEMPERATURE

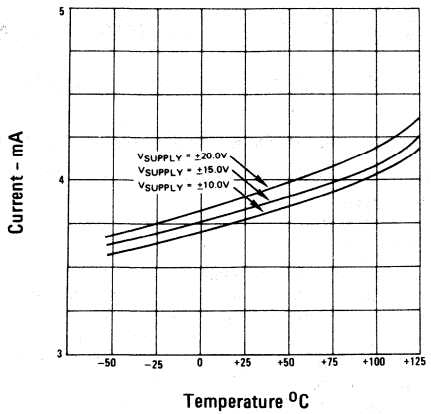


OUTPUT VOLTAGE SWING vs FREQUENCY AT +25°C

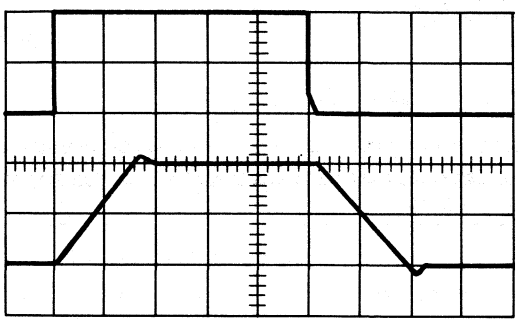


PERFORMANCE CURVES (continued)

POWER SUPPLY CURRENT vs TEMPERATURE



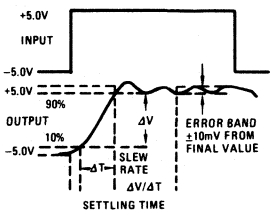
VOLTAGE FOLLOWER PULSE RESPONSE



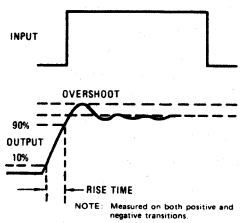
$R_L = 2K\Omega, C_L = 50pF$
Upper Trace: Input
Lower Trace: Output

Vertical = 5V/Div.
Horizontal = 200ns/Div.
$T_A = +25^oC, V_S = \pm 15.0V$

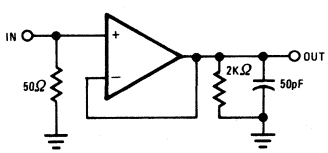
SLEW RATE AND SETTLING TIME



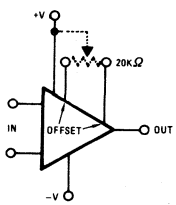
TRANSIENT RESPONSE



SLEW RATE AND TRANSIENT RESPONSE



SUGGESTED OFFSET ZERO ADJUST HOOK-UP



DEFINITIONS

INPUT OFFSET VOLTAGE – That voltage which must be applied between the input terminals through two equal resistances to force the output voltage to zero.

INPUT OFFSET CURRENT – The difference in the currents into the two input terminals when the output is at zero voltage.

INPUT BIAS CURRENT – The average of the currents flowing into the input terminals when the output is at zero voltage.

INPUT COMMON MODE VOLTAGE – The average referred to ground of the voltages at the two input terminals.

COMMON MODE RANGE – The range of voltages which is exceeded at either input terminal will cause the amplifier to cease operating.

TRANSIENT RESPONSE – The closed loop step function response of the amplifier under small signal conditions.

GAIN BANDWIDTH PRODUCT – The product of the gain and the bandwidth at a given gain.

SLEW RATE (Rating Limiting) – The rate at which the output will move between full scale stops, measured in terms of volts per unit time. This limit to an ideal step function response is due to the non-linear behavior in an amplifier due to its limited ability to produce large, rapid changes in output voltage (slewing) . . . restricting it to rates of change of voltage lower than might be predicted by observing the small signal frequency response.

SETTLING TIME – Time required for output waveform to remain within 0.1 percent of final value.

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HA-2507/2517/2527

Epoxy-Packaged, High Slew Rate Operational Amplifier Series

Preliminary

2

FEATURES

	HA-2507	HA-2517	HA-2527	
• High Slew Rate	30	60	120	V/μs
• Fast Settling	330	250	200	ns
• Wide Power Bandwidth	0.5	1.0	1.6	MHz
• High Gain Bandwidth	12	12	20	MHz
• High Input Impedance	50	100	100	MΩ

APPLICATIONS

- Pulse Amplification
- Video Amplifiers
- High Speed Test Equipment
- Medical Instrumentation
- Data Acquisition Systems
- Signal Generators

DESCRIPTION

HA-2507/2517/2527 operational amplifiers are a series of high-performance, epoxy-packaged monolithic IC's designed to deliver excellent slew rate, bandwidth and settling time specifications. Typical slew rate specifications for HA-2507, HA-2517 and HA-2527 are 30V/μsec, 60V/μsec and 120V/μsec respectively. Corresponding settling times (10V step to 0.1%) are 330ns, 250ns and 200ns for HA-2507, HA-2517 and HA-2527 respectively. Bandwidths range from 12MHz to 20MHz. This level of performance is achieved through the use of Harris's unique Dielectric Isolation processing techniques. HA-2507/2517/2527 are internally compensated; HA-2507 and HA-2517 are stable for closed loop gains (A_V) greater than or equal to unity. HA-2527 is stable for $A_V > 3$.

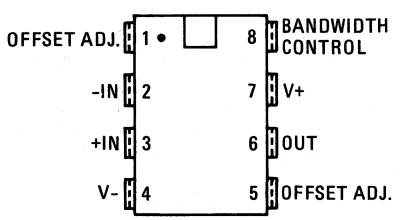
This series of op amps affords an economical means of designing high performance equipment for industrial and commercial use. Their slew rate and settling time performance makes them ideally suited for high speed D/A, A/D and pulse amplification designs. The wide bandwidth offered by these devices also makes them valuable components in RF and video applications. HA-2507/2517/2527 also deliver offset current, bias current and offset voltage specifications compatible with the requirements of accurate signal conditioning systems.

The HA-2507/2517/2527 are specified from 0°C to +75°C and are available in 8-lead epoxy DIP packages that have been extensively tested and qualified to deliver the high level of performance and reliability that are expected of Harris Semiconductor's operational amplifiers.

PINOUT

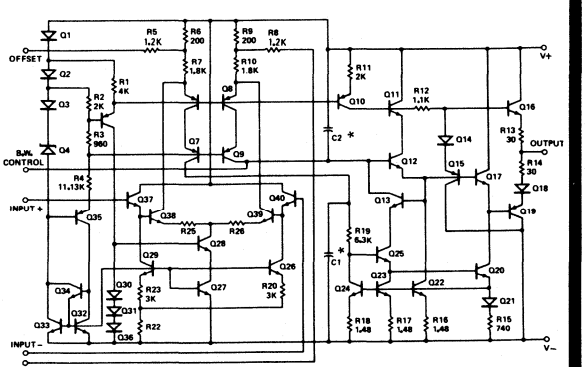
Package Code 3A

TOP VIEW



8 LEAD DIP EPOXY

SCHEMATIC



*VALUES OF C1 AND C2 VARY DEPENDING ON DEVICE TYPE.

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	40.0V	Operating Temperature Range – HA-2507/HA-2517	$0^oC \leq T_A \leq +75^oC$
Differential Input Voltage	±15.0V	HA-2527	
Peak Output Current	50mA	Storage Temperature Range	$-65^o \leq T_A \leq +150^oC$
Internal Power Dissipation	300mW		

ELECTRICAL CHARACTERISTICS

$V^+ = +15V$ D.C., $V^- = -15V$ D.C.

PARAMETER	TEMP.	HA-2507 0°C to +75°C LIMITS MIN.	HA-2507 TYP.	HA-2507 MAX.	HA-2517 0°C to +75°C LIMITS MIN.	HA-2517 TYP.	HA-2517 MAX.	HA-2527 0°C to +75°C LIMITS MIN.	HA-2527 TYP.	HA-2527 MAX.	UNITS
INPUT CHARACTERISTICS											
Offset Voltage	+25°C		5	8		5	10		5	10	mV
	Full			10			14			14	mV
Offset Voltage Average Drift	Full		25			30			30		µV/°C
Bias Current	+25°C		125	250		125	250		125	250	nA
	Full			500			500			500	nA
Offset Current	+25°C		20	50		20	50		20	50	nA
	Full			100			100			100	nA
Input Resistance (Note 10)	+25°C	20	50		40	100		40	100		MΩ
Common Mode Range	Full	±10.0			±10.0			±10.0			V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Note 1, 4)	+25°C	15K	25K		7.5K	15K		7.5K	15K		V/V
	Full	10K			5K			5K			V/V
Common Mode Rejection Ratio (Note 2)	Full	74	90		74	90		74	90		dB
Gain Bandwidth Product (Note 3)	+25°C		12			12			20		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		±10.0	±12.0		V
Output Current (Note 4)	+25°C	±10	±20		±10	±20		±10	±20		mA
Full Power Bandwidth (Note 4)	+25°C	220	500		450	1000		750	1600		kHz
TRANSIENT RESPONSE											
Rise Times (Notes 1, 5, 6 & 8)	+25°C		25	50		25	50		25	50	ns
Overshoot (Notes 1, 5, 7 & 8)	+25°C		25	50		25	50		25	50	%
Slew Rate (Notes 1, 5, 8 & 11)	+25°C	±15	± 30		±30	± 60		±60	±120		V/µs
Settling Time to 0.1% (Notes 1, 5, 8 & 11)	+25°C		0.33			0.25			0.20		µs
POWER SUPPLY CHARACTERISTICS											
Supply Current	+25°C		4	6		4	6		4	6	mA
Power Supply Rejection Ratio (Note 9)	Full	74	90		74	90		74	90		dB

NOTES:
1. $R_L = 2K$
2. $V_{CM} = \pm 10V$
3. $A_V > 10$
4. $V_O = +10.0V$
5. $C_L = 50pF$
6. $V_O = \pm 200mV$ for HA-2507 and HA-2517; $V_O = +200mV$ for HA-2527
7. $V_O = \pm 200mV$
8. For HA-2507 and HA-2517, $A_V = 1$ For HA-2527, $A_V = 3$
9. $\Delta V = +5.0V$
10. Guaranteed by design
11. $V_{OUT} = \pm 5V$ for 2507, 2517 & 2527

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HA-2510/2512/2515

High Slew Rate Operational Amplifiers

2

FEATURES

- HIGH SLEW RATE — 60V/μs
- FAST SETTLING — 250ns
- WIDE POWER BANDWIDTH — 1,000kHz
- HIGH GAIN BANDWIDTH — 12MHz
- HIGH INPUT IMPEDANCE — 100MΩ
- LOW OFFSET CURRENT — 10nA
- INTERNALLY COMPENSATED

APPLICATIONS

- DATA ACQUISITION SYSTEMS
- R.F. AMPLIFIERS
- VIDEO AMPLIFIERS
- SIGNAL GENERATORS
- PULSE AMPLIFICATION

DESCRIPTION

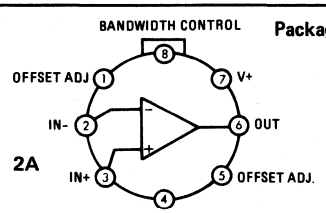
The HA-2510/2512/2515 are a series of high performance operational amplifiers which set the standards for maximum slew rate, highest accuracy and widest bandwidth for internally compensated monolithic devices. In addition to excellent dynamic characteristics, these dielectrically isolated amplifiers also offer low offset current and high input impedance.

The ±60V/ μs slew rate and 250ns (0.1%) settling time of these amplifiers is ideally suited for high speed D/A, A/D, and pulse amplification designs. HA-2510/2512/2515's superior 12MHz gain bandwidth and 1000kHz power bandwidth is extremely useful in R.F. and video applications. For accurate signal conditioning these amplifiers also provide 10nA offset current, coupled with 100MΩ input impedance, and offset trim capability.

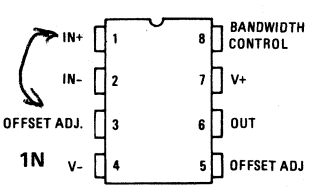
The HA-2510/2512 are available in metal can (TO-99) and 14-pin flat packages. HA-2510 and HA-2512 are specified from -55°C to +125°C. HA-2515 is specified over the 0°C to +75°C range, and is available in the TO-99 package.

PINOUT

TO-99 — **Package Code 2A, 1N, LA**

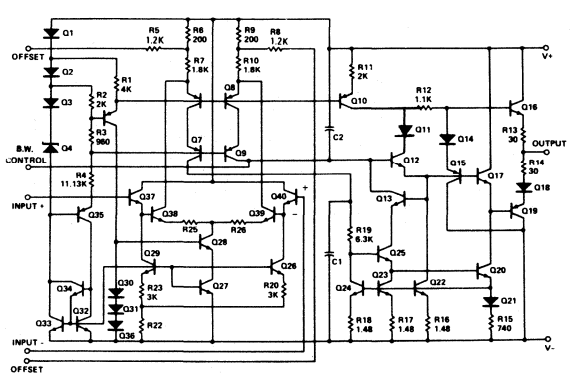


TOP VIEWS



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

SCHEMATIC



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	40.0V	Peak Output Current	50mA
Differential Input Voltage	±15.0V	Internal Power Dissipation	300mW
Operating Temperature Range		Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$
HA-2510/HA-2512	$-55^oC \leq T_A \leq +125^oC$		
HA-2515	$0^oC \leq T_A \leq +75^oC$		

ELECTRICAL CHARACTERISTICS

V+ = +15V D.C., V– = 15V D.C.

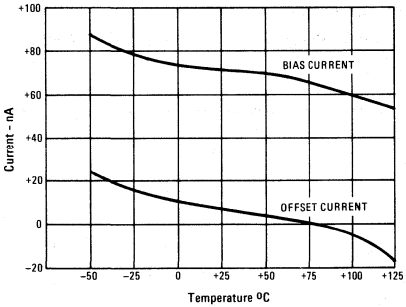
PARAMETER	TEMP.	HA-2510 -55°C to +125°C LIMITS MIN.	HA-2510 LIMITS TYP.	HA-2510 LIMITS MAX.	HA-2512 -55°C to +125°C LIMITS MIN.	HA-2512 LIMITS TYP.	HA-2512 LIMITS MAX.	HA-2515 0°C to +75°C LIMITS MIN.	HA-2515 LIMITS TYP.	HA-2515 LIMITS MAX.	UNITS
INPUT CHARACTERISTICS											
* Offset Voltage	+25°C		4	8		5	10		5	10	mV
	Full			11			14			14	mV
Offset Voltage Average Drift	Full		20			25			30		µV/°C
* Bias Current	+25°C		100	200		125	250		125	250	nA
	Full			400			500			500	nA
* Offset Current	+25°C		10	25		20	50		20	50	nA
	Full			50			100			100	nA
Input Resistance (Note10)	+25°C	50	100		40	100		40	100		MΩ
Common Mode Range	Full	±10.0			±10.0			±10.0			V
TRANSFER CHARACTERISTICS											
* Large Signal Voltage Gain (Note 1,4)	+25°C	10K	15K		7.5K	15K		7.5K	15K		V/V
	Full	7.5K			5K			5K			V/V
* Common Mode Rejection Ratio (Note 2)	Full	80	90		74	90		74	90		dB
Gain Bandwidth Product (Note 3)	+25°C		12			12			12		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		±10.0	±12.0		V
* Output Current (Note 4)	+25°C	±10	±20		±10	±20		±10	±20		mA
Full Power Bandwidth (Note 4, 11)	+25°C	750	1000		600	1000		600	1000		kHz
TRANSIENT RESPONSE											
Rise Time (Notes 1, 5, 6 & 8)	+25°C		25	50		25	50		25	50	ns
Overshoot (Notes 1, 5, 7 & 8)	+25°C		25	40		25	50		25	50	%
* Slew Rate (Notes 1, 5, 8 & 12)	+25°C	±50	±65		±40	±60		±40	±60		V/µs
Settling Time (Notes 1, 5, 8 & 12)	+25°C		0.25			0.25			0.25		µs
POWER SUPPLY CHARACTERISTICS											
* Supply Current	+25°C		4	6		4	6		4	6	mA
* Power Supply Rejection Ratio (Note 9)	Full	80	90		74	90		74	90		dB

NOTES:
1. R_L = 2K
2. $V_{CM} = \pm 10V$
3. $A_V > 10$
4. $V_O = \pm 10.0V$
5. C_L = 50pF
6. $V_O = \pm 200mV$
7. $V_O = \pm 200mV$
8. See transient response test circuits and waveforms
9. $\Delta V = \pm 5.0V$
10. This parameter value is based upon design calculations.
11. Full power bandwidth guaranteed based upon slew rate measurement FPBW = S.R./2πV_{peak}.
12. $V_{OUT} = \pm 5V$

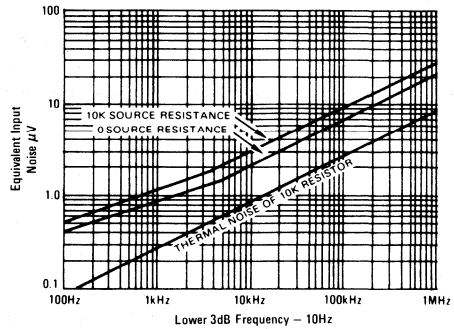
*100% Tested For DASH 8

V+ = 15VDC, T_A = 25°C UNLESS OTHERWISE STATED.

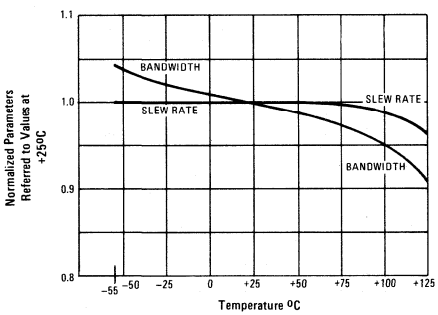
INPUT BIAS AND OFFSET CURRENT vs. TEMPERATURE



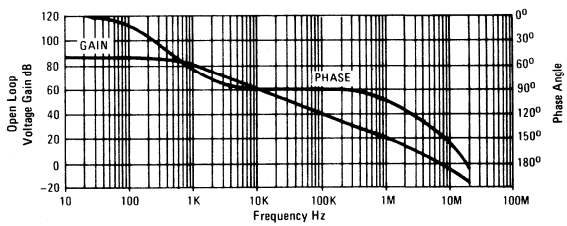
EQUIVALENT INPUT NOISE vs. BANDWIDTH



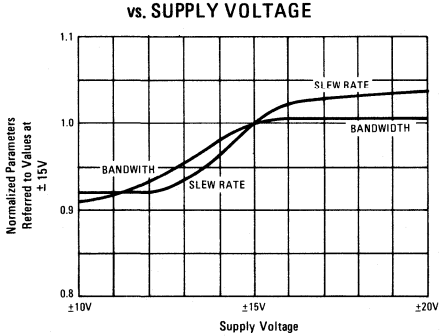
NORMALIZED AC PARAMETERS vs. TEMPERATURE



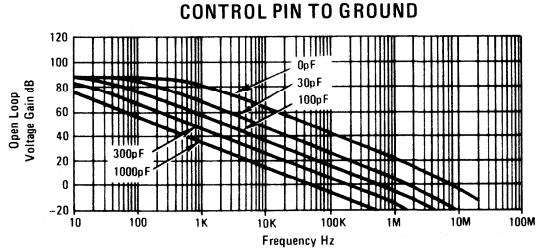
OPEN LOOP FREQUENCY AND PHASE RESPONSE



NORMALIZED AC PARAMETERS vs. SUPPLY VOLTAGE

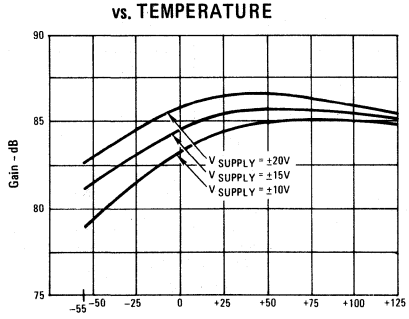


OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM BANDWIDTH CONTROL PIN TO GROUND

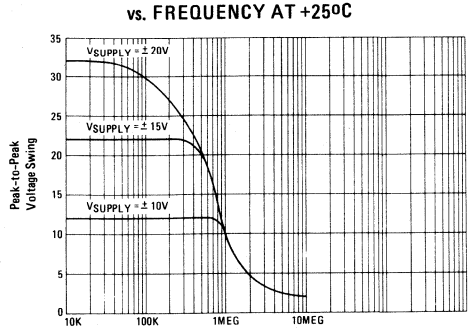


NOTE: External compensation components are not required for stability, but may be added to reduce bandwidth if desired.

OPEN LOOP VOLTAGE GAIN vs. TEMPERATURE

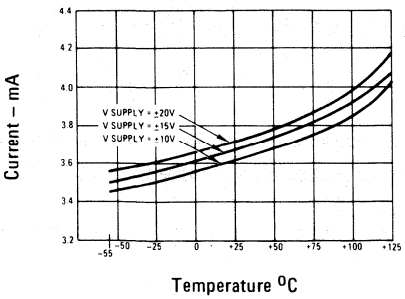


OUTPUT VOLTAGE SWING vs. FREQUENCY AT +25°C

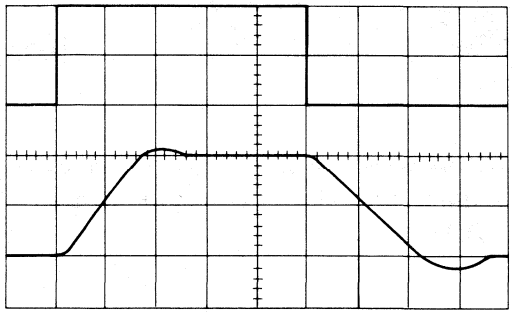


PERFORMANCE CURVES (continued)

POWER SUPPLY CURRENT
VS
TEMPERATURE



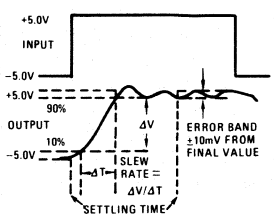
VOLTAGE FOLLOWER PULSE RESPONSE



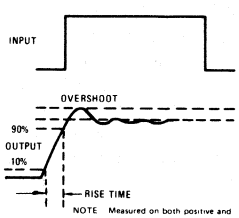
R_L = 2K Ω , C_L = 50pF
Upper Trace: Input
Lower Trace: Output

Vertical = 5V/Div.
Horizontal = 100n/Div.
T_A = +25°C, V_S = ±15.0V

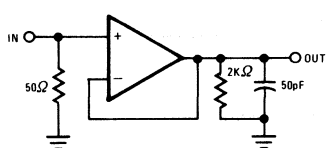
SLEW RATE AND
SETTLING TIME



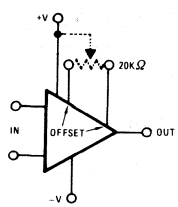
TRANSIENT RESPONSE



SLEW RATE AND
TRANSIENT RESPONSE



SUGGESTED
OFFSET ZERO
ADJUST HOOK-UP



DEFINITIONS

INPUT OFFSET VOLTAGE – That voltage which must be applied between the input terminals through two equal resistances to force the output voltage to zero.

INPUT OFFSET CURRENT – The difference in the currents into the two input terminals when the output is at zero voltage.

INPUT BIAS CURRENT – The average of the currents flowing into the input terminals when the output is at zero voltage.

INPUT COMMON MODE VOLTAGE – The average referred to ground of the voltages at the two input terminals.

COMMON MODE RANGE – The range of voltages which is exceeded at either input terminal will cause the amplifier to cease operating.

COMMON MODE REJECTION RATIO – The ratio of a specified range of input common mode voltage to the peak-to-peak change in input offset voltage over this range.

OUTPUT VOLTAGE SWING – The peak symmetrical output voltage swing, referred to ground, that can be obtained without clipping.

INPUT RESISTANCE – The ratio of the change in input voltage to the change in input current.

OUTPUT RESISTANCE – The ratio of the change in output voltage to the change in output current.

VOLTAGE GAIN – The ratio of the change in output voltage to the change in input voltage producing it

UNITY GAIN BANDWIDTH – The frequency at which the voltage gain of the amplifier is unity.

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HA-2520/22/25

Uncompensated High Slew Rate Operational Amplifiers

2

FEATURES

- HIGH SLEW RATE — 120V/μs
- FAST SETTLING — 200ns
- WIDE POWER BANDWIDTH — 2,000kHz
- HIGH GAIN BANDWIDTH — 20MHz
- HIGH INPUT IMPEDANCE — 100MΩ
- LOW OFFSET CURRENT — 10nA

APPLICATIONS

- DATA ACQUISITION SYSTEMS
- R.F. AMPLIFIERS
- VIDEO AMPLIFIERS
- SIGNAL GENERATORS
- PULSE AMPLIFICATION

DESCRIPTION

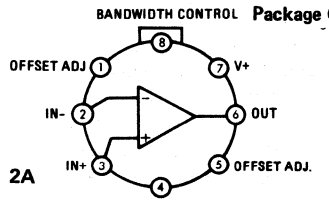
HA-2520/2522/2525 comprise a series of monolithic operational amplifiers delivering an unsurpassed combination of specifications for slew rate, bandwidth and settling time. These dielectrically isolated amplifiers are controlled at closed loop gains greater than 3 without external compensation. In additon, these high performance components also provide low offset current and high input impedance.

120V/μs slew rate and 200ns (0.1%) settling time of these amplifiers make them ideal components for pulse amplification and data acquisition designs. These devices are valuable components for R.F. and video circuitry requiring up to 20MHz gain bandwidth and 2MHz power bandwidth. For accurate signal conditioning designs the HA-2520/2522/2525's superior dynamic specifications are complimented by 10nA offset current, 100MΩ input impedance and offset trim capability.

The HA-2520/2522 are available in metal can (TO-99) and 14-pin flat packages. HA-2520 and HA-2522 are specified over -55°C to +125°C range. HA-2525 is specified from 0°C to +75°C, and is available in the TO-99 package.

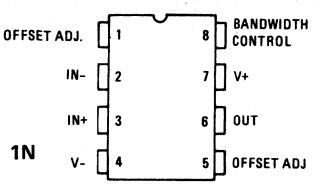
PINOUT

TO-99 — **Package Code 2A, 1N, LA**



2A

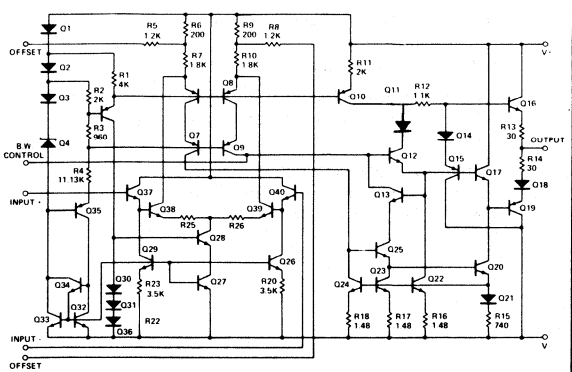
TOP VIEWS



1N

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	40.0V	Peak Output Current	50mA
Differential Input Voltage	±15.0V	Internal Power Dissipation	300mW
Operating Temperature Range			
HA-2520/2522	$-55^oC \leq T_A \leq +125^oC$	Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$
HA-2525	$0^oC \leq T_A \leq +75^oC$		

ELECTRICAL CHARACTERISTICS

V+ = +15V D.C., V- = -15V D.C.

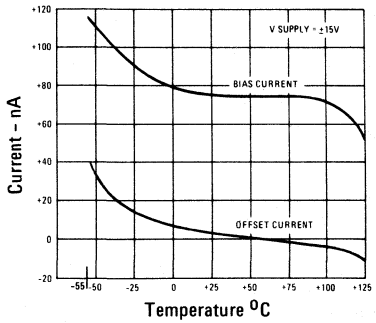
PARAMETER	TEMP.	HA-2520 -55°C to +125°C LIMITS MIN.	HA-2520 TYP.	HA-2520 MAX.	HA-2522 -55°C to +125°C LIMITS MIN.	HA-2522 TYP.	HA-2522 MAX.	HA-2525 0°C to +75°C LIMITS MIN.	HA-2525 TYP.	HA-2525 MAX.	UNITS
INPUT CHARACTERISTICS											
* Offset Voltage	+25°C Full		4	8 11		5	10 14		5	10 14	mV mV
Offset Voltage Average Drift	Full		20			25			30		µV/°C
* Bias Current	+25°C Full		100	200 400		125	250 500		125	250 500	nA nA
* Offset Current	+25°C Full		10	25 50		20	50 100		20	50 100	nA nA
Input Resistance (Note 9)	+25°C	50	100		40	100		40	100		MΩ
Common Mode Range	Full	±10.0			±10.0			±10.0			V
TRANSFER CHARACTERISTICS											
* Large Signal Voltage Gain (Note 1,4)	+25°C Full	10K 7.5K	15K		7.5K 5K	15K		7.5K 5K	15K		V/V V/V
* Common Mode Rejection Ratio (Note 2)	Full	80	90		74	90		74	90		dB
Gain Bandwidth Product (Note 3)	+25°C	10	20		10	20		10	20		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		±10.0	±12.0		V
* Output Current (Note 4)	+25°C	±10	±20		±10	±20		±10	±20		mA
Full Power Bandwidth (Note 4, 10)	+25°C	1500	2000		1200	1600		1200	1600		kHz
TRANSIENT RESPONSE (A_V = +3)											
Rise Time (Notes 1, 5, 6 & 8)	+25°C		25	50		25	50		25	50	ns
Overshoot (Notes 1, 5, 6 & 8)	+25°C		25	40		25	50		25	50	%
* Slew Rate (Notes 1, 5, 8 & 11)	+25°C	±100	±120		±80	±120		±80	±120		V/µs
Settling Time (Notes 1, 5, 8 & 11)	+25°C		0.20			0.20			0.20		µs
POWER SUPPLY CHARACTERISTICS											
* Supply Current	+25°C		4	6		4	6		4	6	mA
* Power Supply Rejection Ratio (Note 7)	Full	80	90		74	90		74	90		dB

NOTES:
1. R_L = 2K
2. V_{CM} = ±10V
3. $A_V > 10$
4. V_O = ±10.0V
5. C_L = 50pF
6. V_O = ±200mV
7. ΔV = ±5.0V
8. See transient response test circuits and waveforms
9. This parameter value is based upon design calculations.
10. Full power bandwidth guaranteed based upon slew rate measurement FPBW = S.R./$2\pi V_{peak}$.
11. V_{OUT} = ±5V

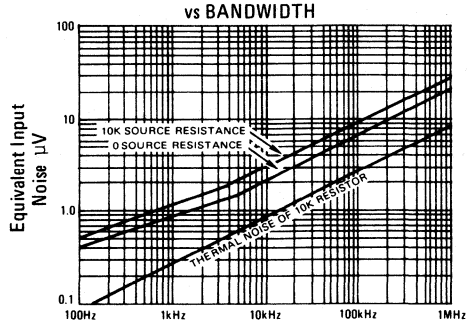
*100% Tested For DASH 8

V+ = 15VDC, V- = 15VDC, T_A = 25°C UNLESS OTHERWISE STATED

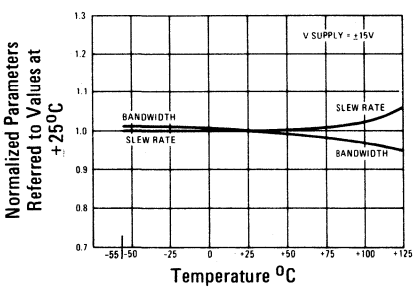
INPUT BIAS AND OFFSET CURRENT vs TEMPERATURE



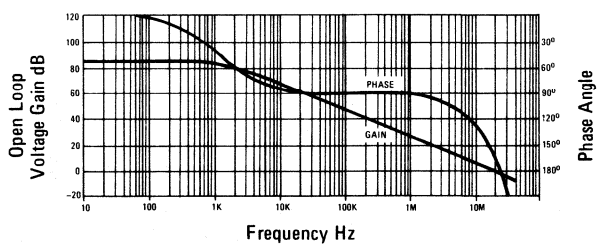
EQUIVALENT INPUT NOISE vs BANDWIDTH



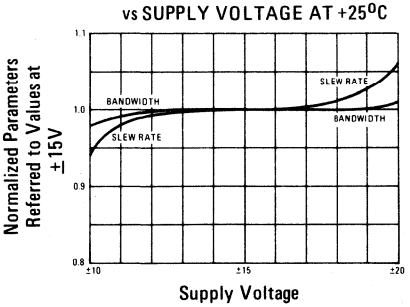
NORMALIZED AC PARAMETERS vs TEMPERATURE



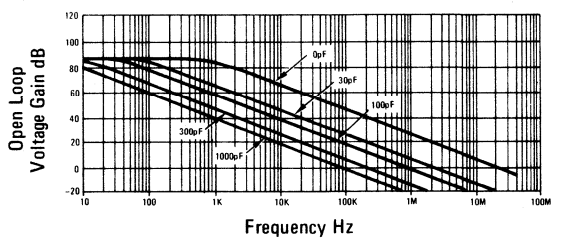
OPEN-LOOP FREQUENCY AND PHASE RESPONSE



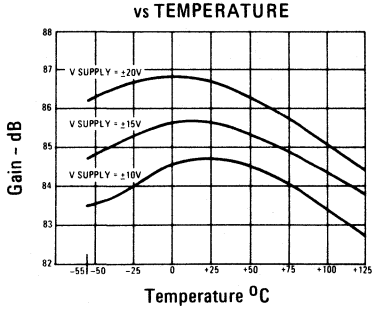
NORMALIZED AC PARAMETERS vs SUPPLY VOLTAGE AT +25°C



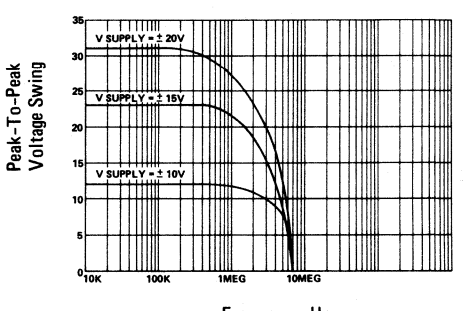
OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM BANDWIDTH CONTROL PIN TO GROUND



OPEN LOOP VOLTAGE GAIN vs TEMPERATURE

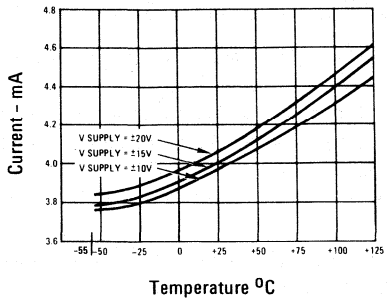


OUTPUT VOLTAGE SWING vs FREQUENCY AT +25°C

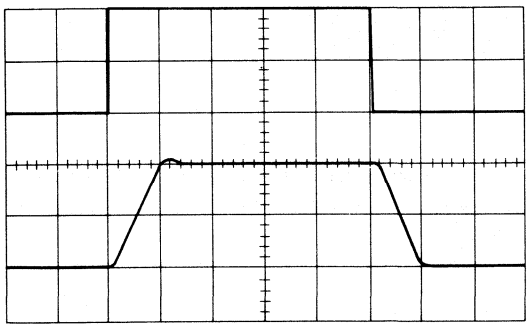


PERFORMANCE CURVES (continued)

POWER SUPPLY CURRENT vs TEMPERATURE



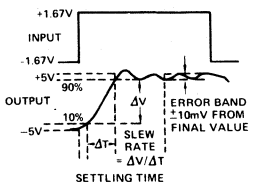
VOLTAGE FOLLOWER PULSE RESPONSE



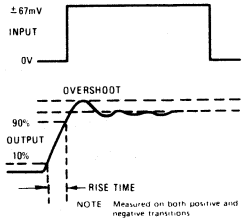
$R_L = 2K\Omega$, $C_L = 50pF$
Upper Trace: Input; 1.67V/Div.
Lower Trace: Output; 5V/Div.

Horizontal = 100ns/Div.
$T_A = +25^oC$, $V_S = \pm 15V$

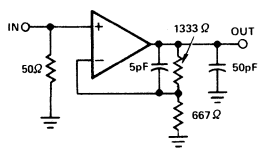
SLEW RATE AND SETTLING TIME



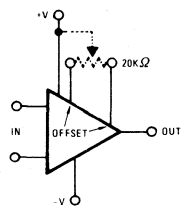
TRANSIENT RESPONSE



SLEW RATE AND TRANSIENT RESPONSE

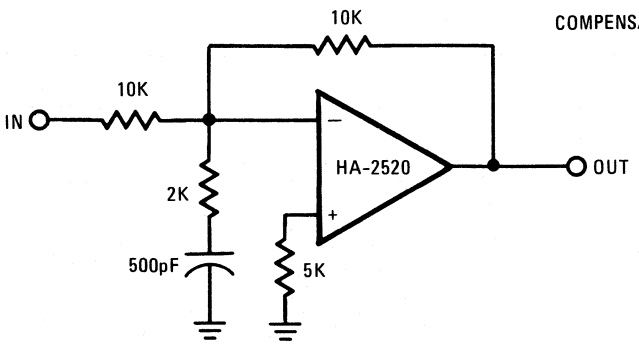


SUGGESTED OFFSET ZERO ADJUST HOOK-UP



TYPICAL APPLICATIONS

COMPENSATION CIRCUIT FOR INVERTING UNITY GAIN



Slew Rate	≈	120V/μs
Bandwidth	≈	10MHz
Settling Time	≈	500ns

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HA-2530/2535

High Slew Rate, Wideband Inverting Amplifier

2

FEATURES

- HIGH SLEW RATE ±320V/μs
- FAST SETTLING TIME 550ns
- WIDE POWER BANDWIDTH 5MHz
- HIGH GAIN BANDWIDTH PRODUCT 70MHz
- LOW OFFSET VOLTAGE 0.8mV
- LOW POWER SUPPLY CURRENT 3.5mA

APPLICATIONS

- PULSE AMPLIFICATION
- SIGNAL CONDITIONING
- SIGNAL GENERATORS
- COAXIAL CABLE DRIVERS
- INTEGRATORS

DESCRIPTION

HA-2530 and HA-2535 are monolithic high speed inverting amplifiers which deliver superior slew rate, bandwidth, and accuracy specifications compared to any other amplifier in its class. Designs of these dielectrically isolated amplifiers utilize the feed forward amplifier technique to produce excellent dynamic and DC specifications coupled with low power consumption. These devices require no external compensation at closed loop gains greater than 10.

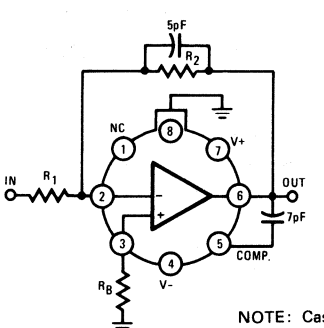
These amplifiers are excellent components for pulse circuits, data acquisition designs, and high speed integrators that can take advantage of the ±320V/μs slew rate and 550ns (0.1%) settling time. 70MHz gain bandwidth product, 5MHz power bandwidth coupled with 0.8mV offset voltage and ±50mA typical output current levels make these amplifiers ideally suited for signal conditioning, signal generation, and coaxial driver applications.

The HA-2530 and HA-2535 are available in metal can (TO-99) packages. HA-2530 is specified over the -55°C to +125°C range while HA-2535 is specified from 0°C to +75°C.

PINOUT

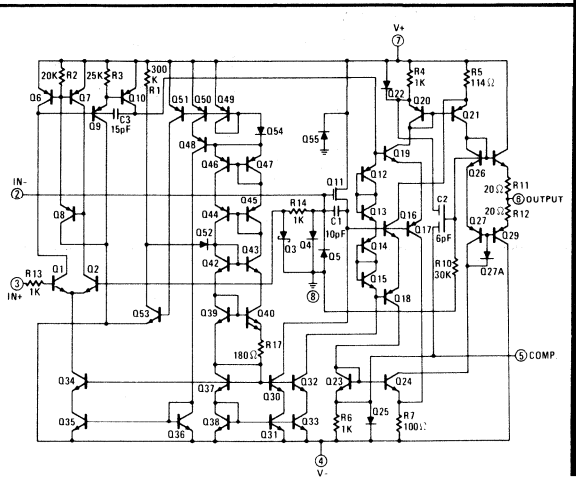
TO-99 **Package Code 2A**

TOP VIEW



NOTE: Case tied to V-

SCHEMATIC



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	40V	Internal Power Dissipation (Note 1)	550mW	
		Operating Temperature Range	$-55^{o}C \leq T_A \leq +125^{o}C$	(HA-2530)
Peak Output Current	±100mA		$0^{o}C \leq T_A \leq +75^{o}C$	(HA-2535)
		Storage Temperature Range	$-65^{o}C \leq T_A \leq +150^{o}C$	

ELECTRICAL CHARACTERISTICS

Test Conditions: $V_{Supply} = \pm 15.0V$ Unless Otherwise Specified.

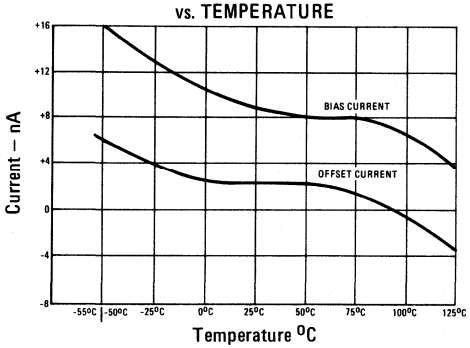
		HA-2530 -55°C to +125°C			HA-2535 0°C to +75°C			
		LIMITS			LIMITS			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS								
* Offset Voltage	+25°C		0.8			0.8		mV
	Full			3			5	mV
Average Offset Voltage Drift	Full		5			5		µV/°C
* Bias Current	+25°C		15			15		nA
	Full			100			200	nA
* Offset Current	+25°C		5			5		nA
	Full			20			20	nA
Input Resistance	+25°C		2			2		MΩ
Input Capacitance	+25°C		10			10		pF
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Notes 2,5)	+25°C		$2X10^6$			$2X10^6$		V/V
*	Full	10^5			10^5			V/V
* Common-Mode Rejection Ratio (Note 3)	Full	86	100		80	100		dB
Gain Bandwidth Product (Note 4)	+25°C		70			70		MHz
OUTPUT CHARACTERISTICS								
* Output Voltage Swing (Note 2)	Full	±10	±12		±10	±12		V
* Output Current (Note 5)	+25°C	±25	±50		±25	±50		mA
Full Power Bandwidth (Note 5)	+25°C	4	5		4	5		MHz
TRANSIENT RESPONSE (NOTES 6&7)								
* Rise Time	+25°C		20	40		20	40	ns
* Overshoot	+25°C		30	45		30	50	%
* Slew Rate	+25°C	±280	±320		±250	±320		V/µs
Settling Time	+25°C		500			500		ns
POWER SUPPLY CHARACTERISTICS								
* Supply Current	+25°C		3.5	6		3.5	6	mA
* Power Supply Rejection Ratio (Note 8)	Full	86	100		80	100		dB

NOTES:
1. Derate at 5.5mW/°C for Operation at Ambient Temperature Above 75°C.
2. $R_L = 2K$
3. $V_{CM} = \pm 5.0V$
4. $A_V > 10$
5. $V_O = \pm 10V$
6. $C_L = 50pF$
7. See Transient Response Test Circuit and Wave Forms
8. $\Delta V = \pm 5.0V$

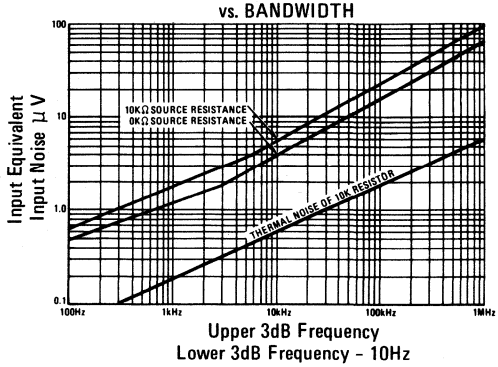
*100% Tested For DASH 8

V+ = 15VDC, V- = 15VDC, T_A = 25°C UNLESS OTHERWISE STATED

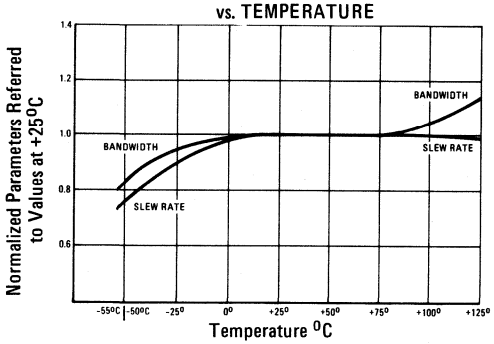
INPUT BIAS AND OFFSET CURRENT vs. TEMPERATURE



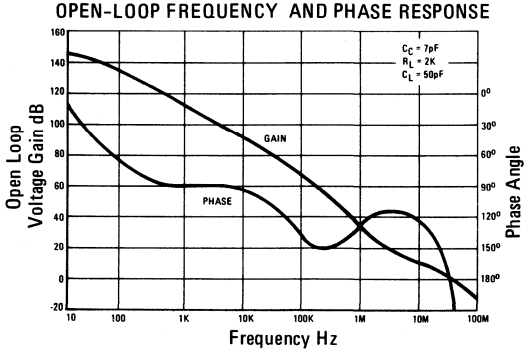
EQUIVALENT INPUT NOISE vs. BANDWIDTH



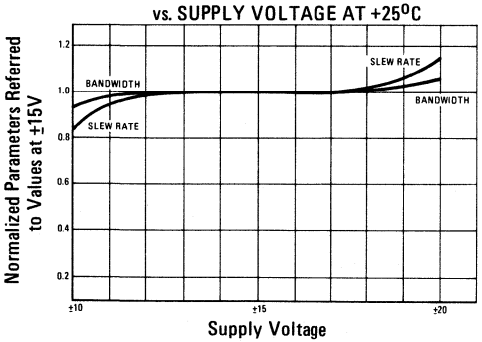
NORMALIZED AC PARAMETERS vs. TEMPERATURE



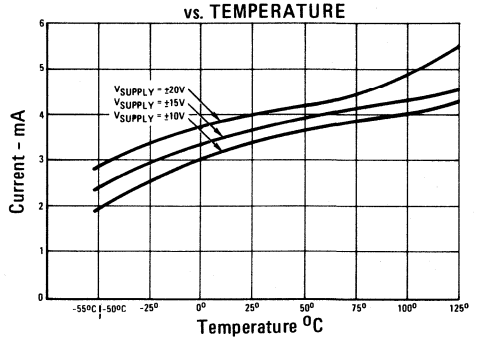
OPEN-LOOP FREQUENCY AND PHASE RESPONSE



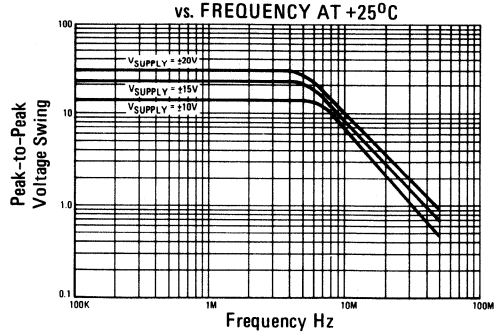
NORMALIZED AC PARAMETERS vs. SUPPLY VOLTAGE AT +25°C



POWER SUPPLY CURRENT vs. TEMPERATURE

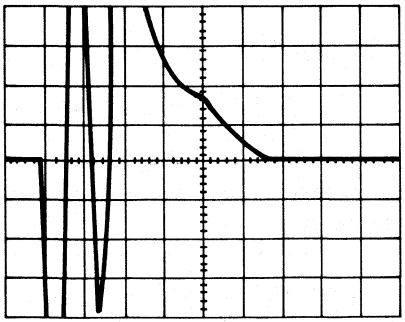


OUTPUT VOLTAGE SWING vs. FREQUENCY AT +25°C



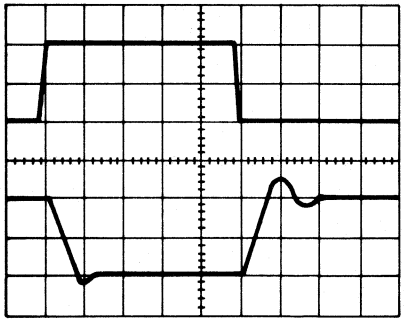
PERFORMANCE CURVES (continued)

SETTLING TIME MEASUREMENT *1



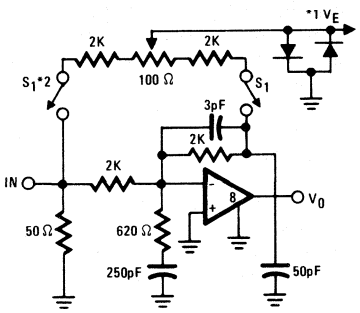
VERTICAL = 5mV/DIV.
HORIZONTAL = 100ns/DIV.
T_A = +25°C, V_S = ±15V

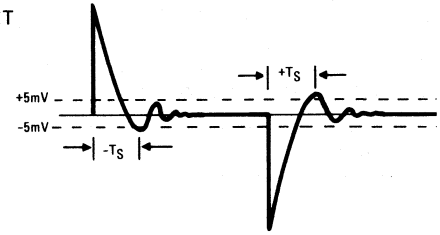
UNITY GAIN PULSE RESPONSE



UPPER TRACE: INPUT VERTICAL = 5V/DIV.
LOWER TRACE: OUTPUT HORIZONTAL = 50ns/DIV.
T_A = +25°C, V_S = ±15V

SLEW RATE/SETTLING TIME/TRANSIENT RESPONSE TEST CIRCUIT

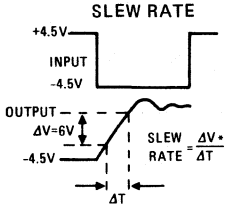




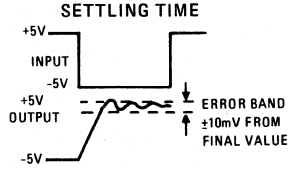
*1 Settling time (T_S) is measured using a high speed high recovery oscilloscope to display the error voltage V_E. When V_E is within ±5mV of final value the output V_O will be within ±10mV (0.1%).

*2 S_1 closed for settling time.

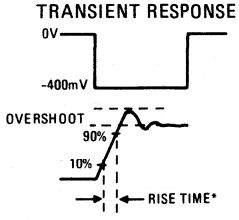
SLEW RATE



SETTLING TIME

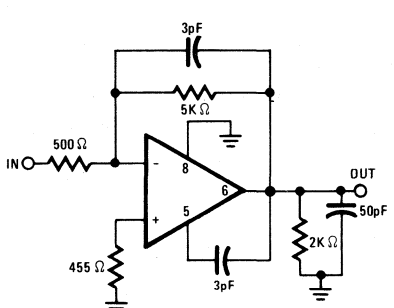


TRANSIENT RESPONSE



* MEASURED ON BOTH POSITIVE AND NEGATIVE EXCURSIONS.

5MHz VIDEO AMPLIFIER (A_V = 10)



HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HA-2600/2602/2605

Wide Band, High Impedance Operational Amplifier

2

FEATURES

- WIDE BANDWIDTH 12MHz
- HIGH INPUT IMPEDANCE 500MΩ
- LOW INPUT BIAS CURRENT 1nA
- LOW INPUT OFFSET CURRENT 1nA
- LOW INPUT OFFSET VOLTAGE 0.5mV
- HIGH GAIN 150K V/V
- HIGH SLEW RATE 7V/μs
- OUTPUT SHORT CIRCUIT PROTECTION

APPLICATIONS

- VIDEO AMPLIFIER
- PULSE AMPLIFIER
- AUDIO AMPLIFIERS AND FILTERS
- HIGH-Q ACTIVE FILTERS
- HIGH-SPEED COMPARATORS
- LOW DISTORTION OSCILLATORS

DESCRIPTION

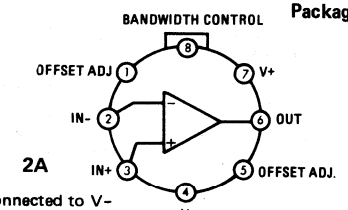
HA-2600/2602/2605 are internally compensated bipolar operational amplifiers that feature very high input impedance (500 MΩ, HA-2600) coupled with wideband AC performance. The high resistance of the input stage is complemented by low offset voltage (0.5mV, HA-2600) and low bias and offset current (1nA, HA-2600) to facilitate accurate signal processing. Input offset can be reduced further by means of an external nulling potentiometer. 12MHz unity gain-bandwidth product, 7V/μs slew rate and 150,000V/V open-loop gain enables HA-2600/2602/2605 to perform high-gain amplification of fast, wideband signals. These dynamic characterisitics, coupled with fast settling times, make these amplifiers ideally suited to pulse amplification designs as well as high frequency (e.g. video) applications. The frequency response of the amplifier can be tailored to exact design requirements by means of an external bandwidth control capacitor.

In addition to its application in pulse and video amplifier designs, HA-2600/2602/2605 is particularly suited to other high performance designs such as high-gain low distortion audio amplifiers, high-Q and wideband active filters and high-speed comparators.

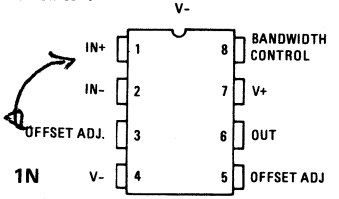
HA-2600 and HA-2602 are guaranteed over -55°C to +125°C. HA-2605 is specified from 0°C to +75°C. All devices are available in TO-99 cans, and HA-2600/2602 are available in 10 lead flat packages.

PINOUT

TO-99 Package Code 2A, 1N, LA

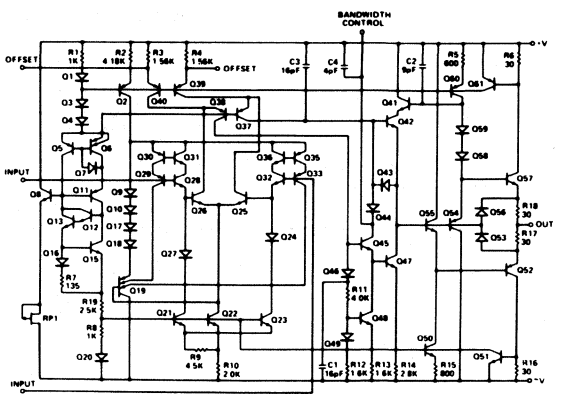


TOP VIEWS



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	45.0V
Differential Input Voltage	±12.0V
Peak Output Current	Full Short Circuit Protection
Internal Power Dissipation	300mW
Operating Temperature Range – HA-2600/HA-2602	$-55^oC \leq T_A \leq +125^oC$
HA-2605	$0^o \leq T_A \leq +75^oC$
Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$

ELECTRICAL CHARACTERISTICS V+ = +15VDC, V- = -15VDC

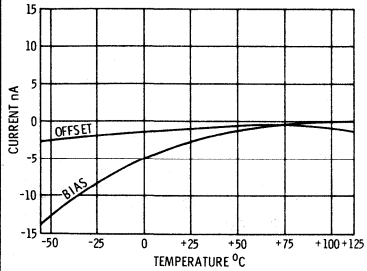
		HA-2600 −55°C to +125°C			HA-2602 −55°C to +125°C			HA-2605 0°C to +75°C			
		LIMITS			LIMITS			LIMITS			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS											
* Offset Voltage	+25°C		0.5	4		3	5		3	5	mV
	Full		2	6			7			7	mV
Offset Voltage Average Drift	Full		5								µV/°C
* Bias Current	+25°C		1	10		15	25		5	25	nA
	Full		10	30			60			40	nA
* Offset Current	+25°C		1	10		5	25		5	25	nA
	Full		5	30			60			40	nA
Input Resistance (Note 10)	+25°C	100	500		40	300		40	300		MΩ
Common Mode Range	Full	±11.0			±11.0			±11.0			V
TRANSFER CHARACTERISTICS											
* Large Signal Voltage Gain (Notes 1, 4)	+25°C	100K	150K		80K	150K		80K	150K		V/V
	Full	70K			60K			70K			V/V
* Common Mode Rejection Ratio (Note 2)	Full	80	100		74	100		74	100		dB
Unity Gain Bandwidth (Note 3)	+25°C		12			12			12		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		±10.0	±12.0		V
* Output Current (Note 4)	+25°C	±15	±22		±10	±18		±10	±18		mA
Full Power Bandwidth (Note 4 &11)	+25°C	50	75		50	75		50	75		kHz
TRANSIENT RESPONSE											
Rise Time (Notes 1, 5, 6 & 8)	+25°C		30	60		30	60		30	60	ns
Overshoot (Notes 1, 5, 7 & 8)	+25°C		25	40		25	40		25	40	%
* Slew Rate (Notes 1, 5, 8 & 12)	+25°C	±4	±7		±4	±7		±4	±7		V/µs
Settling Time (Notes 1, 5, 8 & 12)	+25°C		1.5			1.5			1.5		µs
POWER SUPPLY CHARACTERISTICS											
* Supply Current	+25°C		3.0	3.7		3.0	4.0		3.0	4.0	mA
* Power Supply Rejection Ratio (Note 9)	Full	80	90		74	90		74	90		dB

TEST CONDITIONS

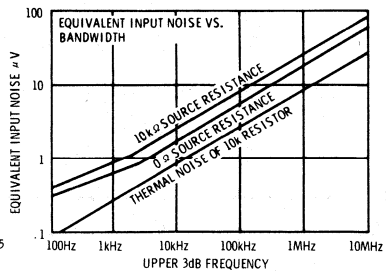
NOTES:
1. R_L = 2K
2. $V_{CM} = \pm 10V$
3. V_O <90mV
4. $V_O = \pm 10V$
5. C_L = 100pF
6. $V_O = \pm 200mV$
7. $V_O = \pm 200mV$
8. See Transient response test circuits and waveforms
9. $\Delta VS = \pm 5V$
10. This parameter value guaranteed by design calculations.
11. Full power bandwidth guaranteed by slew rate measurement. FPBW = S.R./2π V_{peak}.
12. $V_{OUT} = \pm 5V$

*100% Tested For DASH 8

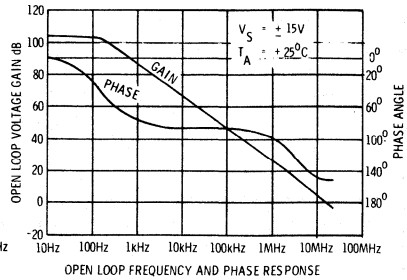
V+ = 15VDC, V- = 15VDC, T_A = 25°C UNLESS OTHERWISE STATED.



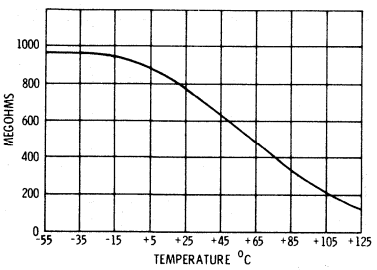
INPUT BIAS CURRENT AND OFFSET CURRENT
AS A FUNCTION OF TEMPERATURE



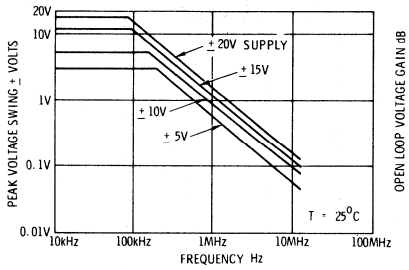
UPPER 3dB FREQUENCY
LOWER 3dB FREQUENCY - 10Hz
BROADBAND NOISE CHARACTERISTICS



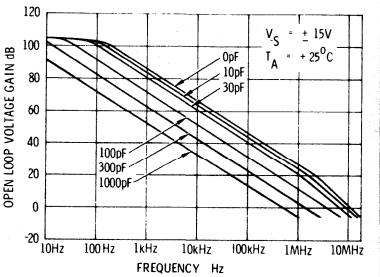
OPEN LOOP FREQUENCY AND PHASE RESPONSE



INPUT IMPEDANCE VS. TEMPERATURE, 100Hz

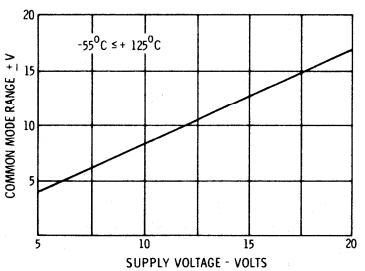


OUTPUT VOLTAGE SWING VS. FREQUENCY

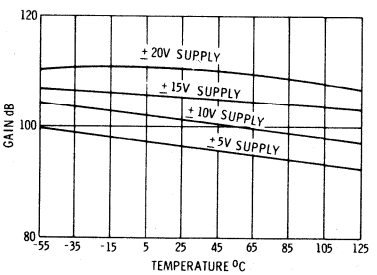


OPEN-LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM BANDWIDTH CONTROL PIN TO GROUND

Note: External Compensation Components are not Required for Stability, But May be Added to Reduce Bandwidth if Desired. If External Compensation is Used, Also Connect 100pF Capacitor From Output to Ground.

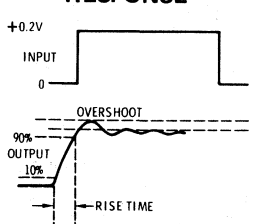


COMMON MODE VOLTAGE RANGE
AS A FUNCTION OF SUPPLY VOLTAGE



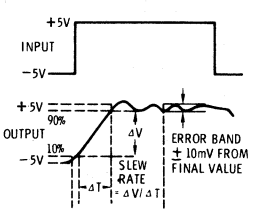
OPEN-LOOP VOLTAGE GAIN VS. TEMPERATURE

TRANSIENT RESPONSE

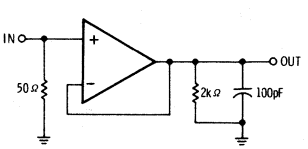


NOTE: MEASURED ON BOTH POSITIVE AND NEGATIVE TRANSITIONS.

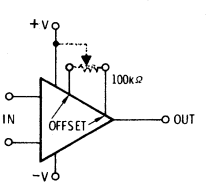
SLEW RATE AND SETTLING TIME



SLEW RATE AND TRANSIENT RESPONSE

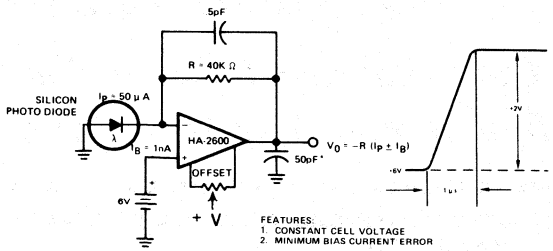


SUGGESTED OFFSET ZERO ADJUST HOOK-UP

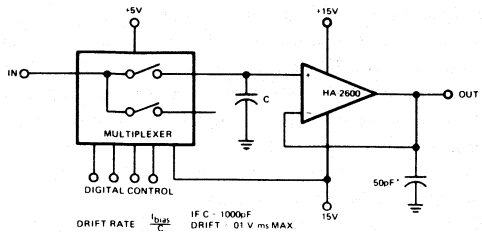


TYPICAL APPLICATIONS

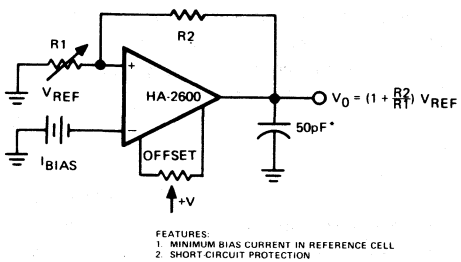
PHOTO-CURRENT TO VOLTAGE CONVERTER



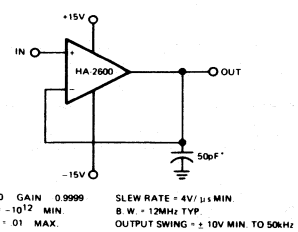
SAMPLE – AND – HOLD



REFERENCE VOLTAGE AMPLIFIER



VOLTAGE FOLLOWER



*A small load capacitance is recommended in all applications where practical to prevent possible high frequency oscillations resulting from external wiring parasitics. Capacitance up to 100pF has negligible effect on the bandwidth or slew rate.

DEFINITIONS

INPUT OFFSET VOLTAGE – That voltage which must be applied between the input terminals through two equal resistances to force the output voltage to zero.

INPUT OFFSET CURRENT – The difference in the currents into the two input terminals when the output is at zero voltage.

INPUT BIAS CURRENT – The average of the currents flowing into the input terminals when the output is at zero voltage.

INPUT COMMON MODE VOLTAGE – The average referred to ground of the voltages at the two input terminals.

COMMON MODE RANGE – The range of voltages which is exceeded at either input terminal will cause the amplifier to cease operating.

COMMON MODE REJECTION RATIO – The ratio of a specified range of input common mode voltage to the peak-to-peak change in input offset voltage over this range.

OUTPUT VOLTAGE SWING – The peak symmetrical output voltage swing, referred to ground, that can be obtained without clipping.

INPUT RESISTANCE – The ratio of the change in input voltage to the change in input current.

OUTPUT RESISTANCE – The ratio of the change in output voltage to the change in output current.

VOLTAGE GAIN – The ratio of the change in output voltage to the change in input voltage producing it.

BANDWIDTH – The frequency at which the voltage gain is 3dB below its low frequency value.

UNITY GAIN BANDWIDTH – The frequency at which the voltage gain of the amplifier is unity.

POWER SUPPLY REJECTION RATIO – The ratio of the change in input offset voltage to the change in power supply voltage producing it.

TRANSIENT RESPONSE – The closed loop step function response of the amplifier under small signal conditions.

PHASE MARGIN – $(180^0 - (\phi_1 - \phi_2))$ where ϕ_1 is the phase shift at the frequency where the absolute magnitude of gain is unity ϕ_2 is the phase shift at a frequency much lower than the open loop bandwidth.

SLEW RATE (Rate Limiting) – The rate at which the output will move between full scale stops, measured in terms of volts per unit time. This limit to an ideal step function response is due to the non-linear behavior in an amplifier due to its limited ability to produce large, rapid changes in output voltage (slewing) . . . restricting it to rates of change of voltage lower than might be predicted by observing the small signal frequency response.

SETTLING TIME – Time required for output waveform to remain within 0.1% of final value.

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HA-2607/2627

Epoxy-Packaged, Wide Band Operational Amplifier Series

Preliminary

2

FEATURES

	HA-2607	HA-2627	
• Wide Gain-Bandwidth	12	100	MHz
• High Slew Rate	7	35	V/μ S
• Wide Power Bandwidth	75	600	kHz
• High Gain	150KV/V		
• High Input Impedance	500M Ω		
• Output Short Circuit Protection			

APPLICATIONS

- Pulse Amplification
- Video Amplifiers
- Audio Amplifiers and Filters
- High Speed Test Equipment
- High Speed Comparators

DESCRIPTION

HA-2607/2627 bipolar operational amplifiers are high performance, epoxy-packaged monolithic IC's designed to deliver outstanding wideband AC performance. HA-2607 has a specified bandwidth of 12MHz while HA-2627 has a typical gain-bandwidth of 100MHz!* HA-2607 and HA-2627 also offer correspondingly high slew rates of 7V/μ Sec and 35V/μ Sec respectively. These dynamic characteristics, coupled with 150,000V/V open-loop gain enables HA-2607/2627 to perform high-gain amplification of very fast, wideband signals. This level of performance is achieved through the use of Harris' unique Dielectric Isolation processing techniques.

The HA-2607 and HA-2627 op amps afford an economical means of designing high performance equipment for industrial and commercial use. These amplifiers are ideally suited to pulse amplification designs as well as high frequency (e.g. RF, video) applications. The frequency response of both amplifiers can be tailored to exact design requirements by means of an external bandwidth control capacitor.

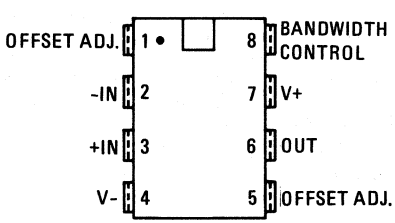
HA-2607/2627 are specified from 0°C to +75°C and are available in 8-lead epoxy DIP packages that have been extensively tested and qualified to deliver the high level of performance and reliability that are expected of Harris Semiconductor's operational amplifiers.

*HA-2607/2627 are internally compensated – HA-2607 is stable for $A_V \geq 1$, – HA- 2627 is stable for $A_V \geq 5$.

PINOUT

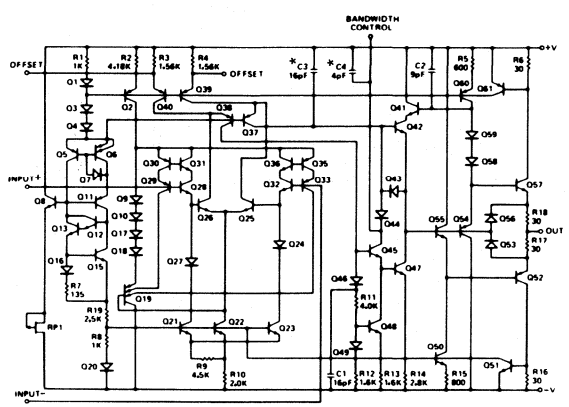
Package Code 3A

TOP VIEW



8 LEAD DIP EPOXY

SCHEMATIC



*VALUES OF C3 AND C4 VARY DEPENDING ON DEVICE TYPE.

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	45.0V
Differential Input Voltage	±12.0V
Peak Output Current	Full Short Circuit Protection
Internal Power Dissipation (Note 10)	300mW
Operating Temperature Range – HA-2607/HA-2627	$0^o \leq T_A \leq +75^oC$
Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$

ELECTRICAL CHARACTERISTICS

V+=+15VDC, V-= -15VDC

		HA-2607 0°C to +75°C LIMITS			HA-2627 0°C to +75°C			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		4	6		4	6	mV
	Full			8			8	mV
Offset Voltage Average Drift	Full		5			5	30	nA
Bias Current	+25°C		5	30		5	30	nA
	Full			50			50	
Offset Current	+25°C		5	30		5	30	nA
	Full			50			50	nA
Input Resistance	+25°C	40	300		40	300		MΩ
Common Mode Range	Full	±10.0			±10.0			V
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 1)	+25°C	70	150K		70	150K		V/V
	Full	60			60			V/V
Common Mode Rejection Ratio (Note 2)	Full	74	100		74	100		dB
Gain Bandwidth Product (Note 3, 11)	+25°C		12			100		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		V
Output Current (Note 4)	+25°C	±10	±18		±10	±18		mA
Full Power Bandwidth (Note 4)	+25°C	50	75		290	600		kHz
TRANSIENT RESPONSE								
Rise Time (Notes 1, 5, 6 & 8)	+25°C		30	60		17	45	ns
Overshoot (Notes 1, 5, 7 & 8)	+25°C		25	40		25	40	%
Slew Rate (Notes 1, 5, 8 & 12)	+25°C	±4	±7		±17	±35		V/μs
Settling Time (Notes 1, 5, 8 & 12)	+25°C		1.5			1.5		μs
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C		3.0	4.0		3.0	4.0	mA
Power Supply Rejection Ratio (Note 9)	Full	74	90		74	90		dB

TEST CONDITIONS

NOTES:
1. R_L = 2K
2. V_{CM} = +5.0V
3. V_O < 90mV
4. V_O = +10V
5. C_L = 100pF
6. V_L = +200mV
7. V_O = +400mV
8. For HA-2607, A_V = 1; For HA-2627, A_V = 5.
9. V_S = +9.0V to +15V
10. Derate by 6.6mW/°C above 105°C
11. 40 dB gain setting used to measure Gain-Bandwidth for HA-2627
12. V_{OUT} = ±5V

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HA-2620/2622/2625

Very Wide Band, Uncompensated Operational Amplifiers

2

FEATURES

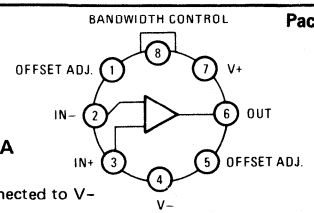
- GAIN BANDWIDTH PRODUCT(A_V = 5) 100MHz
- HIGH INPUT IMPEDANCE 500MΩ
- LOW INPUT BIAS CURRENT 1nA
- LOW INPUT OFFSET CURRENT 1nA
- LOW INPUT OFFSET VOLTAGE 0.5mV
- HIGH GAIN 150K V/V
- HIGH SLEW RATE 35V/μs
- OUTPUT SHORT CIRCUIT PROTECTION

APPLICATIONS

- VIDEO AND R.F. AMPLIFIERS
- PULSE AMPLIFIER
- AUDIO AMPLIFIERS AND FILTERS
- HIGH-Q ACTIVE FILTERS
- HIGH-SPEED COMPARATORS
- LOW DISTORTION OSCILLATORS

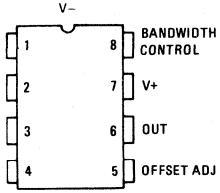
PINOUT

TO-99 — **Package Code 2A, 1N, 4U, LA**



2A

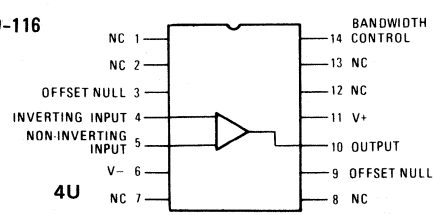
Case Connected to V−



TOP VIEWS

1N

TO-116



4U

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

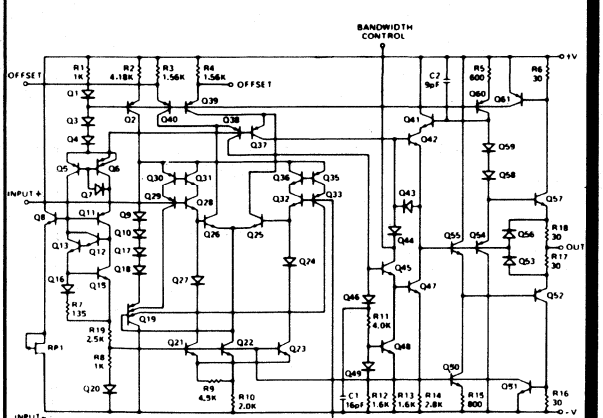
DESCRIPTION

HA-2620/2622/2625 are bipolar operational amplifiers that feature very high input impedance (500MΩ, HA-2620) coupled with wideband AC performance. The high resistance of the input stage is complemented by low offset voltage (0.5mV, HA-2620) and low bias and offset current (1nA, HA-2620) to facilitate accurate signal processing. Input offset can be reduced further by means of an external nulling potentiometer. 100MHz gain-bandwidth product (HA-2620/2622/2625 are stable for closed loop gains greater than 5), 35V/ μs slew rate and 150,000V/V open-loop gain enables HA-2620/2622/2625 to perform high-gain amplification of very fast, wideband signals. These dynamic characterisitcs, coupled with fast settling times, make these amplifiers ideally suited to pulse amplification designs as well as high frequiency (e.g. video) applications. The frequency response of the amplifier can be tailored to exact design requirements by means of an external bandwidth control capacitor.

In addition to its application in pulse and video amplifier designs HA-2620/2622/2625 is particularly suited to other high performance designs such as high-gain low distortion audio amplifiers, high-Q and wideband active filters and high-speed comparators.

HA-2620 and HA-2622 are guaranteed over -55°C to +125°C. HA-2625 is specified from 0°C to +75°C. All devices are available in TO-99 cans, and 14 lead D.I.P. packages.

SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	45.0V
Differential Input Voltage	±12.0V
Peak Output Current	Full Short Circuit Protection
Internal Power Dissipation	300mW
Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$

ELECTRICAL CHARACTERISTICS

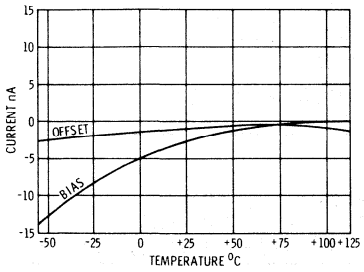
$V^+ = +15$ VDC, $V^- = -15$ VDC

PARAMETER	TEMPERATURE	HA-2620 −55°C to +125°C MIN.	HA-2620 TYP.	HA-2620 MAX.	HA-2622 −55°C to +125°C MIN.	HA-2622 TYP.	HA-2622 MAX.	HA-2625 0°C to +75°C MIN.	HA-2625 TYP.	HA-2625 MAX.	UNITS
INPUT CHARACTERISTICS											
* Offset Voltage (Note 1)	+25°C		0.5	4		3	5		3	5	mV
	Full			6			7			7	mV
* Bias Current	+25°C		1	15		5	25		5	25	nA
	Full		10	35			60			40	nA
* Offset Current	+25°C		1	15		5	25		5	25	nA
	Full		5	35			60			40	nA
Input Resistance (Note 11)	+25°C	65	500		40	300		40	300		MΩ
Common Mode Range	Full	±11.0			±11.0			±11.0			V
TRANSFER CHARACTERISTICS											
* Large Signal Voltage Gain (Notes 2 & 3)	+25°C	100K	150K		80K	150K		80K	150K		V/V
	Full	70K			60K			70K			V/V
* Common Mode Rejection Ratio (Note 4)	Full	80	100		74	100		74	100		dB
Gain Bandwidth Product (Notes 2, 5, &6)	+25°C		100			100			100		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 2)	Full	±10.0	±12.0		±10.0	±12.0		±10.0	±12.0		V
* Output Current (Note 3)	+25°C	±15	±22		±10	±18		±10	±18		mA
Full Power Bandwidth (Notes 2, 3, 7 &12)	+25°C	400	600		320	600		320	600		kHz
TRANSIENT RESPONSE											
Rise Time (Notes 2, 7 & 8)	+25°C		17	45		17	45		17	45	ns
* Slew Rate (Notes 2, 7, 8 & 10)	+25°C	±25	±35		± 20	±35		± 20	±35		V/μs
POWER SUPPLY CHARACTERISTICS											
* Supply Current	+25°C		3.0	3.7		3.0	4.0		3.0	4.0	mA
* Power Supply Rejection Ratio (Note 9)	Full	80	90		74	90		74	90		dB

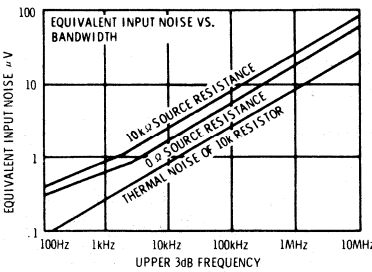
NOTES:
1. Offset may be externally adjusted to zero.
2. $R_L = 2K\Omega$, $C_L = 50pF$
3. $V_O = \pm 10.0V$
4. $V_{CM} = \pm 10V$
5. $V_O < 90mV$
6. 40dB Gain
7. See transient response test circuits and waveforms
8. $A_V = 5$ (The HA-2620 family is not stable at unity gain without external compensation.)
9. $\Delta V_{Sup} = \pm 5V$
10. $V_{OUT} = \pm 5V$
11. This parameter value based upon design calculations.
12. Full power bandwidth guaranteed based upon slew rate measurement FPBW = $S.R./2\pi V_{peak}$.

*100% Tested For DASH 8

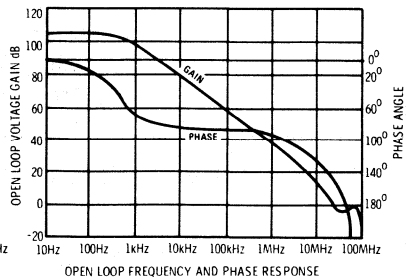
V+ = 15VDC, V- = 15VDC, T_A = 25°C UNLESS OTHERWISE STATED.



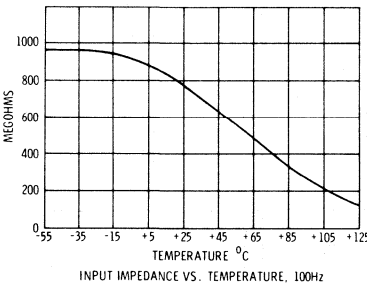
INPUT BIAS CURRENT AND OFFSET CURRENT-
AS A FUNCTION OF TEMPERATURE



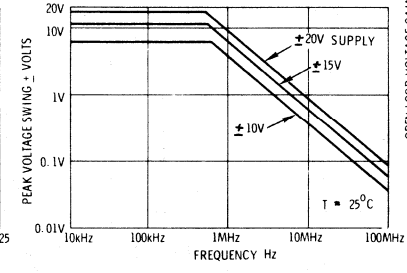
UPPER 3dB FREQUENCY
LOWER 3dB FREQUENCY - 10Hz
BROADBAND NOISE CHARACTERISTICS



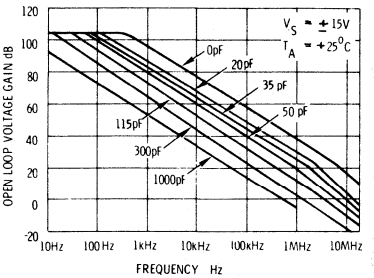
OPEN LOOP FREQUENCY AND PHASE RESPONSE



INPUT IMPEDANCE VS. TEMPERATURE, 100Hz

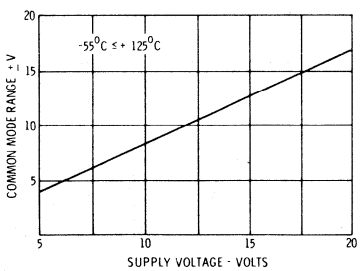


OUTPUT VOLTAGE SWING VS. FREQUENCY

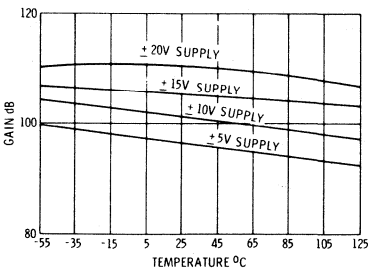


OPEN-LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM BANDWIDTH CONTROL PIN TO GROUND

Note: External Compensation is Required For Closed Loop Gain <5. If External Compensation is Used, Also Connect 100 pF Capacitor From Output to Ground.

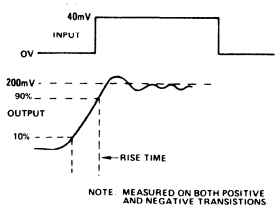


COMMON MODE VOLTAGE RANGE
AS A FUNCTION OF SUPPLY VOLTAGE



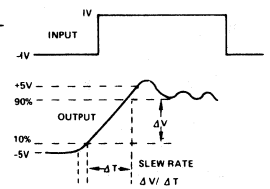
OPEN-LOOP VOLTAGE GAIN VS. TEMPERATURE

TRANSIENT RESPONSE

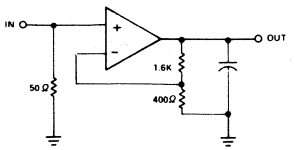


NOTE: MEASURED ON BOTH POSITIVE AND NEGATIVE TRANSISTIONS

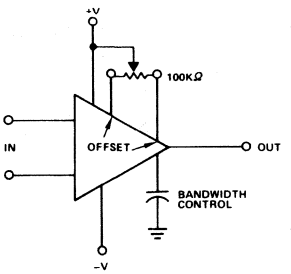
SLEW RATE



SLEW RATE AND TRANSIENT RESPONSE

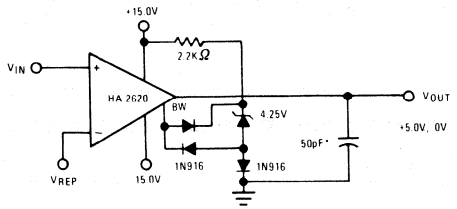


SUGGESTED OFFSET ZERO ADJUST AND BANDWIDTH CONTROL HOOK-UP

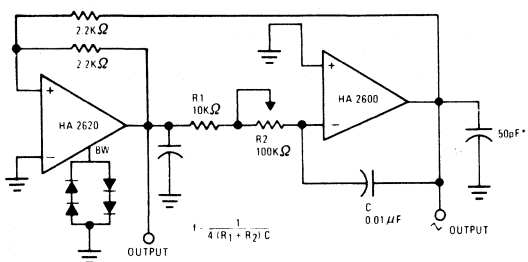


TYPICAL APPLICATIONS

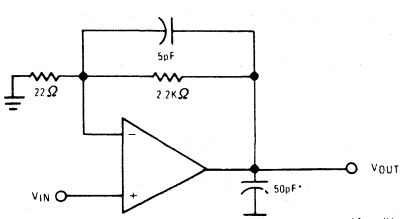
HIGH IMPEDANCE COMPARATOR



FUNCTION GENERATOR



VIDEO AMPLIFIER



*A small load capacitance of at least 30pF (including stray capacitance) is recommended to prevent possible high frequency oscillations.

DEFINITIONS

INPUT OFFSET VOLTAGE—That voltage which must be applied between the input terminals through two equal resistances to force the output voltage to zero.

INPUT OFFSET CURRENT—The difference in the currents into the two input terminals when the output is at zero voltage.

INPUT BIAS CURRENT—The average of the currents flowing into the input terminals when the output is at zero voltage.

INPUT COMMON MODE VOLTAGE—The average referred to ground of the voltages at the two input terminals.

COMMON MODE RANGE—The range of voltages which is exceeded at either input terminal will cause the amplifier to cease operating.

COMMON MODE REJECTION RATIO—The ratio of a specified range of input common mode voltage to the peak-to-peak change in input offset voltage over this range.

OUTPUT VOLTAGE SWING—The peak symmetrical output voltage swing, referred to ground, that can be obtained without clipping.

INPUT RESISTANCE—The ratio of the change in input voltage to the change in input current.

OUTPUT RESISTANCE—The ratio of the change in output voltage to the change in output current.

VOLTAGE GAIN—The ratio of the change in output voltage to the change in input voltage producing it.

UNITY GAIN BANDWIDTH—The frequency at which the voltage gain of the amplifier is unity.

POWER SUPPLY REJECTION RATIO—The ratio of the change in input offset voltage to the change in power supply voltage producing it.

TRANSIENT RESPONSE—The closed loop step function response of the amplifier under small signal conditions.

GAIN BANDWIDTH PRODUCT—The product of the gain and the bandwidth at a given gain.

SLEW RATE (Rate Limiting)—The rate at which the output will move between full scale stops, measured in terms of volts per unit time. This limit to an ideal step function response is due to the non-linear behavior in an amplifier due to its limited ability to produce large, rapid changes in output voltage (slewing)...restricting it to rates of change of voltage lower than might be predicted by observing the small signal frequency response.

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HA-2630/2635

High Performance Current Booster

2

FEATURES

- OUTPUT CURRENT ±400mA
- SLEW RATE 500V/μs
- BANDWIDTH 8MHz
- FULL POWER BANDWIDTH 8MHz
- INPUT RESISTANCE $2.0 \times 10^6 \Omega$
- OUTPUT RESISTANCE 2.0Ω
- POWER SUPPLY RANGE ±5V to ±20V
- PACKAGE IS ELECTRICALLY ISOLATED

APPLICATIONS

- COAXIAL CABLE DRIVERS
- AUDIO OUTPUT AMPLIFIERS
- SERVO MOTOR DRIVERS
- POWER SUPPLIES (BIPOLAR)
- PRECISION DATA RECORDING

DESCRIPTION

HA-2630 and HA-2635 are monolithic, unity voltage gain current amplifiers delivering extremely high slew rate, wide bandwidth, and full power bandwidth even under heavy output loading conditions. This dielectrically isolated current booster also offers high input impedance and low output resistance. These devices are intended to be used in series with an operational amplifier and inside the feedback loop whenever additional output current is required. Output current levels are programmable by selecting two optional external resistors.

These current amplifiers offer an exceptional 500V/μs slew rate and 8MHz bandwidth which allows them to be used with many high performance op amps in precision data recording and high speed coaxial cable driver designs. 2.0M ohm input resistance and 2 ohm output resistance coupled with ±400mA output current make HA-2630 and HA-2635 ideal components in high fidelity audio output amplifier designs.

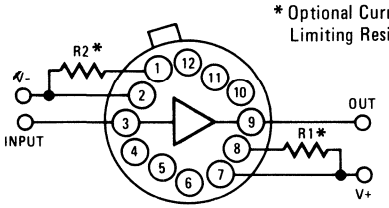
HA-2630 and HA-2635 are available in an electrically isolated TO-8 type can for ease of mounting with or without a heat sink. HA-2630 is specified over the -55°C to +125°C range. HA-2635 is specified from 0°C to +75°C.

PINOUT

TO-8 **Package Code 6G**

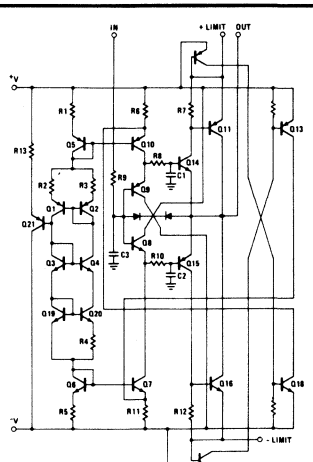
TOP VIEW

* Optional Current Limiting Resistor



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	40V
Input Voltage Range	± V Supply
Output Current (Note 2)	±700mA
Internal Power Dissipation (Note 6) Free Air:	1W
In Heat Sink:	4W

Operating Temperature Range:
$-55^{o}C \leq T_A \leq +125^{o}C$ (HA-2630)
$0^{o}C \leq T_A \leq +75^{o}C$ (HA-2635)
Storage Temperature Range:
$-65^{o}C \leq T_A \leq +150^{o}C$

ELECTRICAL CHARACTERISTICS

V_{Supply} = ±15 Volts R_L = 50 Ohms $R_1 = R_2$ = 0 Ohms Unless otherwise specified.

PARAMETER	TEMP.	HA-2630 -55°C to +125°C MIN.	HA-2630 -55°C to +125°C TYP.	HA-2630 -55°C to +125°C MAX.	HA-2635 0°C to +75°C MIN.	HA-2635 0°C to +75°C TYP.	HA-2635 0°C to +75°C MAX.	UNITS
INPUT CHARACTERISTICS								
*Bias Current	+25°C		30	150		30	150	µA
	Full			200			200	µA
Input Resistance	+25°C		2.0			2.0		MΩ
Input Capacitance	+25°C		5.0			5.0		pF
TRANSFER CHARACTERISTICS								
Voltage Gain (Note 1)	Full	.85	.95		.85	.95		V/V
*Offset Voltage ($V_{OUT} - V_{IN}$)	+25°C		70	±200		70	±200	mV
	Full			±300			±300	mV
Bandwidth (-3dB)	+25°C		8.0			8.0		MHz
OUTPUT CHARACTERISTICS								
*Output Voltage Swing	Full	±10			±10			V
*Output Current (Note 1)	Full	±300	±400		±300	±400		mA
Output Resistance	+25°C		2.0			2.0		Ω
Full Power Bandwidth (Note 1)	+25°C		8.0			8.0		MHz
TRANSIENT RESPONSE								
Rise Time (Note 3)	+25°C		30			30		ns
Slew Rate (Note 4)	+25°C	200	500		200	500		V/µs
POWER SUPPLY CHARACTERISTICS								
*Supply Current	Full		15	20		15	23	mA
Supply Voltage Range	Full	±5		±20	±5		±20	V
Power Supply Rejection Ratio (Note 5)	Full		66			66		dB

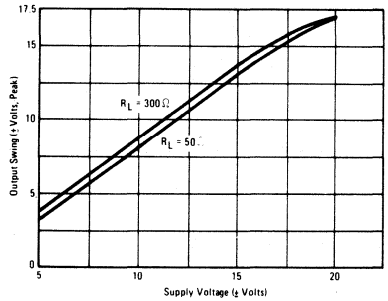
NOTES:
1. V_O = ±10V
2. Heat sink is required for continuous short circuit protection, regardless of current limit setting.
3. V_O = 0.4V p-p.
4. V_O = 10V p-p.
5. ΔV_{SUPPLY} = ±5V.
6. Without heat sink, derate by 14mW/°C ambient temperature above 100°C ambient, with heat sink, derate by 67mW/°C case temperature above 115°C case.

*100% Tested For DASH 8

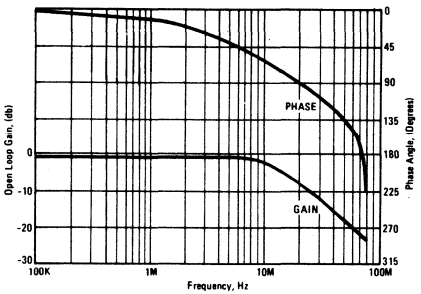
PERFORMANCE CURVES

V+ = 15VDC, V- = 15VDC, T_A = 25°C UNLESS OTHERWISE STATED

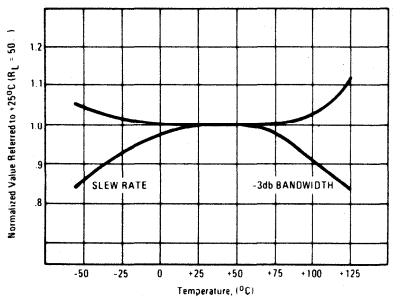
OUTPUT SWING
(R_{LIMIT} = 0Ω)



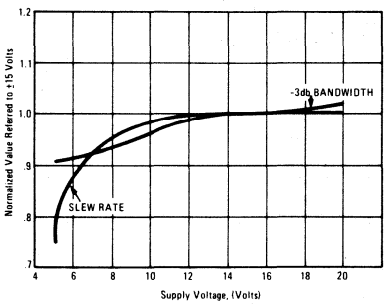
OPEN LOOP FREQUENCY AND
PHASE RESPONSE (R_L = 50Ω, C_L ≈10pf)



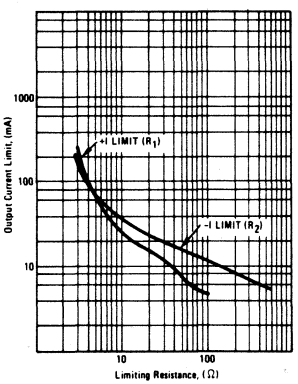
NORMALIZED AC PARAMETERS vs.
TEMPERATURE (R_L = 50Ω)



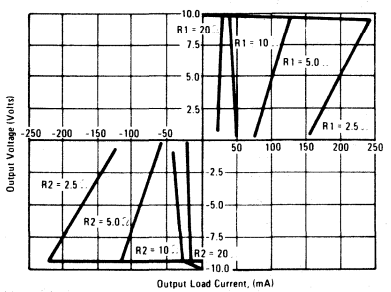
NORMALIZED AC PARAMETERS vs.
SUPPLY VOLTAGE (R_L = 50Ω)



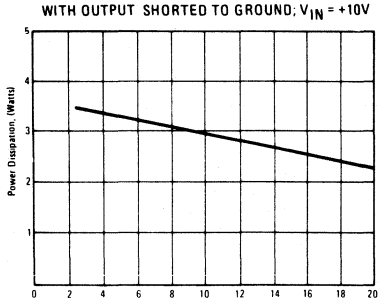
OUTPUT CURRENT LIMITING vs.
LIMITING RESISTANCE



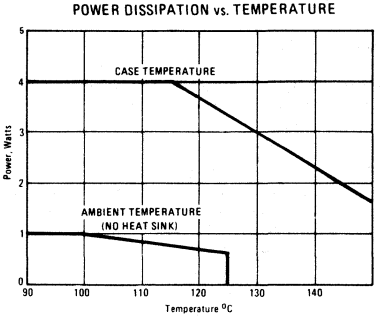
OUTPUT CURRENT CHARACTERISTIC



POWER DISSIPATION vs. LIMITING RESISTANCE
WITH OUTPUT SHORTED TO GROUND; V_{IN} = +10V

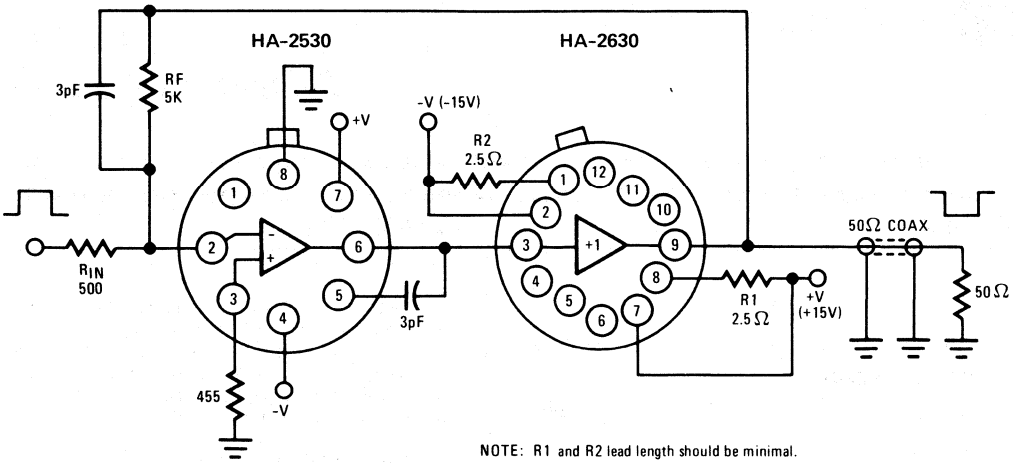


MAXIMUM ALLOWABLE INTERNAL
POWER DISSIPATION vs. TEMPERATURE



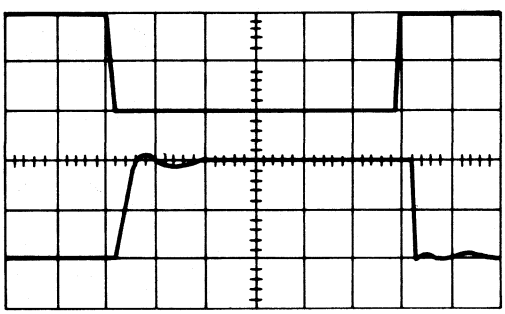
TYPICAL APPLICATION

20dB, 5MHz VIDEO COAXIAL LINE DRIVER



NOTE: R1 and R2 lead length should be minimal.

LINE DRIVER PULSE RESPONSE



Horizontal Scale = 200ns/Div.
Upper Trace: Input, 200mV/Div.
Lower Trace: Output, 2V/Div.

SOME OTHER APPLICATIONS

- BIPOLAR POWER SUPPLY
- FUNCTION GENERATOR OUTPUT
- DEFLECTION COIL DRIVE
- AUDIO OUTPUT AMPLIFIER

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HA-2640/2645

High Voltage Operational Amplifier

2

FEATURES

- OUTPUT VOLTAGE SWING ±35V
- SUPPLY VOLTAGE ±10V TO ±40V
- OFFSET CURRENT 5nA
- BANDWIDTH 4MHz
- SLEW RATE 5V/μs
- COMMON MODE INPUT VOLTAGE SWING ±35V
- OUTPUT OVERLOAD PROTECTION

APPLICATIONS

- INDUSTRIAL CONTROL SYSTEMS
- POWER SUPPLIES
- HIGH VOLTAGE REGULATORS
- RESOLVER EXCITATION
- SIGNAL CONDITIONING

DESCRIPTION

HA-2640 and HA-2645 are monolithic operational amplifiers which are designed to deliver unprecedented dynamic specifications for a high voltage internally compensated device. These dielectrically isolated devices offer very low values for offset voltage and offset current coupled with large output voltage swing and common mode input voltage.

For maximum reliability, these amplifiers offer unconditional output overload protection through current limiting and a chip temperature sensing circuit. This sensing device turns the amplifier "off", when the chip reaches a certain temperature level.

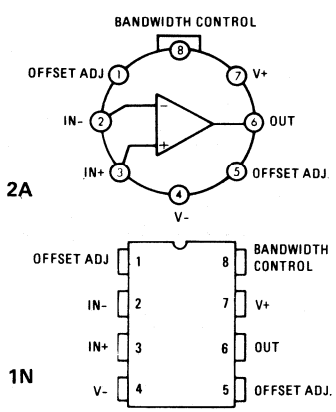
These amplifers deliver ±35V common mode input voltage swing, ±35V output voltage swing, and up to ±40V supply range for use in such designs as regulators, power supplies, and industrial control systems. 4MHz gain bandwidth and 5V/μs slew rate make these devices excellent components for high performance signal conditioning applications. Outstanding input and output voltage swings coupled with a low 5nA offset current make these amplifiers excellent components for resolver excitation designs.

HA-2640 and HA-2645 are available in metal can (TO-99) packages and can be used as high performance pin-to-pin replacements for many general purpose op amps. HA-2640 is specified from -55°C to +125°C and HA-2645 is specified over the 0°C to +75°C range.

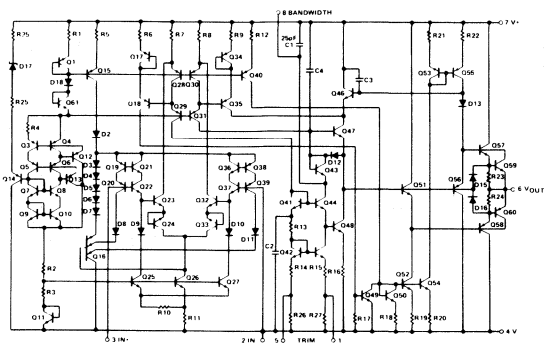
PINOUT

TO-99 **Package Code 2A, 1N**

TOP VIEWS



SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals 100V
Input Voltage Range ±37V
Output Current/Full Short Circuit Protection
Internal Power Dissipation 680mW*

*Derate by 4.6mW/°C above +25°C

Operating Temperature Range
$-55^{\circ}C \leq T_A \leq +125^{\circ}C$ (HA-2640)
$0^{\circ}C \leq T_A \leq +75^{\circ}C$ (HA-2645)
Storage Temperature Range
$-65^{\circ}C \leq T_A \leq +150^{\circ}C$

ELECTRICAL CHARACTERISTICS

$V_{Supply} = \pm 40V$, $R_L = 5K$, Unless Otherwise Specified.

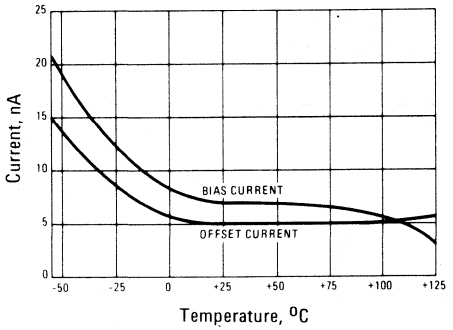
PARAMETER	TEMP.	HA-2640 -55°C to +125°C MIN.	HA-2640 -55°C to +125°C TYP.	HA-2640 -55°C to +125°C MAX.	HA-2645 0°C to +75°C MIN.	HA-2645 0°C to +75°C TYP.	HA-2645 0°C to +75°C MAX.	UNITS
INPUT CHARACTERISTICS								
* Offset Voltage	+25°C		2	4		2	6	mV
	Full			6			7	mV
Offset Voltage Average Drift	Full		15			15		µV/°C
* Bias Current	+25°C		10	25		12	30	nA
	Full			50			50	nA
* Offset Current	+25°C		5	12		15	30	nA
	Full			35			50	nA
Input Resistance **(Note 10)**	+25°C	50	250		40	200		MΩ
Common Mode Range	Full	±35			±35			V
TRANSFER CHARACTERISTICS								
* Large Signal Voltage Gain (Note 8)	+25°C	100K	200K		100K	200K		V/V
	Full	75K			75K			V/V
* Common Mode Rejection Ratio (Note 1)	Full	80	100		74	100		dB
Unity Gain Bandwidth (Note 2)	+25°C		4			4		MHz
OUTPUT CHARACTERISTICS								
* Output Voltage Swing	Full	±35			±35			V
* Output Current (Note 9)	+25°C	±12	±15		±10	±12		mA
Output Resistance	+25°C		500			500		Ω
Full Power Bandwidth **(Notes 3 &11)**	+25°C		23			23		kHz
TRANSIENT RESPONSE (Note 7)								
Rise Time (Notes 4, 6)	+25°C		60	**100**		60	**100**	ns
Overshoot (Notes 4, 6)	+25°C		15	**30**		15	**40**	%
Slew Rate (Note 6)	+25°C	**±3**	**±5**		**±2.5**	**±5**		V/µs
POWER SUPPLY CHARACTERISTICS								
* Supply Current	+25°C		3.2	3.8		3.2	4.5	mA
Supply Voltage Range	Full	±10		±40	±10		±40	V
* Power Supply Rejection Ratio (Note 5)	Full	80	90		74	90		dB

NOTES:
1. $V_{CM} = \pm 20V$
2. $V_O = 90mV$
3. $V_O = \pm 35V$
4. $V_O = \pm 200mV$
5. $V_S = \pm 10V$ to $\pm 40V$
6. $A_V = 1$
7. $C_L = 50pF$
8. $V_O = \pm 30V$
9. $R_L = 1K$
10. This parameter based upon design calculations.
11. Full power bandwidth guaranteed based upon slew rate measurement. $FPBW = S.R./2\pi V_{peak}$.

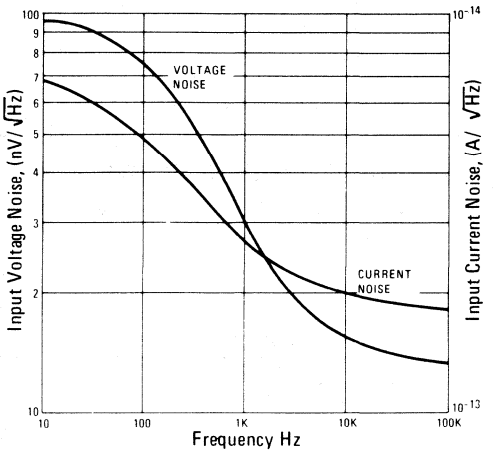
*100% Tested For DASH 8

V+ = V- = 40VDC, T_A = +25°C UNLESS OTHERWISE STATED

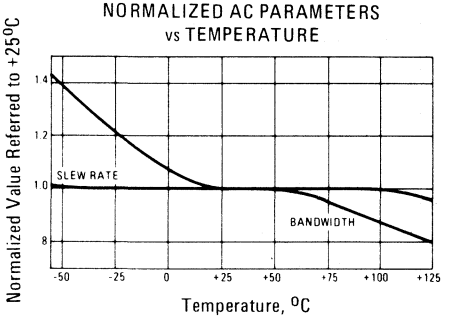
INPUT BIAS AND OFFSET CURRENT vs TEMPERATURE



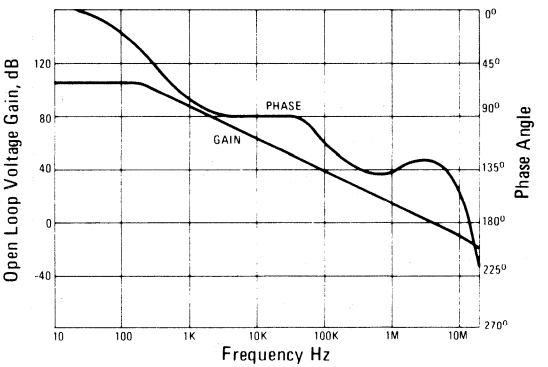
INPUT NOISE CHARACTERISTICS



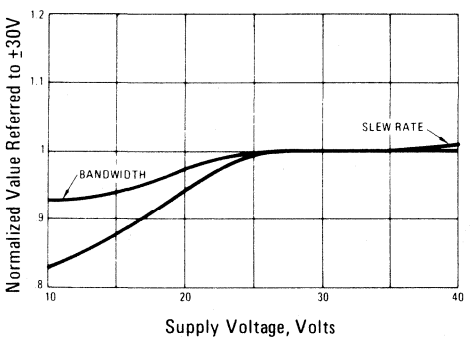
NORMALIZED AC PARAMETERS vs TEMPERATURE



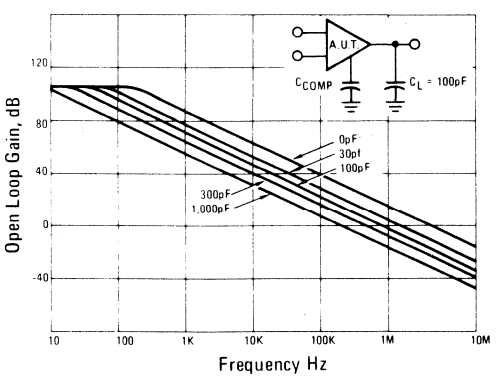
OPEN LOOP FREQUENCY AND PHASE RESPONSE



NORMALIZED AC PARAMETERS vs SUPPLY VOLTAGE AT +25°C



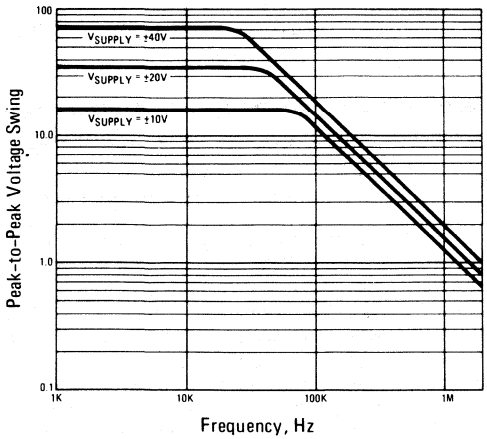
OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM BANDWIDTH CONTROL PIN TO GROUND



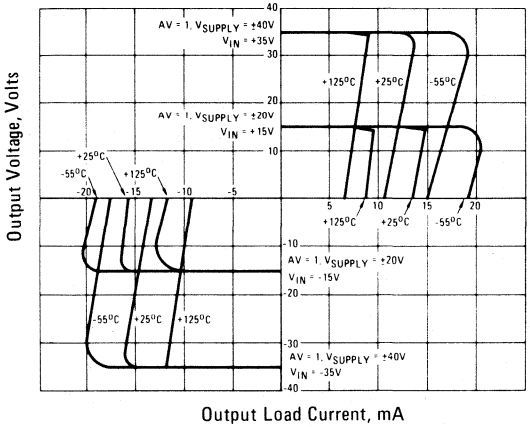
NOTE: External Compensation Components are not Required for Stability. But May be Added to Reduce Bandwidth if Desided. C_L = 100pF is Also Required for Stability Only if External Compensation Capacitor is Used.

PERFORMANCE CURVES (continued)

OUTPUT VOLTAGE SWING
vs FREQUENCY AT +25°C

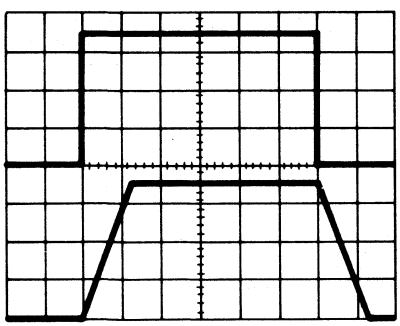


OUTPUT CURRENT CHARACTERISTIC



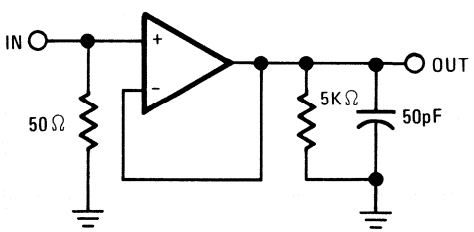
SWITCHING WAVEFORM AND TEST CIRCUIT

VOLTAGE FOLLOWER
PULSE RESPONSE



R_L = 5K, C_L = 50pF
Vertical = 10V/Div.
Horizontal = 5µs/Div.
T_A = +25°C
V_S = ±40V

SLEW RATE AND TRANSIENT
RESPONSE TEST CIRCUIT



2

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HA-2650/2655

Dual High Performance Operational Amplifier

2

FEATURES

- SLEW RATE — 5V/μs
- BANDWIDTH — 8MHz
- BIAS CURRENT — 35nA
- AV. OFFSET VOLTAGE DRIFT — 8μV/°C
- POWER CONSUMPTION — 75mW
- SUPPLY VOLTAGE RANGE — ±2V TO ±20V

APPLICATIONS

- VIDEO AMPLIFIERS
- HIGH IMPEDANCE, WIDEBAND BUFFERS
- INTEGRATORS
- AUDIO AMPLIFIERS
- ACTIVE FILTERS

DESCRIPTION

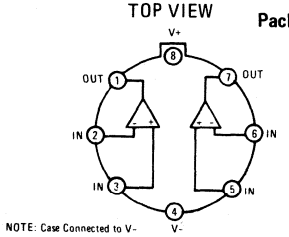
HA-2650/2655 contains two internally compensated operational amplifiers offering high slew rate and high frequency performance combined with exceptional DC characteristics. 5V/μ sec slew rate and 8MHz bandwidth make these amplifiers suitable for processing fast, wideband signals extending into the video frequency spectrum. Signal processing accuracy is enhanced by front-end performance that includes 1.5mV offset voltage, 8 μ V/°C offset voltage drift and low offset and bias current (1nA and 35nA respectively). Offset voltage can be trimmed to zero on the devices offered in dual-in-line packages. Signal conditioning is further enhanced by 500MΩ input impedance.

Applications for HA-2650/2655 include video circuit designs such as high impedance buffers, integrators, tone generators and filters. These amplifiers are also ideal components for active filtering of audio and voice signals.

HA-2650/2655 are offered in 14 pin D.I.P. and metal TO-99 packages and are also available in dice form. HA-2650 is specified from -55°C to +125°C. HA-2655 operates from 0°C to +75°C.

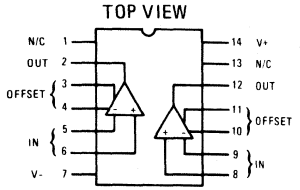
PINOUT

TO-99 — TOP VIEW — **Package Code 2A, 4U, 3A, LA**



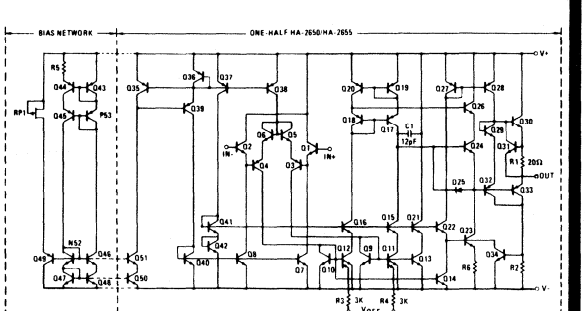
NOTE: Case Connected to V-

TO-116 — TOP VIEW



NOTE: Bottom of package is connected to V-

SCHEMATIC



 CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

T_A = +25°C Unless Otherwise Stated

Voltage Between V+ and V- Terminals	40.0V
Differential Input Voltage	±30.0V
Input Voltage (Note 1)	±15.0V
Output Short Circuit Duration	Indefinite

Power Dissipation (Note 2)	TO-99	300 mW
	TO-116	300 mW
Operating Temperature Range:		
HA-2650	$-55^{\circ}C \leq T_A \leq +125^{\circ}C$	
HA-2655	$0^{\circ}C \leq T_A \leq +75^{\circ}C$	
Storage Temperature Range	$-65^{\circ}C \leq T_A \leq +150^{\circ}C$	

ELECTRICAL CHARACTERISTICS

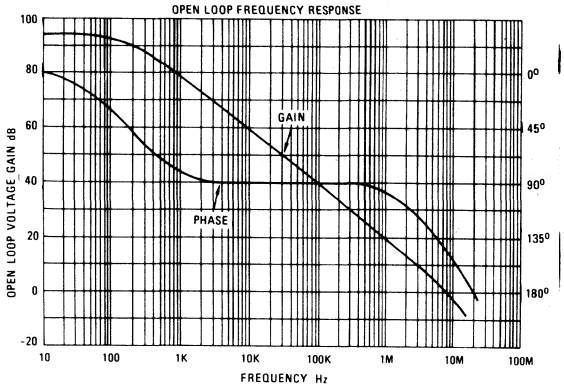
V+ = 15V V- = -15V

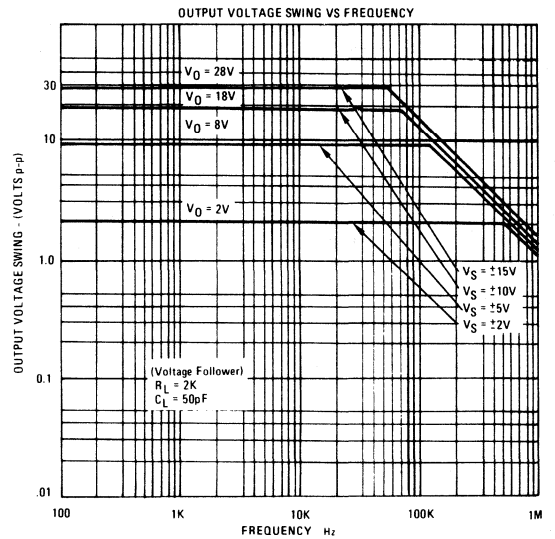
PARAMETER	TEMP.	HA-2650 -55°C to +125°C MIN.	HA-2650 -55°C to +125°C TYP.	HA-2650 -55°C to +125°C MAX.	HA-2655 0°C to +75°C MIN.	HA-2655 0°C to +75°C TYP.	HA-2655 0°C to +75°C MAX.	UNITS
INPUT CHARACTERISTICS								
*Offset Voltage	+25°C		1.5	3		2	5	mV
	Full			5			7	mV
Av. Offset Voltage Drift	Full		8			8		µV/°C
*Bias Current	+25°C		35	100		50	200	nA
	Full			200			300	nA
*Offset Current	+25°C		1	30		2	60	nA
	Full			60			100	nA
Common Mode Range	Full	±13			±13			V
Differential Input Resistance (Note 9)	+25°C	5	20		5	20		MΩ
Common Mode Input Resistance	+25°C		500			500		MΩ
Input Capacitance	+25°C		5			5		pF
TRANSFER CHARACTERISTICS								
*Large Signal Voltage Gain (Note 3ab)	+25°C	25K	40K		20K	40K		V/V
	Full	20K			15K			V/V
*Common Mode Rejection Ratio (Note 4)	+25°C	80	100		74	100		dB
	Full	80			74			dB
OUTPUT CHARACTERISTICS								
*Output Voltage Swing (Note 3c)	+25°C	±13	±14		±13	±14		V
	Full	±13			±13			V
Full Power Bandwidth (Notes 5 &10)	+25°C	30	80		30	80		KHz
Output Current (Note 3a)	+25°C		±20			±18		mA
Output Resistance	+25°C		100			100		Ω
TRANSIENT RESPONSE (Note 6)								
Rise Time (Note 7)	+25°C		40	80		40	90	ns
Overshoot (Note 7)	+25°C		15	30		15	40	%
Slew Rate	+25°C	±2	±5		±2	±5		V/µs
POWER SUPPLY CHARACTERISTICS								
*Supply Current	+25°C		2.5	3		3	4	mA
*Power Supply Rejection Ratio (Note 8)	+25°C	80	100		74	100		dB
	Full	80			74			dB

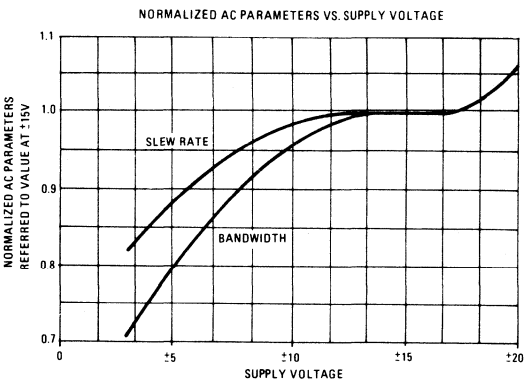
NOTES:
1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. Derate at 4.7mW/°C at ambient temperatures above +110°C.
3. (a) V_O = ±10V (b) R_L = 2K (c) R_L = 10K
4. V_{CM} = ±5.0V
5. A_V = 1, R_L = 2K, V_O = $20V_{pp}$
6. See transient response/slew rate circuit.
7. V_{in} = 200mV
8. Δ V = ±5.0V
9. This parameter value based upon design calculations.
10. Full power bandwidth guaranteed based upon slew rate measurement FPBW = S.R./$2\pi V_{peak}$.

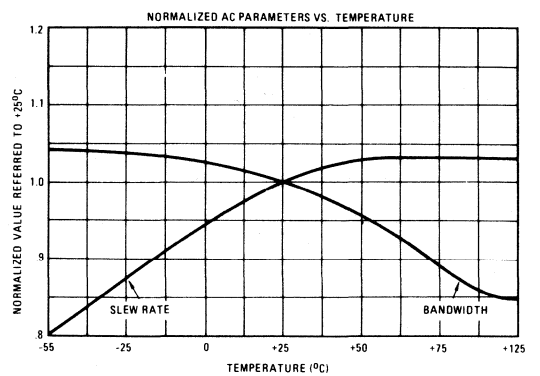
*100% Tested For DASH 8

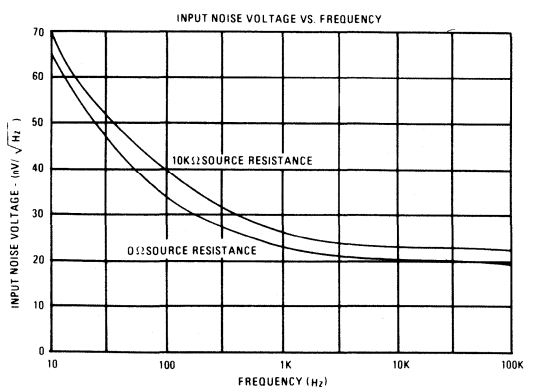
V+ = +15V, V- = -15V, T_A = +25°C Unless Otherwise Stated.

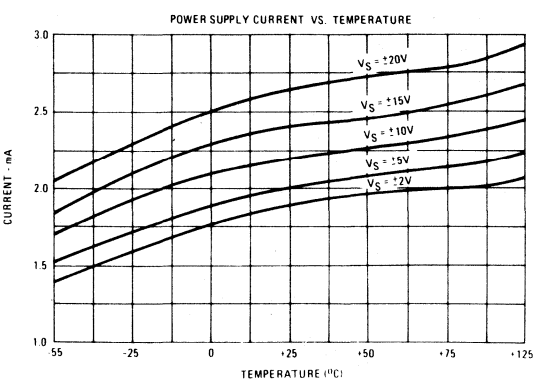






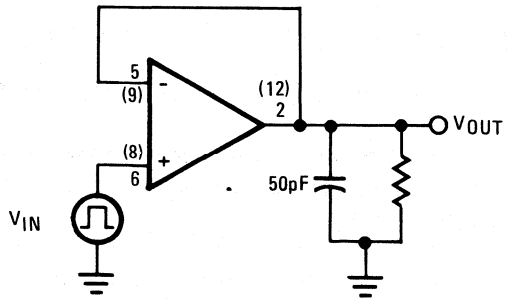






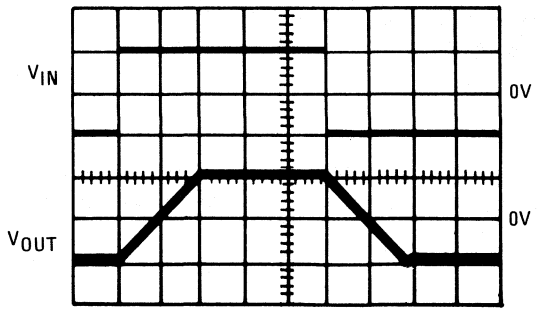
PERFORMANCE CHARACTERISTICS

TRANSIENT RESPONSE/SLEW RATE CIRCUIT



Note: Numbers in parentheses refer to the second half of TO-116 package.

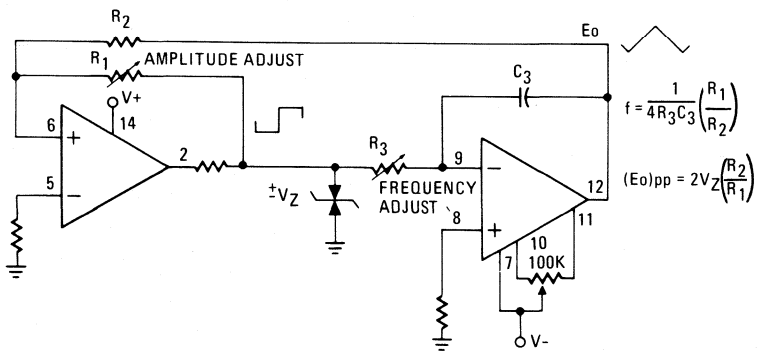
SLEWING WAVEFORM



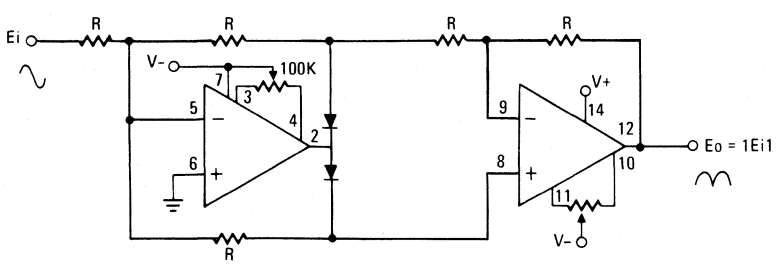
VERTICAL 5V/DIV. HORIZONTAL 1μs/DIV.

TYPICAL APPLICATIONS

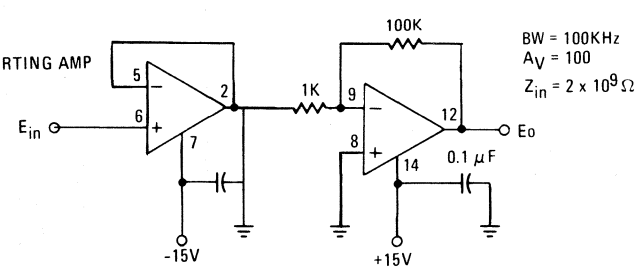
LOW COST HIGH FREQUENCY GENERATOR



ABSOLUTE-VALUE CIRCUIT



HIGH IMPEDANCE
HIGH GAIN
HIGH FREQUENCY INVERTING AMP



BW = 100KHz
A_V = 100
$Z_{in} = 2 \times 10^9 \Omega$

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
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HA-2700/2704/2705

Low Power, High Performance Operational Amplifiers

2

FEATURES

- LOW POWER DISSIPATION — 2.24mW AT ±15.0V
- HIGH SLEW RATE — 20V/μs
- HIGH OPEN LOOP GAIN — 300k(R_L = 2kΩ)
- LOW INPUT BIAS CURRENT — 5nA
- LOW OFFSET VOLTAGE — 0.5mV
- HIGH CM_{rr} — 106dB
- WIDE POWER SUPPLY RANGE — ±5.5V TO ±20.0V

APPLICATIONS

- HIGH GAIN AMPLIFIER
- INSTRUMENTATION AMPLIFIERS
- ACTIVE FILTERS
- TELEMETRY SYSTEMS
- BATTERY-POWERED EQUIPMENT

DESCRIPTION

HA-2700/2704/2705 are internally compensated operational amplifiers which employ dielectric isolation to achieve excellent DC and dynamic performance with very low quiescent power consumption.

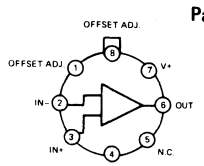
DC performance of the amplifier input is characterized by high CMRR (106dB), low offset voltage (0.5mV, HA-2700 and HA-2704; 1mV, HA-2705) along with low bias and offset current (5.0nA and 2.5nA respectively). These input specifications, in conjunction with offset null capability and open-loop gain of 300,000V/V, enable HA-2700/2704/2705 to provide accurate, high-gain signal amplification. Gain bandwidth 1MHz and slew rate of 20V/μs allow for processing of fast, wideband signals. Input and output signal amplitudes of at least ±11 volts can be accomodated while providing output drive capability of 10mA. For maximum reliability, the output is protected in the event of short circuits to ground.

These amplifiers operate from a wide range of supplies (±5.5V to ±20V) with a maximum quiescent supply drain of only 150μA. HA-2700/2704/2705 are, therefore, ideally suited to low-power instrumentation and filtering applications that require fast, accurate response over a wide range of signal frequency.

These amplifers are available in three performance grades: HA-2700 is rated for operation from -55°C to +125°C; HA-2704 is specified over -25°C to +85°C; HA-2705 is specified from 0°C to +75°C. All three devices are available in TO-99 cans or 14 lead D.I.P. packages.

PINOUT

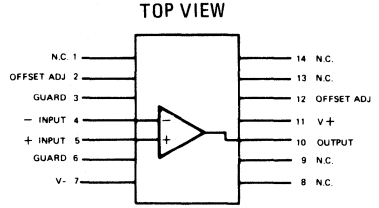
TO-99 — Package Code 2A, 4U



Case Connected to V-

TOP VIEW

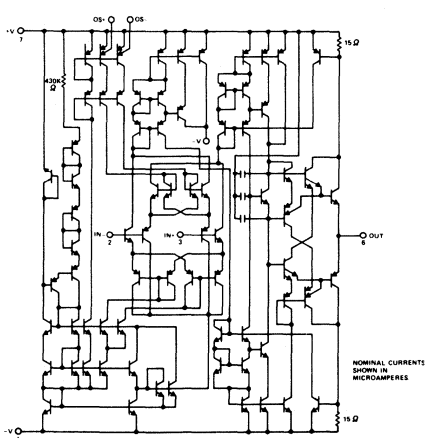
TO-116



TOP VIEW

Case Connected to V-

SCHEMATIC



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	44.0V
Differential Input Voltage	±18.0V
Internal Power Dissipation (Note 7)	300mW
Storage Temperature	$-65^oC \leq T_A \leq +150^oC$

ELECTRICAL CHARACTERISTICS

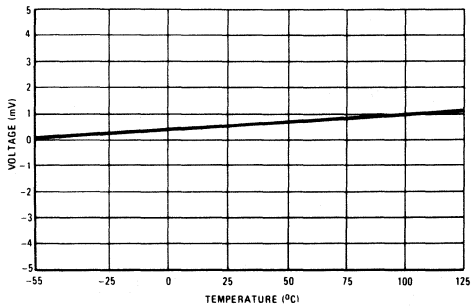
$V^+ = +15.0$ V.D.C. $V^- = -15.0$ V.D.C.

PARAMETER	TEMP.	HA-2700 −55°C to +125°C			HA-2704 −25°C to +85°C			HA-2705 0°C to +75°C			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
INPUT CHARACTERISTICS											
* Offset Voltage (Note 1)	+25°C		0.5	3.0		0.5	3.0		1.0	5.0	mV
	Full			5.0			6.0			7.0	mV
* Bias Current	+25°C		5.0	20.0		5.0	20.0		5.0	40.0	nA
	Full			50.0			50.0			70.0	nA
* Offset Current	+25°C		2.5	10.0		2.5	10.0		2.5	15.0	nA
	Full			30.0			30.0			40.0	nA
Common Mode Range	Full	±11.0			±11.0			±11.0			V
TRANSFER CHARACTERISTICS											
* Large Signal Voltage Gain (Notes 2 & 3)	+25°C	200K	300K		200K	300K		200K	300K		V/V
	Full	100K			100K			100K			V/V
* Common Mode Rejection Ratio (Note 4)	Full	86	106		86	106		80	106		dB
Gain Bandwidth Product (Note 2)	+25°C		1.0			1.0			1.0		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 2)	+25°C	±12.0	±13.0		±12.0	±13.0		±12.0	±13.0		V
	Full	±11.0			±11.0			±11.0			V
Output Current (Note 3)	+25°C		10			10			10		mA
TRANSIENT RESPONSE CHARACTERISTICS											
* Slew Rate (Notes 2 & 6)	+25°C	10	20		10	20		10	20		V/µs
POWER SUPPLY CHARACTERISTICS											
* Supply Current	+25°C		75	150		75	150		75	150	µA
* Power Supply Rejection Ratio (Note 5)	Full	86	100		86	100		80	100		dB

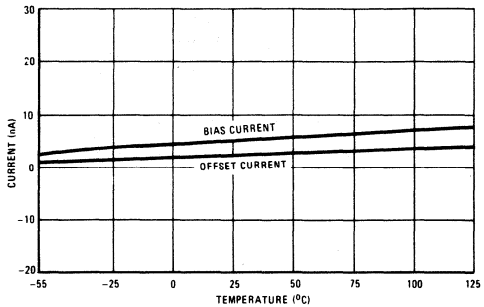
NOTES:
1. Can be adjusted to zero with 1 megohm pot between Pins 1 and 8 with the tap to Pin 7.
2. $R_L = 2K$, $C_L = 100pF$
3. $V_O = \pm 10.0V$
4. $V_{CM} = \pm 10V$
5. $V_S = \pm 10.0V$ to $\pm 20.0V$
6. $A_V = 5$
7. Derate by 6.6 mW/°C above 105°C.

*100% Tested For DASH 8

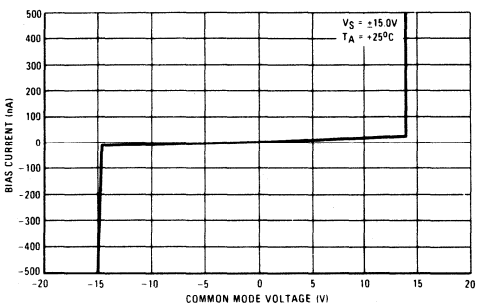
OFFSET VOLTAGE AS A FUNCTION OF TEMPERATURE



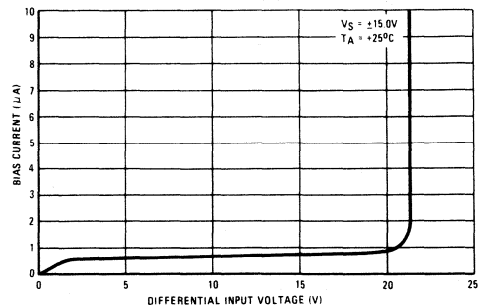
INPUT BIAS CURRENT AND OFFSET CURRENT AS A FUNCTION OF TEMPERATURE



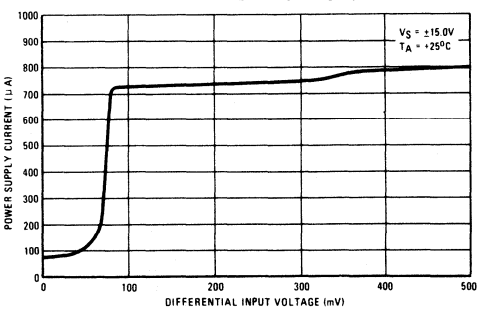
BIAS CURRENT AS A FUNCTION OF COMMON MODE VOLTAGE



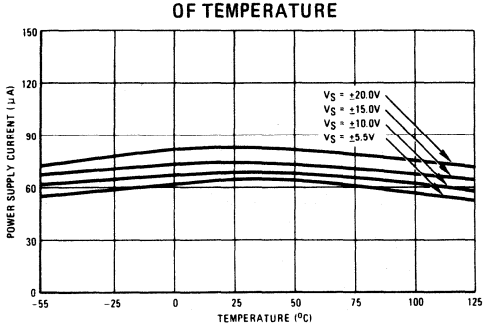
BIAS CURRENT AS A FUNCTION OF DIFFERENTIAL INPUT VOLTAGE



POWER SUPPLY CURRENT AS A FUNCTION OF DIFFERENTIAL INPUT VOLTAGE

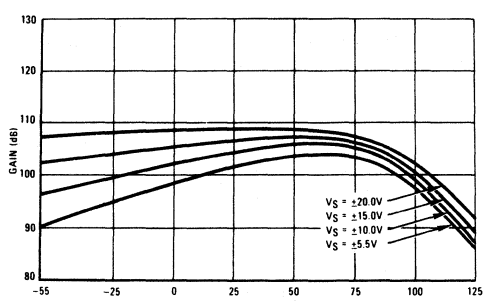


POWER SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



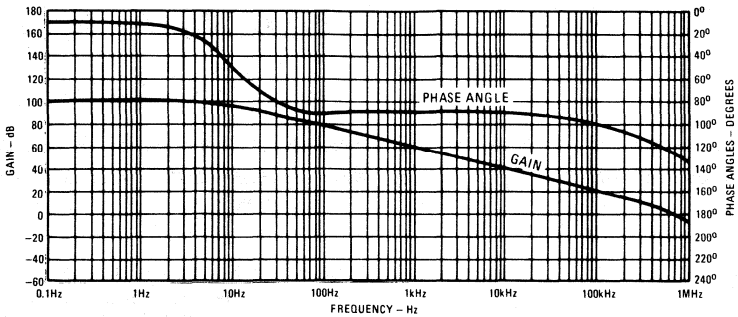
NOTE: Open loop (comparator) applications are not recommended, because of the above characteristic.

VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE



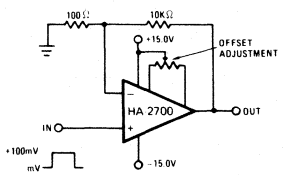
TYPICAL PERFORMANCE CURVES (continued)

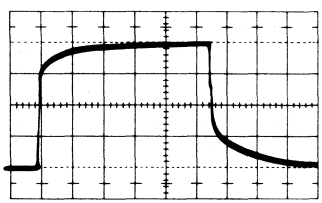
PHASE-FREQUENCY RESPONSE FOR THE HA-2700



TYPICAL APPLICATIONS

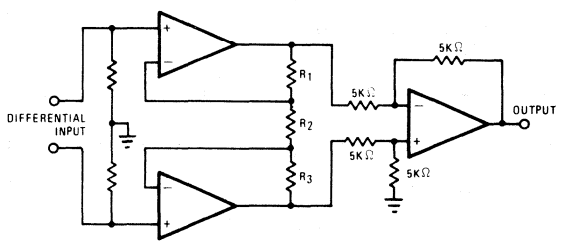
HIGH GAIN AMPLIFIER (100 V/V)





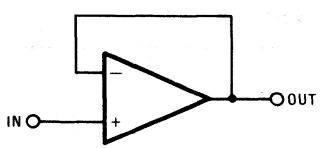
SCALE:
Horizontal – 20μs/division
Vertical – 5.0V/division

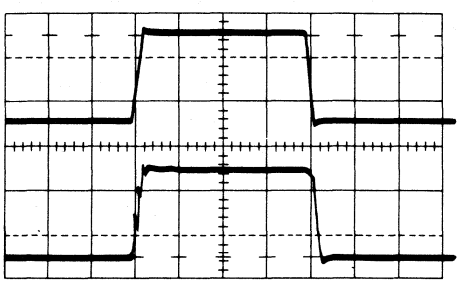
DIFFERENTIAL INPUT INSTRUMENTATION AMPLIFIER



THE GAIN IS GIVEN BY: $\frac{(R_1 + R_2 + R_3)}{R_2} = G$

UNITY GAIN VOLTAGE FOLLOWER





Non-inverting unity gain with a 2KΩ and 100pF load
TOP: V_{IN} = 10.0V Peak to Peak
BOTTOM: V_{OUT}
SCALE: Horizontal -1 μs/division
Vertical -5.0V/division

NOTE: Faster increase rise and fall time and increase distortion on output wave form.

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HA-2720/25

Wide Range Programmable Operational Amplifier

2

FEATURES

- WIDE PROGRAMMING RANGE

SLEW RATE	0.06 TO 6V/μs
BANDWIDTH	5kHz TO 10MHz
BIAS CURRENT	0.4 TO 50nA
SUPPLY CURRENT	1μA TO 1.5mA

- WIDE POWER SUPPLY RANGE ±1.2 TO ±18V
- CONSTANT AC PERFORMANCE OVER SUPPLY RANGE

APPLICATIONS

- ACTIVE FILTERS
- CURRENT CONTROLLED OSCILLATORS
- VARIABLE ACTIVE FILTERS
- MODULATORS
- BATTERY-POWERED EQUIPMENT

DESCRIPTION

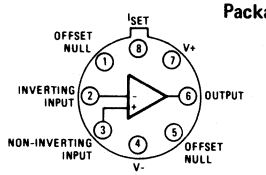
HA-2720/2725 programmable amplifiers are internally compensated monolithic devices offering a wide range of performance, that can be controlled by adjusting the circuits' "set" current (I_{SET}). By means of adjusting an external resistor or current source, power dissipation, slew rate, bandwidth, output current and input noise can be programmed to desired levels. This versatile adjustment capability enables HA-2720/2725 to provide optimum design solutions by delivering the required level of performance with minimum possible power dissipation. HA-2720 and HA-2725 can, therefore, be utilized as the standard amplifier for a variety of designs simply by adjusting their programming current.

A major advantage of HA-2720/2725 is that operating characteristics remain virtually constant over a wide supply range (±1.2V to ±15V), allowing the amplifiers to offer maximum performance in almost any system including battery-operated equipment. A primary application for HA-2720/2725 is in active filters for a wide variety of signals that differ in frequency and amplitude. Also, by modulating the "set" current, HA-2720/2725 can be used for designs such as current controlled oscillators modulators, sample and hold circuits and variable active filters.

HA-2720 is guaranteed over -55°C to +125°C. HA-2725 is specified from 0°C to +75°C. Both parts are available in TO-99 cans or dice form.

PINOUT

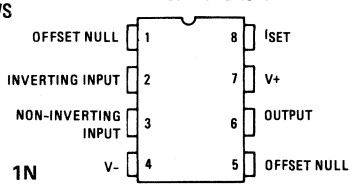
TO-99 **Package Code 2A, 1N**



2A

NOTE: Case tied to V⁻

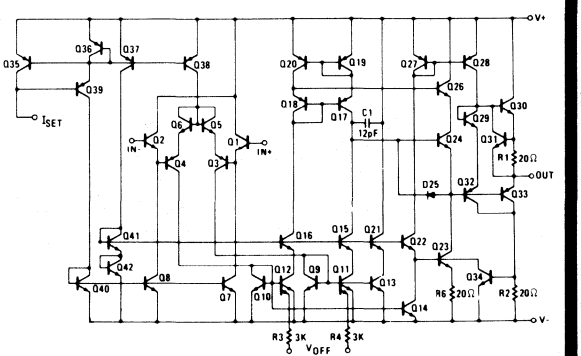
TOP VIEWS



1N

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	45.0V	Power Dissipation (Note 2)	300mW
Differential Input Voltage	±30.0V	Operating Temperature Range:	
Input Voltage (Note 1)	±15.0V	HA-2720	$-55^{o}C \leq T_A \leq +125^{o}C$
I_{SET} (Current at I_{SET})	500μA	HA-2725	$0^{o}C \leq T_A \leq +75^{o}C$
V_{SET} (Voltage to Gnd. at I_{SET})	$V+ - 2.0V \leq V_{SET} \leq V+$	Storage Temperature Range	$-65^{o}C \leq T_A \leq +150^{o}C$

ELECTRICAL CHARACTERISTICS

V+ = +3.0V, V- = -3.0V

		HA-2720 -55°C to +125°C						HA-2725 0°C to +75°C						
		I_{SET} = 1.5μA			I_{SET} = 15μA			I_{SET} = 1.5μA			I_{SET} = 15μA			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS														
*Offset Voltage	25°C		2.0	3.0		2.0	3.0		2.0	5.0		2.0	5.0	mV
	Full			5.0			5.0			7.0			7.0	mV
Offset Current	25°C		0.5	3.0		1.0	10		0.5	5.0		1.0	10	nA
	Full			7.5			20			7.5			20	nA
Bias Current	25°C		2.0	5.0		8.0	20		2.0	10		8.0	30	nA
	Full			10			40			10			40	nA
Input Resistance (Note 10)	25°C		50			5			50			5		MΩ
Input Capacitance	25°C		3.0			3.0			3.0			3.0		pF
TRANSFER CHARACTERISTICS														
*Large Signal Voltage Gain (Note 9)	25°C	20K	40K		20K	40K		15K	40K		15K	40K		V/V
	Full	15K			15K			10K			10K			V/V
*Common Mode Rejection Ratio (Note 4)	Full	80			80			74			74			dB
OUTPUT CHARACTERISTICS														
*Output Voltage Swing (Note 3)	25°C	±2.0	±2.2		±2.0	±2.2		±2.0	±2.2		±2.0	±2.2		V
	Full	±2.0			±1.9			±2.0			±2.0			V
Output Current (Note 5)	25°C		±0.2			±2.0			±0.2			±2.0		mA
Output Resistance	25°C		2K			500			2K			500		Ω
Output Short-Circuit Current	25°C		2.8			14			2.8			14		mA
TRANSIENT RESPONSE														
Rise Time (Note 6)	25°C		2.5			0.25			2.5			0.25		μs
Overshoot (Note 6)	25°C		5			10			5			10		%
Slew Rate (Note 7)	25°C		0.07			0.70			0.07			0.70		V/μs
POWER SUPPLY CHARACTERISTICS														
Supply Current	25°C		15			170			15			170		μA
	Full			20			200			20			200	μA
*Power Supply Rejection Ratio (Note 8)	Full	100			100			150			150			μV/V

*100% Tested For DASH 8

ELECTRICAL CHARACTERISTICS

V+ = +15.0V, V- = -15.0V

PARAMETER	TEMP.	HA-2720 -55°C to +125°C						HA-2725 0°C to +75°C						UNITS
		I_{SET} = 1.5μA			I_{SET} = 15μA			I_{SET} = 1.5μA			I_{SET} = 15μA			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
INPUT CHARACTERISTICS														
*Offset Voltage	25°C		2.0	3.0		2.0	3.0		2.0	5.0		2.0	5.0	mV
	Full			5.0			5.0			7.0			7.0	mV
*Offset Current	25°C		0.5	3.0		1.0	10		0.5	5.0		1.0	10	nA
	Full			7.5			20			7.5			20	nA
*Bias Current	25°C		2.0	5.0		8.0	20		2.0	10		8.0	30	nA
	Full			10			40			10			40	nA
Input Resistance (Note 10)	25°C		50			5			50			5		MΩ
Input Capacitance	25°C		3.0			3.0			3.0			3.0		pF
TRANSFER CHARACTERISTICS														
*Large Signal Voltage Gain (Notes 3 & 9)	25°C	40K	100K		40K	120K		25K	100K		25K	120K		V/V
	Full	25K			25K			20K			20K			V/V
*Common Mode Rejection Ratio (Note 4)	25°C		90			90			90			90		dB
	Full	80			80			74			74			dB
OUTPUT CHARACTERISTICS														
*Output Voltage Swing (Note 3)	25°C	±12	±13.5		±12	±13.5		±12	±13.5		±12	±13.5		V
	Full	±10			±10			±10			±10			V
Output Current (Note 5)	25°C		±0.5			±5.0			±0.5			±5.0		mA
Output Resistance	25°C		2K			500			2K			500		Ω
Output Short-Circuit Current	25°C		3.7			19			3.7			19		mA
TRANSIENT RESPONSE														
Rise Time (Note 6)	25°C		2.0			0.2			2.0			0.2		μs
Overshoot (Note 6)	25°C		5			15			5			15		%
Slew Rate (Note 7)	25°C		0.1			0.8			0.1			0.8		V/μs
POWER SUPPLY CHARACTERISTICS														
*Supply Current	25°C		20			210			20			210		μA
	Full			25			250			25			250	μA
*Power Supply Rejection Ratio (Note 8)	Full	100			100			150			150			μV/V

NOTES:
1. For supply voltages less than ±15.0V, the absolute maximum input voltage is equal to supply voltage.
2. Derate at 6.8mW/°C for operation ambient temperatures above 75°C.

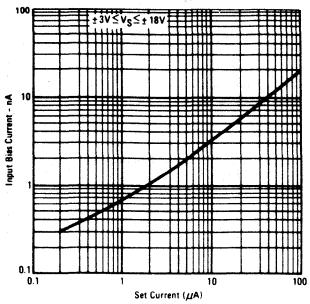
	V_{SUPPLY} = ±3.0V	V_{SUPPLY} = ±15.0V	I_{SET} = 1.5μA	I_{SET} = 15μA
3.	T = +25°C and Full	T = +25°C	R_L = 75KΩ	R_L = 5KΩ
	—	T = Full	R_L = 75KΩ	R_L = 75KΩ
4.	V_{CM} = ±1.5V	V_{CM} = ±5.0V		
5.	V_O = ±2.0V	V_O = ±10.0V		
6.	← A_V = +1, V_{IN} = 400mV, R_L = 5K, C_L = 100pF →			
7.	V_O = ±2.0V	V_O = ±10.0V	R_L = 20K	R_L = 5K
8.	ΔV = ±1.5V	ΔV = ±5.0V		
9.	V_O = ±1.0V	V_O = ±10.0V		

10. This parameter based upon design calculations.

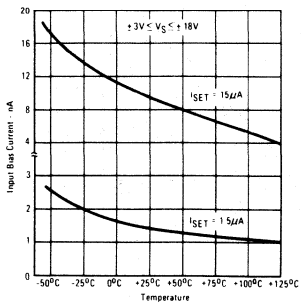
*100% Tested For DASH 8

UNLESS OTHERWISE NOTED: $T_A = +25^oC$, $V_S = \pm 15VDC$

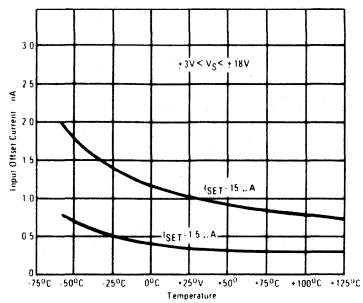
INPUT BIAS CURRENT
vs. SET CURRENT



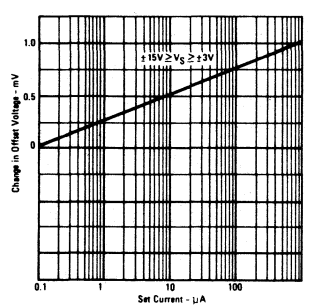
INPUT BIAS CURRENT
vs. TEMPERATURE



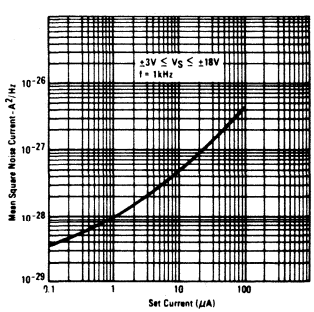
INPUT OFFSET CURRENT
vs. TEMPERATURE



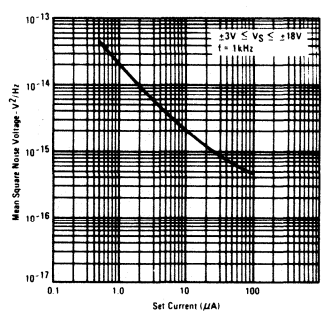
CHANGE IN OFFSET VOLTAGE
vs. I_{SET} (UNNULLED)



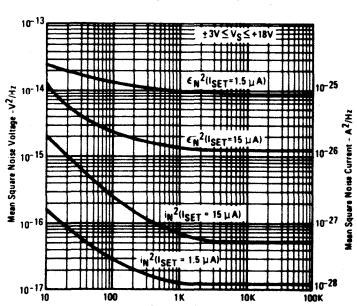
INPUT NOISE CURRENT
vs. I_{SET}



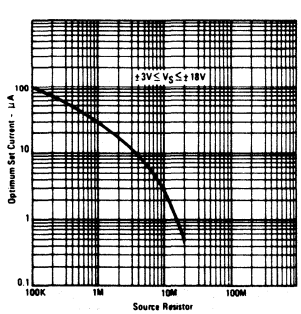
INPUT NOISE VOLTAGE
vs. I_{SET}



INPUT NOISE VOLTAGE AND CURRENT
vs. FREQUENCY



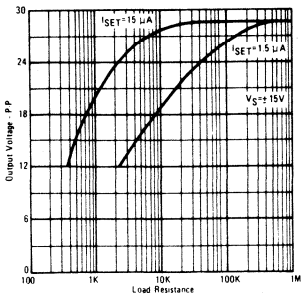
OPTIMUM SET CURRENT FOR MINIMUM
NOISE vs. SOURCE RESISTOR



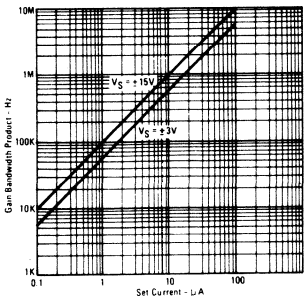
2

UNLESS OTHERWISE NOTED: $T_A = +25^oC$, $V_S = \pm 15VDC$

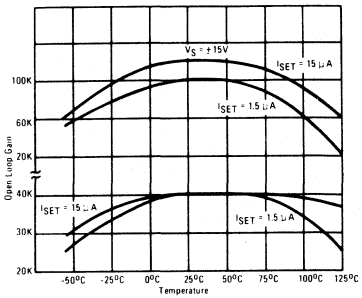
MAXIMUM OUTPUT VOLTAGE SWING
vs. LOAD RESISTANCE



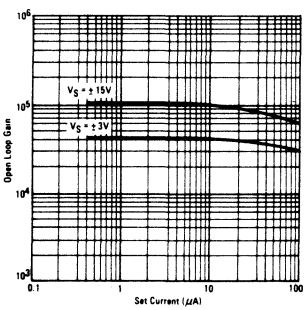
GAIN BANDWIDTH PRODUCT
vs. I_{SET}



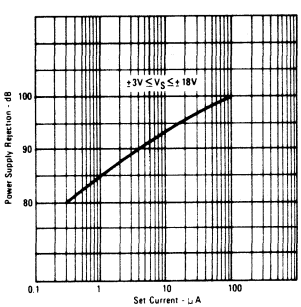
OPEN LOOP VOLTAGE GAIN
vs. TEMPERATURE



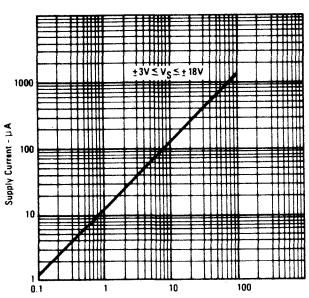
OPEN LOOP VOLTAGE GAIN
vs. I_{SET}



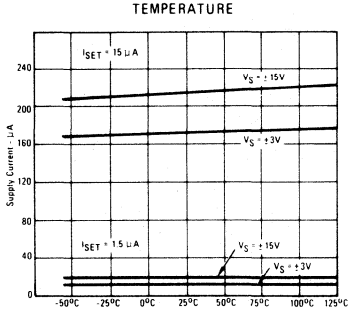
POWER SUPPLY REJECTION
vs. I_{SET}



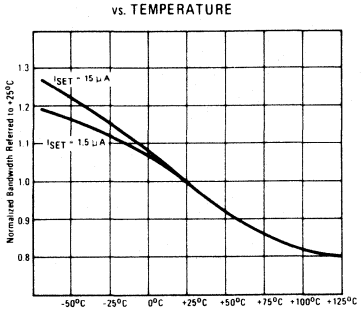
STANDBY SUPPLY CURRENT
vs. I_{SET}



SUPPLY CURRENT vs.
TEMPERATURE

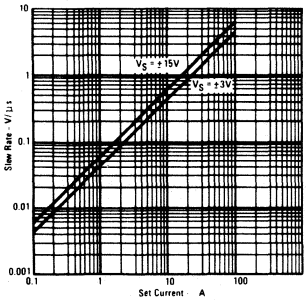


NORMALIZED BANDWIDTH
vs. TEMPERATURE

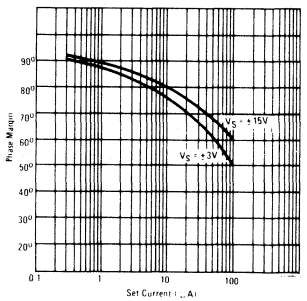


PERFORMANCE CURVES

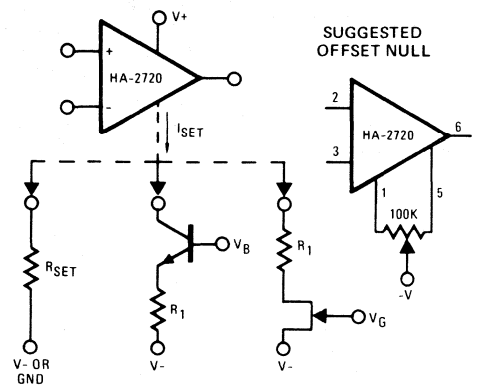
SLEW RATE vs. I_{SET}



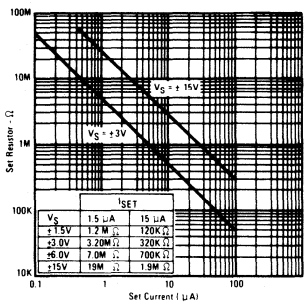
PHASE MARGIN vs. SET CURRENT



TYPICAL BIASING CIRCUITS

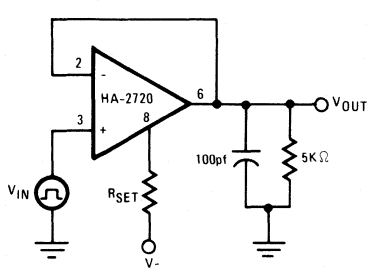


SET CURRENT VS. SET RESISTOR

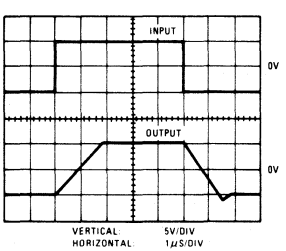


I_{SET}		
V_S	1.5 µA	15 µA
± 1.5V	1.2 MΩ	120KΩ
±3.0V	3.20MΩ	320KΩ
±6.0V	7.0MΩ	700KΩ
±15V	19MΩ	1.9MΩ

TRANSIENT RESPONSE/SLEW RATE CIRCUIT



SLEWING WAVEFORM



2

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HA-2730/35

Wide Range Dual Programmable Operational Amplifier

2

FEATURES

- WIDE PROGRAMMING RANGE

SET CURRENT	0.1 TO 100μA
SLEW RATE	0.06 TO 6V/μs
BANDWIDTH	5kHz TO 10MHz
BIAS CURRENT	0.4 TO 50nA
SUPPLY CURRENT	1μA TO 1.5mA

- WIDE POWER SUPPLY RANGE $^{+}$1.2 TO $^{+}$18V
- CONSTANT AC PERFORMANCE OVER SUPPLY RANGE

APPLICATIONS

- ACTIVE FILTERS
- CURRENT CONTROLLED OSCILLATORS
- VARIABLE ACTIVE FILTERS
- MODULATORS
- BATTERY-POWERED EQUIPMENT

DESCRIPTION

HA-2730/2735 Dual Programmable Amplifiers are internally compensated monolithic devices offering a wide range of performance, that can be controlled by adjusting the circuits' "set" current (I_{SET}). By means of adjusting an external resistor or current source, power dissipation, slew rate, bandwidth, output current and input noise can be programmed to desired levels. Each amplifier on the chip can be adjusted independently. This versatile adjustment capability enables HA-2730/2735 to provide optimum design solutions by delivering the required level of performance with minimum possible power dissipation. HA-2730/2735 can, therefore, be utilized as the standard amplifier for a variety of designs simply by adjusting their programming current.

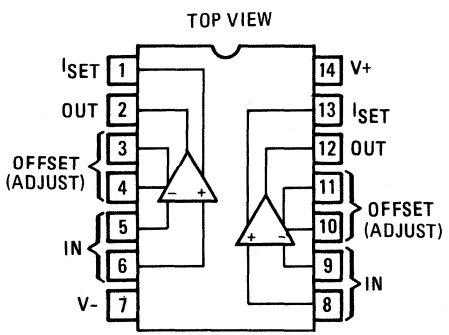
A major advantage of HA-2730/2735 is that operating characteristics remain virtually constant over a wide supply range (±1.2V to ±15V), allowing the amplifiers to offer maximum performance in almost any system including battery-operated equipement. A primary application for HA-2730/2735 is in active filters for a wide variety of signals that differ in frequency and amplitude. Also, by modulating the "set" current, HA-2730/2735 can be used for designs such as current controlled oscillators, modulators, sample and hold circuits and variable active filters.

HA-2730 is guaranteed over -55°C to +125°C. HA-2735 is specified from 0°C to +75°C. Both parts are available in 14 lead D.I.P. package or dice form.

PINOUT

Package Code 4D

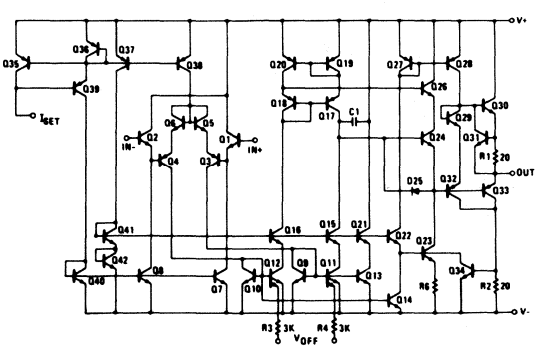
TOP VIEW



NOTE: Bottom of package is connected to V-.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

SCHEMATIC



(ONE HALF ONLY)
HA-2730/35

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	45.0V	Power Dissipation (Note 2)	500mW
Differential Input Voltage	±30.0V	Operating Temperature Range:	
Input Voltage (Note 1)	±15.0V	HA-2730	$-55^{o}C \leq T_A \leq +125^{o}C$
I_{SET} (Current at I_{SET})	500μA	HA-2735	$0^{o}C \leq T_A \leq +75^{o}C$
V_{SET} (Voltage to Gnd. at I_{SET})	$V+ - 2.0V \leq V_{SET} \leq V+$	Storage Temperature Range	$-65^{o}C \leq T_A \leq +150^{o}C$

ELECTRICAL CHARACTERISTICS (Each Side)

V+ = +3.0V, V- = -3.0V

		HA-2730 $-55^{o}C$ to $+125^{o}C$						HA-2735 $0^{o}C$ to $+75^{o}C$						
		I_{SET} = 1.5μA			I_{SET} = 15μA			I_{SET} = 1.5μA			I_{SET} = 15μA			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS														
*Offset Voltage	25°C		2.0	3.0		2.0	3.0		2.0	5.0		2.0	5.0	mV
	Full			5.0			5.0			7.0			7.0	mV
Offset Current	25°C		0.5	3.0		1.0	10		0.5	5.0		1.0	10	nA
	Full			7.5			20			7.5			20	nA
Bias Current	25°C		2.0	5.0		8.0	20		2.0	10		8.0	30	nA
	Full			10			40			10			40	nA
Input Resistance (Note 10)	25°C		50			5			50			5		MΩ
Input Capacitance	25°C		3.0			3.0			3.0			3.0		pF
TRANSFER CHARACTERISTICS														
*Large Signal Voltage Gain (Notes 3 & 9)	25°C	20K	40K		20K	40K		15K	40K		15K	40K		V/V
	Full	15K			15K			10K			10K			V/V
*Common Mode Rejection Ratio (Note 4)	Full	80			80			74			74			dB
OUTPUT CHARACTERISTICS														
*Output Voltage Swing (Note 3)	25°C	±2.0	±2.2		±2.0	±2.2		±2.0	±2.2		±2.0	±2.2		V
	Full	±2.0			±1.9			±2.0			±2.0			V
Output Current (Note 5)	25°C		±0.2			±2.0			±0.2			±2.0		mA
Output Resistance	25°C		2K			500			2K			500		Ω
Output Short-Circuit Current	25°C		2.8			14			2.8			14		mA
TRANSIENT RESPONSE														
Rise Time (Note 6)	25°C		2.5			0.25			2.5			0.25		μs
Overshoot (Note 6)	25°C		5			10			5			10		%
Slew Rate (Note 7)	25°C		0.07			0.70			0.07			0.70		V/μs
POWER SUPPLY CHARACTERISTICS														
*Supply Current (Each Amp)	25°C		15			170			15			170		μA
	Full			20			200			20			200	μA
*Power Supply Rejection Ratio (Note 8)	Full	100			100			150			150			μV/V

*100% Tested For DASH 8

ELECTRICAL CHARACTERISTICS (Each Side)

V+ = +15.0V, V- = -15.0V

PARAMETER	TEMP.	HA-2730 -55°C to +125°C						HA-2735 0°C to +75°C						UNITS
		I_{SET} = 1.5μA			I_{SET} = 15μA			I_{SET} = 1.5μA			I_{SET} = 15μA			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
INPUT CHARACTERISTICS														
*Offset Voltage	25°C		2.0	3.0		2.0	3.0		2.0	5.0		2.0	5.0	mV
	Full			5.0			5.0			7.0			7.0	mV
*Offset Current	25°C		0.5	3.0		1.0	10		0.5	5.0		1.0	10	nA
	Full			7.5			20			7.5			20	nA
*Bias Current	25°C		2.0	5.0		8.0	20		2.0	10		8.0	30	nA
	Full			10			40			10			40	nA
Input Resistance (Note 10)	25°C		50			5			50			5		MΩ
Input Capacitance	25°C		3.0			3.0			3.0			3.0		pF
TRANSFER CHARACTERISTICS														
* Large Signal Voltage Gain (Notes 3 & 9)	25°C	40K	100K		40K	120K		25K	100K		25K	120K		V/V
	Full	25K			25K			20K			20K			V/V
*Common Mode Rejection Ratio (Note 4)	25°C		90			90			90			90		dB
	Full	80			80			74			74			dB
OUTPUT CHARACTERISTICS														
*Output Voltage Swing (Note 3)	25°C	±12	±13.5		±12	±13.5		±12	±13.5		±12	±13.5		V
	Full	±10			±10			±10			±10			V
Output Current (Note 5)	25°C		±0.5			±5.0			±0.5			±5.0		mA
Output Resistance	25°C		2K			500			2K			500		Ω
Output Short-Circuit Current	25°C		3.7			19			3.7			19		mA
TRANSIENT RESPONSE														
Rise Time (Note 6)	25°C		2.0			0.2			2.0			0.2		μs
Overshoot (Note 6)	25°C		5			15			5			15		%
Slew Rate (Note 7)	25°C		0.1			0.8			0.1			0.8		V/μs
POWER SUPPLY CHARACTERISTICS														
*Supply Current (Each Amp)	25°C		20			210			20			210		μA
	Full			25			250			25			250	μA
*Power Supply Rejection Ratio (Note 8)	Full	100			100			150			150			μV/V

NOTES:
1. For supply voltages less than ±15.0V, the absolute maximum input voltage is equal to supply voltage.
2. Derate at 4.7mW/°C at ambient temperatures above 68°C.

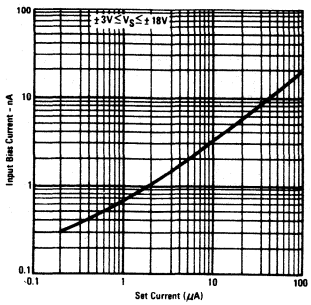
	V_{SUPPLY} = ±3.0V	V_{SUPPLY} = ±15.0V	I_{SET} = 1.5μA	I_{SET} = 15μA
3.	T = +25°C and Full	T = +25°C	R_L = 75KΩ	R_L = 5KΩ
	—	T = Full	R_L = 75KΩ	R_L = 75KΩ
4.	V_{CM} = ±1.5V	V_{CM} = ±5.0V		
5.	V_O = ±2.0V	V_O = ±10.0V		
6.	← A_V = +1, V_{IN} = 400mV, R_L = 5K, C_L = 100pF →			
7.	V_O = ±2.0V	V_O = ±10.0V	RR_L = 20K	R_L = 5K
8.	ΔV = ±1.5V	ΔV = ±5.0V		
9.	V_O = ±1.0V	V_O = ±10.0V		

10. This parameter value based upon design calculations.

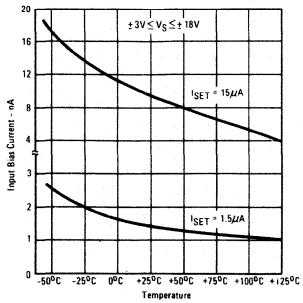
*100% Tested For DASH 8

UNLESS OTHERWISE NOTED: $T_A = 25^oC$, $V_S = \pm 15VDC$

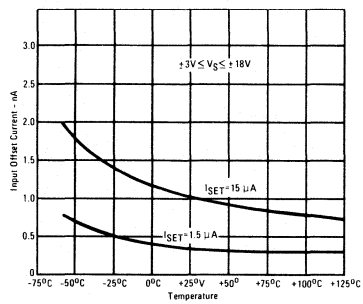
INPUT BIAS CURRENT
vs. SET CURRENT



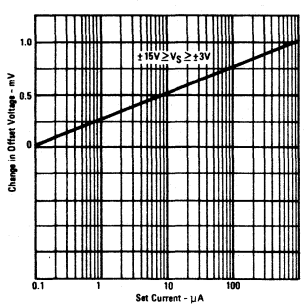
INPUT BIAS CURRENT
vs. TEMPERATURE



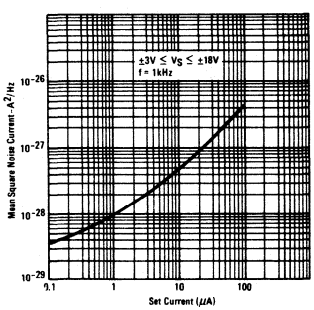
INPUT OFFSET CURRENT
vs. TEMPERATURE



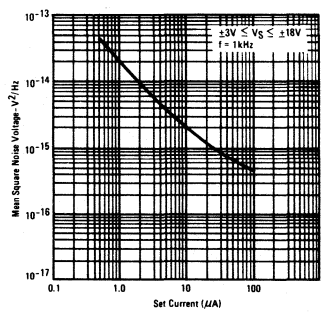
CHANGE IN OFFSET VOLTAGE
vs. I_{SET} (UNNULLED)



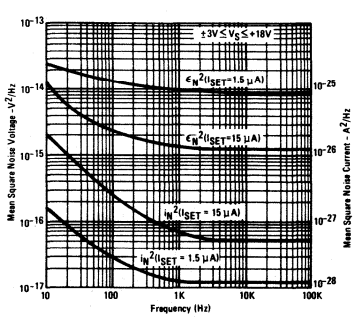
INPUT NOISE CURRENT
vs. I_{SET}



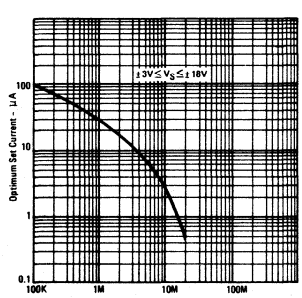
INPUT NOISE VOLTAGE
vs. I_{SET}



INPUT NOISE VOLTAGE AND CURRENT
vs. FREQUENCY



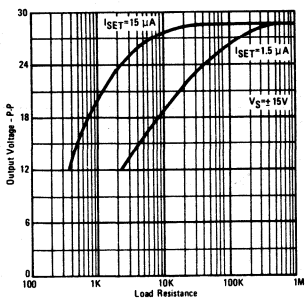
OPTIMUM SET CURRENT FOR MINIMUM
NOISE vs. SOURCE RESISTOR



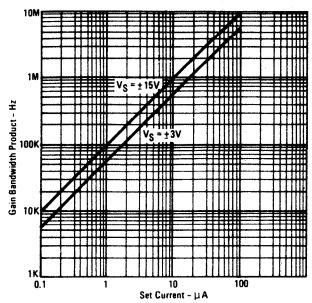
2

UNLESS OTHERWISE NOTED: $T_A = 25^0C$, $V_S = \pm 15VDC$

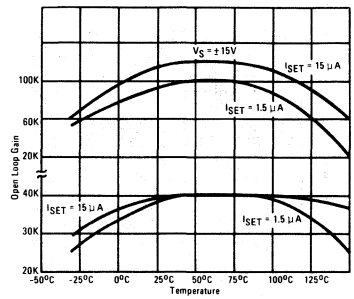
MAXIMUM OUTPUT VOLTAGE SWING
vs. LOAD RESISTANCE



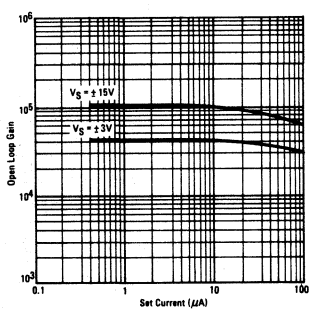
GAIN BANDWIDTH PRODUCT
vs. I_{SET}



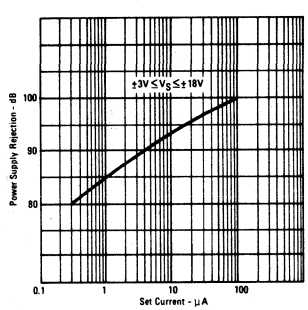
OPEN LOOP VOLTAGE GAIN
vs. TEMPERATURE



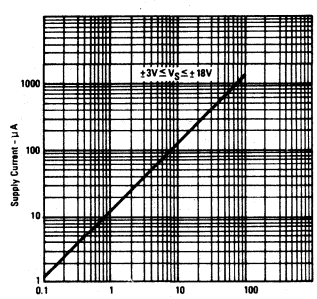
OPEN LOOP VOLTAGE GAIN
vs. I_{SET}



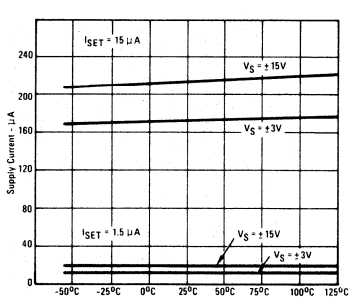
POWER SUPPLY REJECTION
vs. I_{SET}



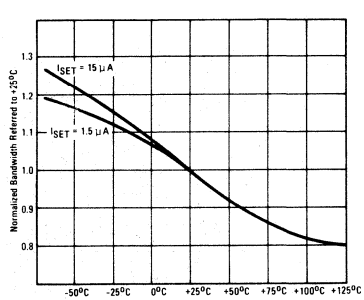
STANDBY SUPPLY CURRENT
vs. I_{SET}



SUPPLY CURRENT vs.
TEMPERATURE

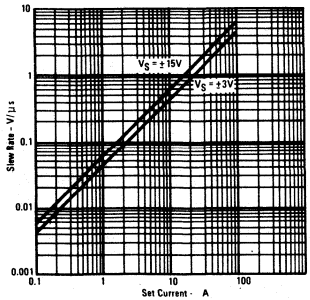


NORMALIZED BANDWIDTH
vs. TEMPERATURE

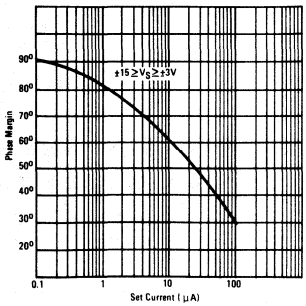


PERFORMANCE CURVES

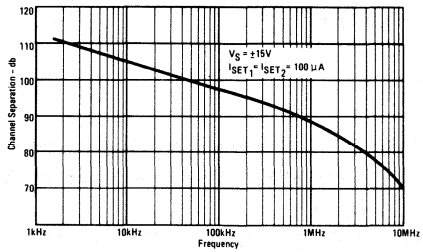
SLEW RATE vs. I_{SET}



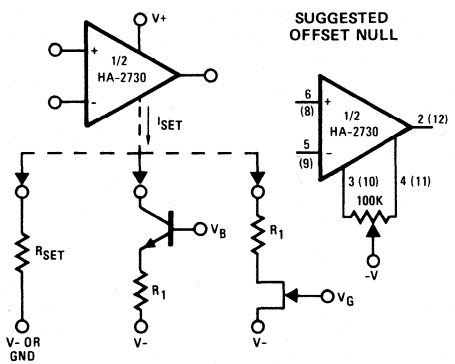
PHASE MARGIN vs. SET CURRENT



CHANNEL SEPARATION vs. FREQUENCY

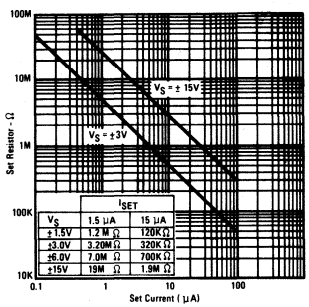


TYPICAL BIASING CIRCUITS



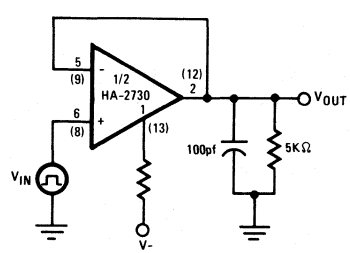
NOTE: Numbers in parenthsis refer to the second half.

SET CURRENT VS. SET RESISTOR



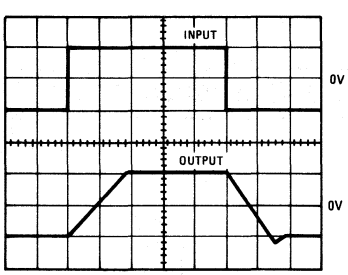
V_S	I_{SET} 1.5 µA	I_{SET} 15 µA
±1.5V	1.2 MΩ	120KΩ
±3.0V	3.20MΩ	320KΩ
±6.0V	7.0MΩ	700KΩ
±15V	19MΩ	1.9MΩ

TRANSIENT RESPONSE/SLEW RATE CIRCUIT



NOTE: Numbers in parenthsis refer to the second half.

SLEWING WAVEFORM



VERTICAL: 5V/DIV
HORIZONTAL: 1µS/DIV
I_{SET} = 100µA

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HA-2900/04/05

Chopper Stabilized Operational Amplifier

2

FEATURES

- OFFSET VOLTAGE DRIFT — 0.2 μV/^{o}C
- OFFSET CURRENT DRIFT — 1pA/^{o}C
- OPEN LOOP GAIN — 5 x 10^{8}
- BANDWIDTH — 3MHz
- SLEW RATE — 2.5V/μs
- TRUE DIFFERENTIAL INPUTS

APPLICATIONS

- HIGH-GAIN DC INSTRUMENTATION
- HIGH-ACCURACY WEIGHING EQUIPMENT
- BIOMEDICAL AMPLIFIERS
- PRECISION INTEGRATORS AND TIMERS

DESCRIPTION

HA-2900/2904/2905 are monolithic chopper-stabilized operational amplifiers that employ dielectric isolation achieving superior offset drift, extremely low input currents and excellent AC performance. Input drift is characterized by offset voltage drift of 0.2 μ V/^{o}C and offset current drift of 1pA/^{o}C. Initial offset voltage is only 20 μV while offset current is 50pA. These input specifications make HA-2900/2904/2905 ideally suited to high accuracy applications such as high-gain DC instrumentation, and precision integration. The amplifiers can be used to replace other op amps in designs where much lower errors are required without external adjustments. 3MHz gain-bandwidth product makes HA-2900/2904/2905 valuable for processing wide band signals as well as for low frequency measurements.

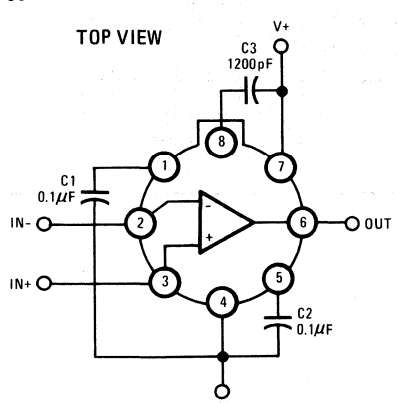
In addition to offering high-accuracy performance, these "choppers" also offer versatility by virtue of their symmetrical, differential inputs which permit operation in any op amp configuration – inverting, non-inverting or balanced. These devices require only three external capacitors for proper operation.

HA-2900 is guaranteed over -55^{o}C to +125^{o}C; HA-2904 operates from -25^{o}C to +85^{o}C; HA-2905 operates from 0^{o}C to +75^{o}C. All devices are available in a hermetically sealed metal can.

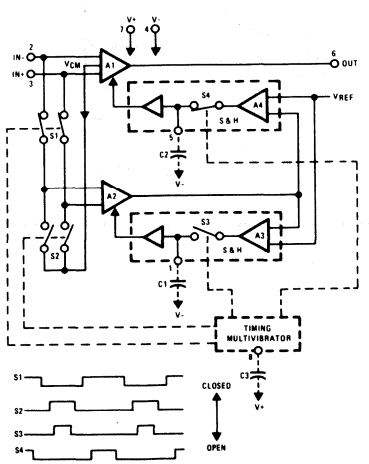
PINOUT AND SUGGESTED HOOKUP

TO-99 — **Package Code 2E**

TOP VIEW



FUNCTIONAL DIAGRAM



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	42.0V	Operating Temperature Range	$-55^{o}C \leq T_A \leq +125^{o}C$ (HA-2900)
Differential Input Voltage (Note 1)	±15V		$-25^{o}C \leq T_A \leq +85^{o}C$ (HA-2904)
Output Current/Full Short Circuit Protection		Storage Temperature Range	$0^{o}C \leq T_A \leq +75^{o}C$ (HA-2905)
Internal Power Dissipation	300mW*		$-65^{o}C \leq T_A \leq +150^{o}C$

*Derate by 6.6mW/°C above +105°C

ELECTRICAL CHARACTERISTICS

Test Conditions: C1 = C2 = 0.1μF, C3 = 1200pF, V_{Supply} = ±15.0V unless otherwise specified.

		HA-2900 -55°C to +125°C			HA-2904 -25°C to +85°C			HA-2905 0°C to +75°C			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS											
Offset Voltage	+25°C		20	60		20			20		μV
	Full			100			50			80	μV
Offset Voltage Average Drift	Full		0.3	0.6		0.2	0.4		0.2		μV/°C
Bias Current	+25°C		150	1,000		150			150		pA
	Full			1,500			1,000			1,000	pA
Offset Current	+25°C		50	500		50			50		pA
	Full			800			500			500	pA
Offset Current Average Drift	Full		1	4		1	3		1		pA/°C
Input Resistance	+25°C		100			100			100		MΩ
Input Capacitance	+25°C		10			10			10		pF
Common Mode Range	Full	±10			±10			±10			V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Note 2, 5)	+25°C		$5x10^8$			5×10^8			5×10^8		V/V
	Full	10^6			10^6			10^6			V/V
Chopper Frequency	+25°C		750			750			750		Hz
Common Mode Rejection Ratio (Note 3)	+25°C	120	160		120	160		120	160		dB
	Full	110									
Gain Bandwidth Product (Note 4)	+25°C		3			3			3		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 2)	Full	±10	±12		±10	±12		±10	±12		V
Output Current	+25°C	±10			±10			±7			mA
Output Resistance	Full		200			200			200		Ω
Full Power Bandwidth (Note 5)	+25°C		40			40			40		kHz
TRANSIENT RESPONSE (NOTES 2, 8, and 9)											
Rise Time (Note 6)	+25°C		200			200			200		ns
Overshoot (Note 6)	+25°C		20			20			20		%
Slew Rate (Note 10)	+25°C		2.5			2.5			2.5		V/μs
POWER SUPPLY CHARACTERISTICS											
Supply Current	+25°C		3.5	5.0		3.5	5.0		3.5	5.0	mA
Supply Voltage Range	Full	±12		±20	±10		±20	±12		±20	V
Power Supply Rejection Ratio (Note 7)	+25°C	120	160		120	160		120	160		dB
	Full	110									

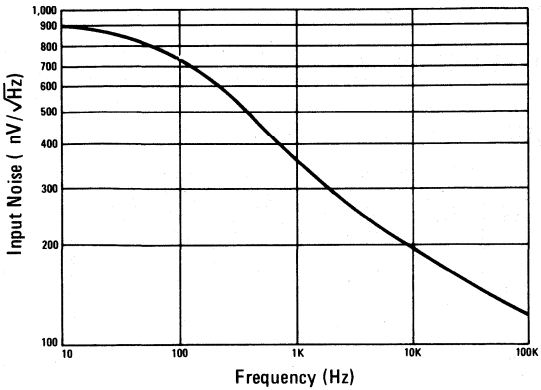
NOTES:
1. Input terminals should be protected against static discharge during handling and installation. Input voltage should never exceed supply voltages.
2. R_L = 2K
3. V_{CM} = ±5.0V
4. A_V = 10
5. V_O = ±10V
6. V_O = ±200mV
7. ΔV_S = ±5V
8. C_L = 50pF
9. A_V = +1 See transient response test circuits and waveforms, page 4.
10. V_{OUT} = ±5V

*100% Tested For DASH 8

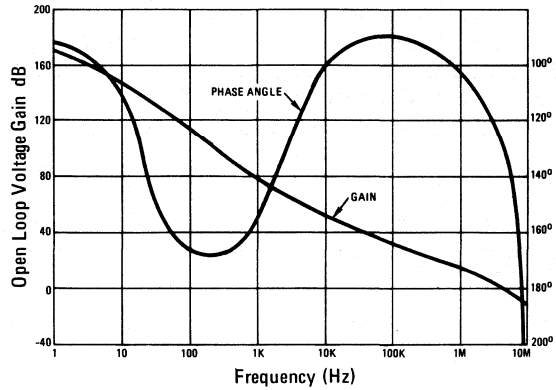
PERFORMANCE CURVES

V+ = V- = 15VDC, T_A = 25°C UNLESS OTHERWISE STATED

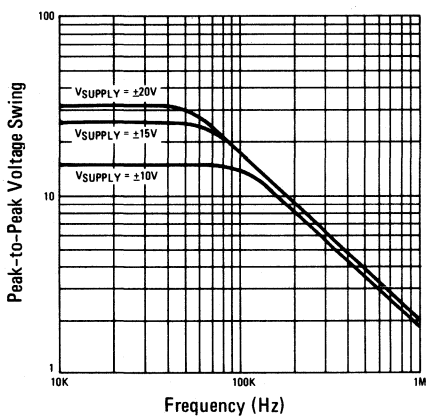
INPUT VOLTAGE NOISE



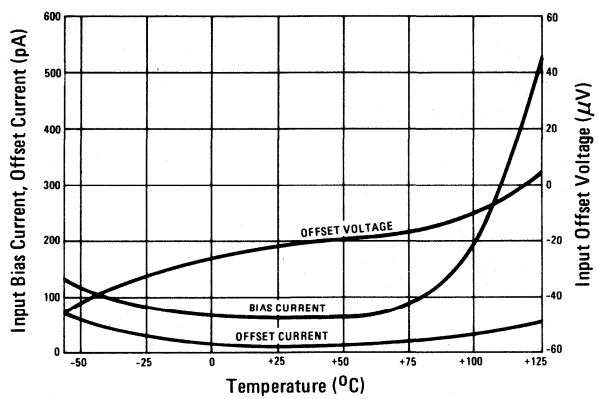
OPEN LOOP FREQUENCY AND PHASE RESPONSE



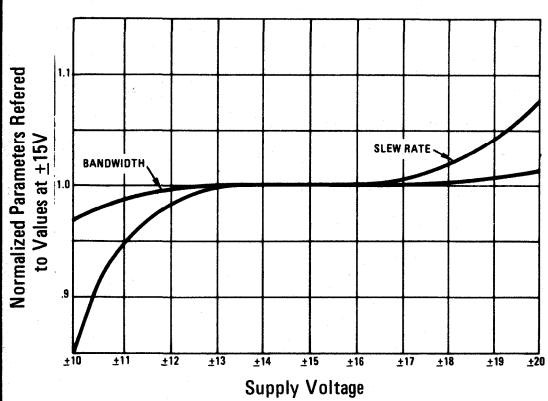
OUTPUT VOLTAGE SWING vs. FREQUENCY



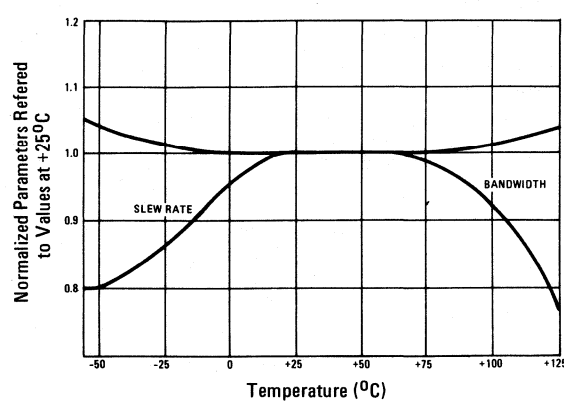
TYPICAL INPUT CHARACTERISTICS vs. TEMPERATURE



NORMALIZED A.C. PARAMETERS vs. SUPPLY VOLTAGE

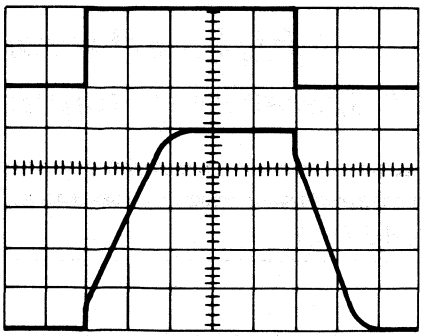


NORMALIZED A.C. PARAMETERS vs. TEMPERATURE



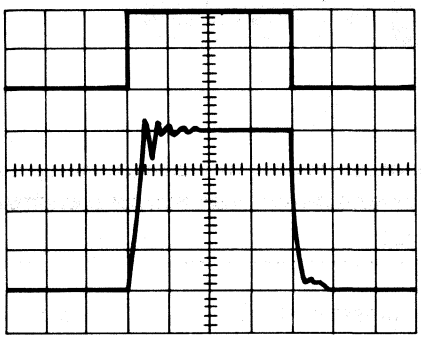
PERFORMANCE CURVES (continued)

VOLTAGE FOLLOWER
SLEWING WAVEFORM



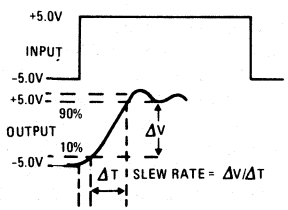
Upper Trace: Input: 5V/Div.
Lower Trace: Output; 2V/Div.
Horizontal: 2μS/Div.

VOLTAGE FOLLOWER
TRANSIENT RESPONSE WAVEFORM

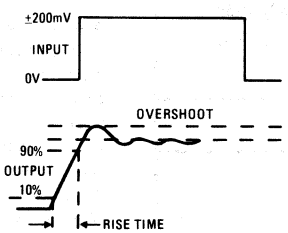


Upper Trace: Input; 100mV/Div.
Lower Trace: Output; 50mV/Div.
Horizontal: 500ns/Div.

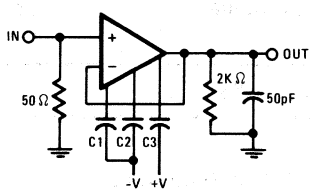
SLEW RATE



TRANSIENT RESPONSE



SLEW RATE AND
TRANSIENT RESPONSE



NOTE: Measured on both positive and negative transitions.

APPLICATION TIPS

(1) Device inputs should be protected against exceeding either supply voltage from static discharge or inadvertent connection, particularly when wired directly to a connector or instrument panel.

(2) External capacitors C1, C2, and C3 should have good temperature stability, low leakage, and low dielectric absorption. Polystyrene (below +85°C), teflon types or polycarbonate are recommended. C3 could also be silver mica.

(3) Particular care must be exercised in system layout and material and component selection to realize the full performance potential of the HA-2900/2904/2905. External sources of drift error may include the thermocouple and electrochemical EMF's generated at junctions of dissimilar metals, leakage across insulating materials, static charges created by moving air, and improper grounding and shielding practices.

(4) Chopper noise is present chiefly as a common mode input current signal, and may be minimized by matching the impedances at the two inputs. Random noise may be reduced at the expense of bandwidth using active or passive filtering.

(5) Input frequencies near the chopper frequency (750Hz) or its harmonics may result in small components of difference frequency in the output. This effect should be checked in the individual application, and if objectionable, a low pass filter may be added in series with the input.

(6) When operating at closed loop gains between 70 dB and 140 dB, compensation networks may be required, because of open loop phase shift in this gain region. In most cases, a capacitor placed in parallel with the feedback resistor to yield a gain-bandwidth product < 2MHz will be sufficient.

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HA-4602/4605

High Performance Quad Operational Amplifier

2

FEATURES

- LOW OFFSET VOLTAGE 0.3mV
- HIGH SLEW RATE ±4V/μs
- WIDE BANDWIDTH 8MHz
- LOW DRIFT 2μV/°C
- FAST SETTLING (0.01%, 10V STEP) 4.2μs
- LOW POWER CONSUMPTION 35mW/AMP
- SUPPLY RANGE ±5V TO ±20V

APPLICATIONS

- HIGH Q, WIDE BAND FILTERS
- INSTRUMENTATION AMPLIFIERS
- AUDIO AMPLIFIERS
- DATA ACQUISITION SYSTEMS
- INTEGRATORS
- ABSOLUTE VALUE CIRCUITS
- TONE DETECTORS

DESCRIPTION

The HA-4602 and HA-4605 are high performance dielectrically isolated monolithic quad operational amplifiers with superior specifications not previously available in a quad amplifier. These amplifiers offer excellent dynamic performance coupled with low values for offset voltage and drift, input noise voltage and power consumption.

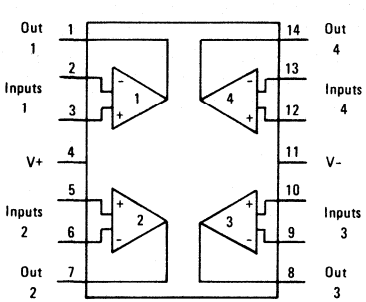
A wide range of applications can be achieved by using the features made available by the HA-4602/4605. With wide bandwidth (8MHz), low power (35mW/amp), and internal compensation, these devices are ideally suited for precision active filter designs. For audio applications these amplifiers offer low noise ($8nV/\sqrt{Hz}$) and excellent full power bandwidth (60kHz). The HA-4602/4605 is particularly useful in designs requiring low offset voltage (0.3mV) and drift (2 μV/°C), such as instrumentation and signal conditioning circuits. The high slew rate (4V/μs) and fast settling time (4.2 μs to 0.01%, 10V step) makes these amplifiers useful components in fast, accurate data acquisition systems.

The HA-4602 and 4605's are available in 14 pin CERDIP packages which are interchangeable with most other quad op amps. HA-4602 is specified from -55°C to +125°C, and HA-4605 is specified over 0°C to +75°C range.

PINOUT

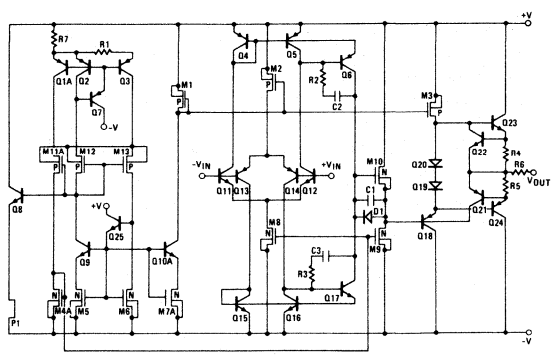
Package Code 4U, LA

TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

SCHEMATIC



ONE FOURTH ONLY (HA-4602/4605)

ABSOLUTE MAXIMUM RATINGS (Note 1)

T_A = +25°C Unless Otherwise Stated

Voltage Between V+ and V- Terminals	40.0V	Power Dissipation (Note 4)	880mW
Differential Input Voltage	±7V	Operating Temperature Range	
Input Voltage (Note 2)	±15.0V	HA-4602-2	$-55^oC \leq T_A \leq +125^oC$
Output Short Circuit Duration (Note 3)	Indefinite	HA-4605-5	$0^oC \leq T_A \leq +75^oC$
		Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$

ELECTRICAL CHARACTERISTICS

V+ = 15V, V- = -15V

PARAMETER	TEMP.	HA-4602-2 -55°C to +125°C MIN.	TYP.	MAX.	HA-4605-5 0°C to +75°C MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS								
* Offset Voltage	+25°C		0.3	2.5		0.5	3.5	mV
	Full			3.0			4.0	mV
Av. Offset Voltage Drift	Full		2			2		µV/°C
* Bias Current	+25°C		130	200		130	300	nA
	Full			325			400	nA
* Offset Current	+25°C		30	75		30	100	nA
	Full			125			120	nA
Common Mode Range	Full	±12			±12			V
Input Noise Voltage (f = 1KHz)	+25°C		8			8		$nV/\sqrt{Hz}$
Input Resistance			500			500		KΩ
TRANSFER CHARACTERISTICS								
* Large Signal Voltage Gain (Note 5)	Full	100K	250K		75K	250K		V/V
* Common Mode Rejection Ratio (Note 9)	Full	86			80			dB
Channel Separation (Note 6)	+25°C		-108			-108		dB
Small Signal Bandwidth	+25°C		8			8		MHz
OUTPUT CHARACTERISTICS								
* Output Voltage Swing (R_L = 10K)	Full	±12	±13		±12	±13		V
(R_L = 2K)	Full	±10	±12		±10	±12		V
Full Power Bandwidth (Note 5)	+25°C		60			60		KHz
Output Current (Note 7)	Full	±10	±15		±8	±15		mA
Output Resistance	+25°C		200			200		Ω
TRANSIENT RESPONSE (Note 8)								
Rise Time	+25°C		50	150		50		ns
Overshoot	+25°C		30	45		30		%
Slew Rate	+25°C	±1	±4			±4		V/µs
Settling Time (Note 10)			4.2			4.2		µs
POWER SUPPLY CHARACTERISTICS								
* Supply Current (I^+ or I^-)	+25°C		4.6	5.5		5.0	6.5	mA
* Power Supply Rejection Ratio (Note 9)	Full	86			80			dB

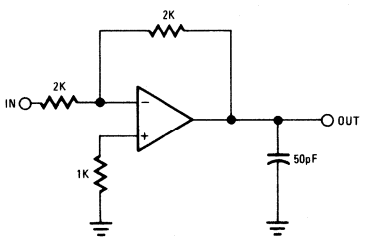
*100% tested for HA1-4602-8

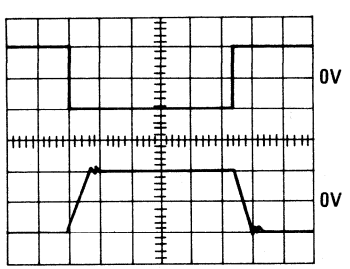
NOTES

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Any one amplifier may be shorted to ground indefinitely.
4. Derate 5.8mW/°C above T_A = +25°C.
5. V_{OUT} = ±10V; R_L = 2K ohms.
6. Channel separation value is referred to the input of the amplifier. Input test conditions are: f = 10kHz; V_{IN} = 200mV peak-to-peak; R_S = 1K ohms. (Refer to Channel Separation vs. Frequency Curve for test circuits.)
7. Output current is measured with V_{OUT} = ±5 volts.
8. For transient response test circuits and measurement conditions refer to Test Circuits section of the data sheet.
9. ΔV = ±5.0 volts.
10. Settling time is measured to 0.1% of final value for a 10 volt input step, A_V = -1.

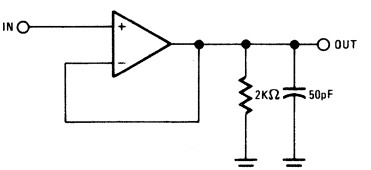
TEST CIRCUITS

LARGE SIGNAL RESPONSE CIRCUIT (Volts: 5V/Div., Time: 5μs/Div.)

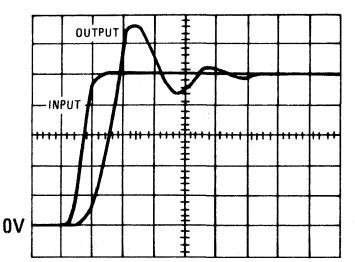




VERT. 5V/DIV.
HORZ. 5 μs/DIV.

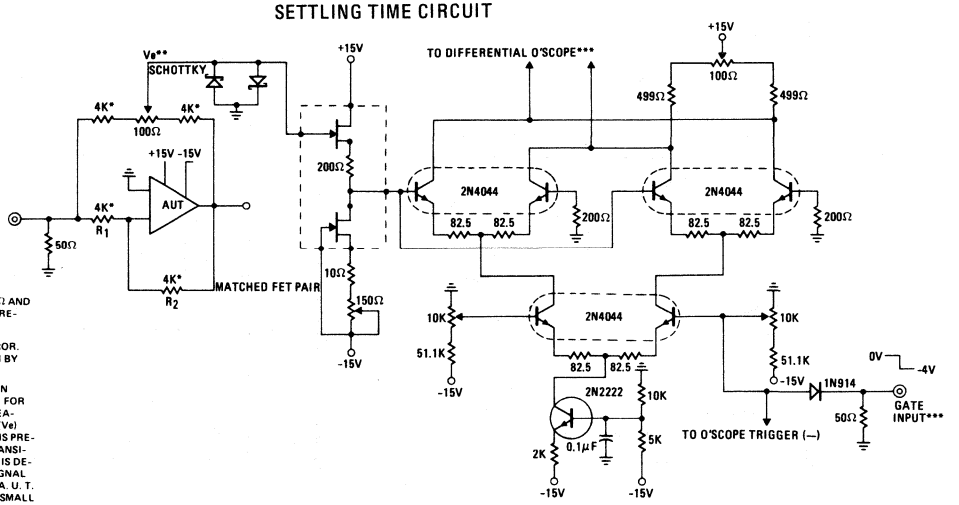


SMALL SIGNAL RESPONSE CIRCUIT (Volts: 10mV/Div., Time: 50ns/Div.)



HORIZONTAL: 50 NSEC/DIV.
VERTICAL: 10mV/DIV

SETTLING TIME CIRCUIT



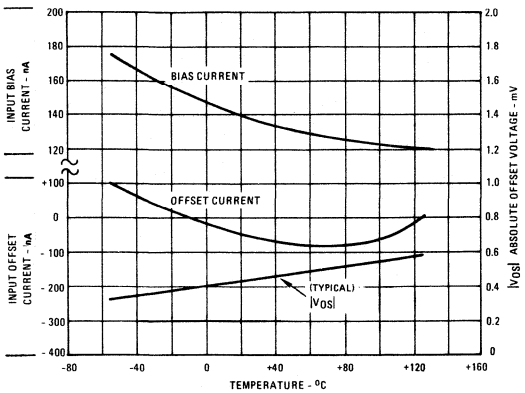
* SHOWN FOR AV = -1. USE 800Ω AND 400Ω FOR AV = -5, AV = -10, RESPECTIVELY.

** THIS IS SUMMING POINT ERROR. OUTPUT ERROR, ε, IS GIVEN BY ε = (1 + AV) Ve.

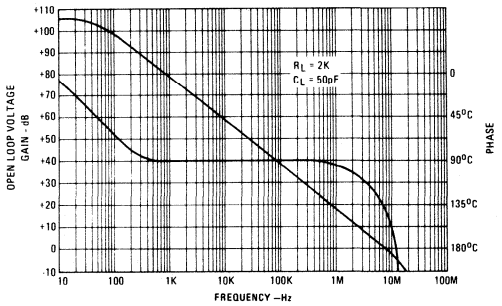
*** MEASUREMENT IS 5× Ve WHEN GATE INPUT IS "LOW" (-4V). FOR GATE INPUT "HIGH" (0V), MEASUREMENT IGNORES INPUT (Ve) SO THAT SCOPE OVERLOAD IS PREVENTED DURING LARGE TRANSITIONS. GATE INPUT SIGNAL IS DELAYED WITH RESPECT TO SIGNAL INPUT TO ALLOW TIME FOR A. U. T. SLEWING AND SETTLING TO SMALL ERROR VOLTAGES.

V+ = +15V, V- = -15V, T_A = +25°C Unless Otherwise Stated.

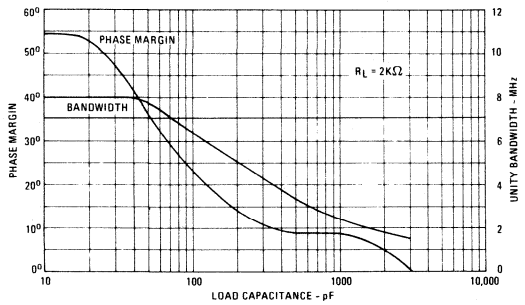
OFFSET VOLTAGE INPUT BIAS AND OFFSET CURRENT VS. TEMPERATURE



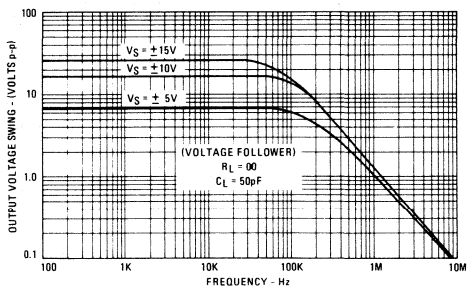
OPEN LOOP FREQUENCY RESPONSE



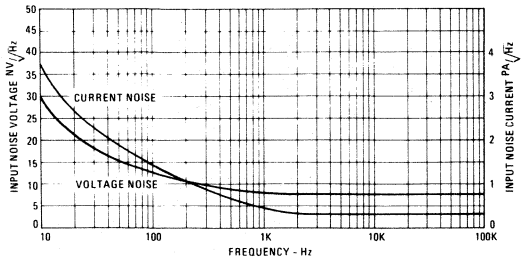
SMALL SIGNAL BANDWIDTH AND PHASE MARGIN VS. LOAD CAPACITANCE



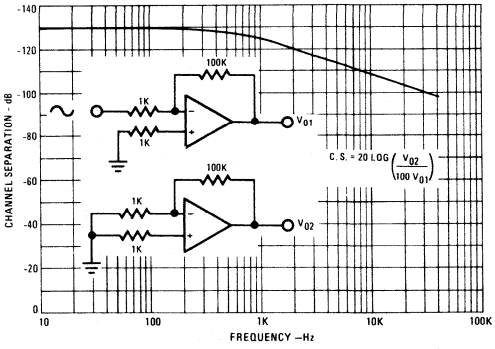
OUTPUT VOLTAGE SWING VS. FREQUENCY AND SUPPLY VOLTAGE



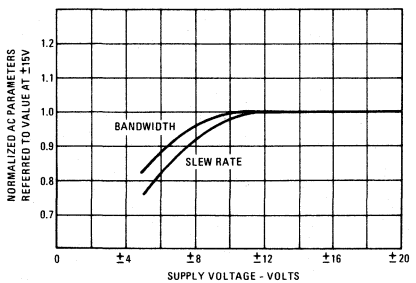
INPUT NOISE VS. FREQUENCY



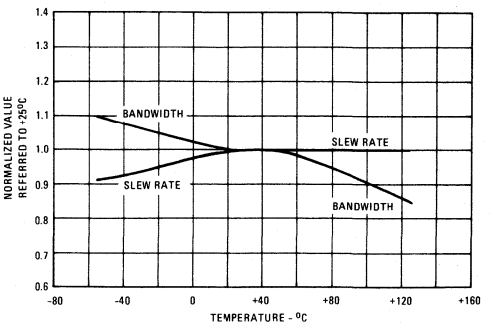
CHANNEL SEPARATION VS. FREQUENCY



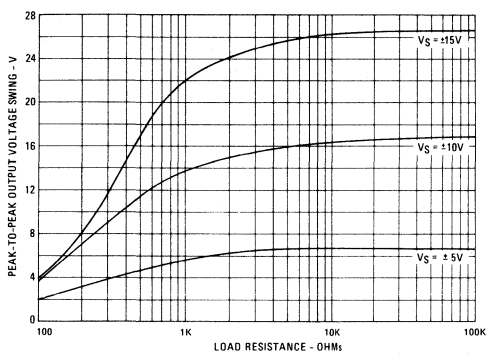
NORMALIZED AC PARAMETERS VS. SUPPLY VOLTAGE



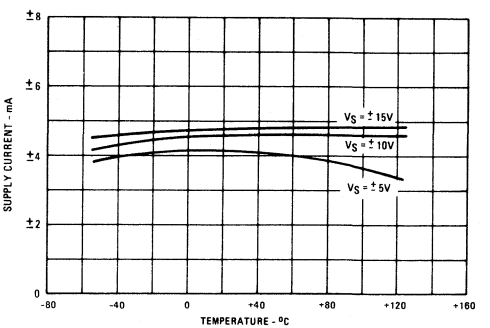
NORMALIZED AC PARAMETERS VS. TEMPERATURE



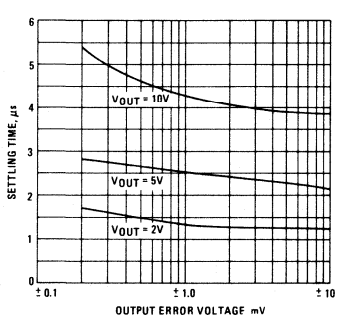
MAXIMUM OUTPUT VOLTAGE SWING VS. LOAD RESISTANCE AND SUPPLY VOLTAGE



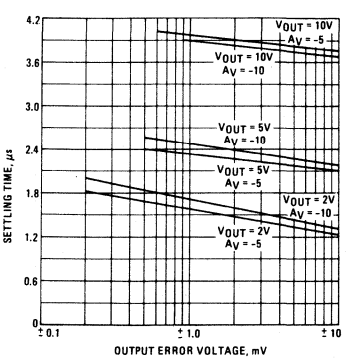
POWER SUPPLY CURRENT VS. TEMPERATURE AND SUPPLY VOLTAGE



SETTLING TIME VS. OUTPUT AMPLITUDE (A_V = -1)



SETTLING TIME VS. OUTPUT AMPLITUDE AND SIGNAL GAIN (A_V = -5 AND A_V = -10)



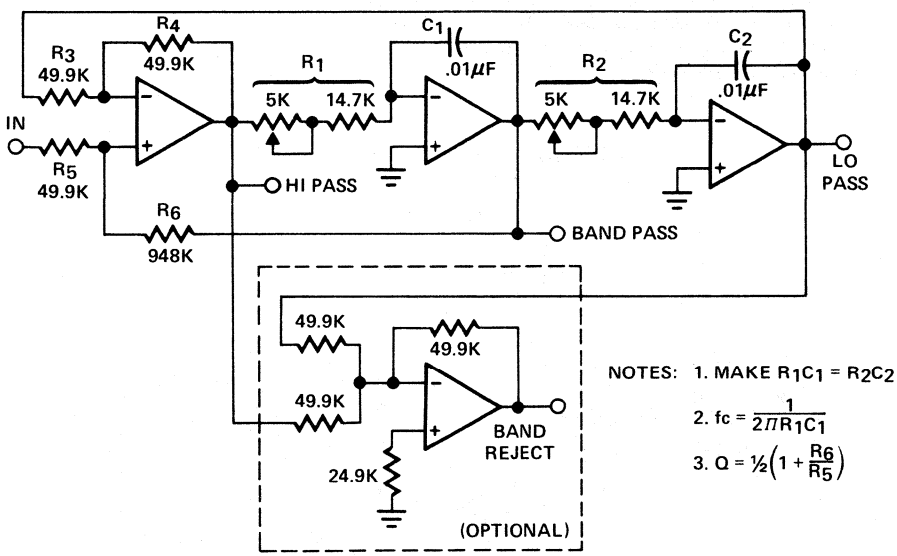
1. POWER SUPPLY DECOUPLING: Although not absolutely necessary, it is recommended that all power supply lines be decoupled with .01 μ F ceramic capacitors to ground. Decoupling capacitors should be located as near to the amplifier terminals as possible.

2. UNUSED OP AMPS: Unused op amp sections should be connected in a non-inverting follower configuration with the (+) input tied to ground in order to insure optimum performance of devices being used.

3. In high frequency applications where large value feedback resistors are used, a small capacitor (3pF) may be needed in parallel with the feedback resistor to neutralize the pole introduced by input capacitance.

APPLICATIONS

2ND ORDER STATE VARIABLE FILTER (1kHz, Q = 10)



NOTES: 1. MAKE $R_1C_1 = R_2C_2$

2. $f_c = \frac{1}{2\pi R_1 C_1}$

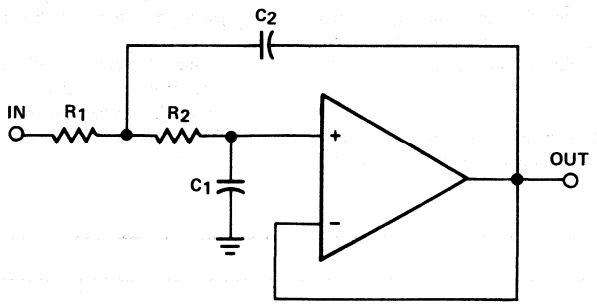
3. $Q = \frac{1}{2}\left(1 + \frac{R_6}{R_5}\right)$

The state variable filter is relatively insensitive to component changes (changes can be adjusted out with potentiometers) and also has low sensitivity to amplifier bandwidths. (Amplifier gain bandwidth product should be $\gg Q \times f_C$). The bandwidth criteria will determine whether a general purpose op amp like Harris HA-4741 or the wide band HA-4602/4605 should be used.

This filter finds wide application because multiple filtering functions are available simultaneously (High pass, Lo pass, Band pass, Band reject). In this circuit the various RC products are matched with pot adjustments allowing for non-interactive adjustment of Q and f_C. This allows capacitors (C_1, C_2) with loose tolerances to be used. To tune for f_C, apply a sine wave at f_C to the input, adjust R_1 for equal amplitudes at the Hi pass and Band pass terminals (they will be phased 90° apart) then adjust R_2 for equal amplitudes at the Band pass and Lo pass terminals.

The state variable filter is often used as building blocks in multiple pole Butterworth of Chebyshev filters. Many references contain normalized tables indicating settings for Q and f_C of each pole-pair section.

SALLEN AND KEY 2ND ORDER LO PASS FILTER



NOTES:

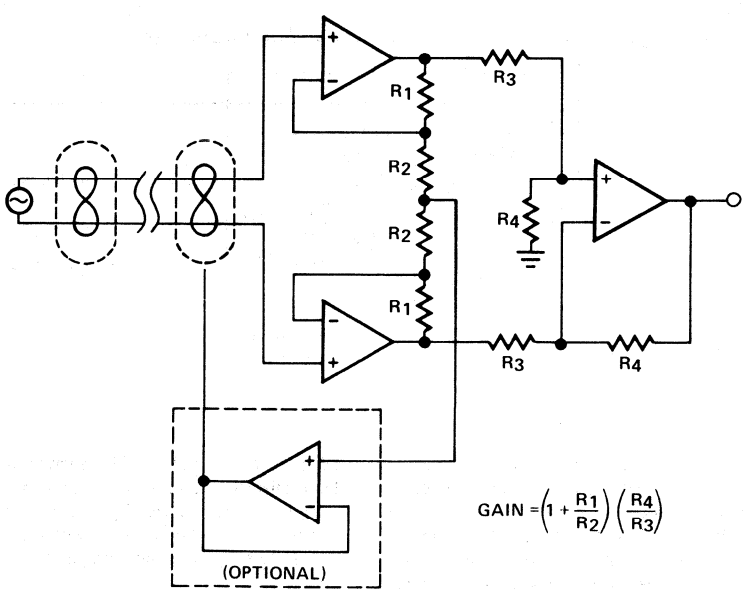
1. Make $R_1 = R_2$
2. $f_c = \frac{1}{2\pi R_1 \sqrt{C_1 C_2}}$
3. $Q = \frac{1}{2}\sqrt{\frac{C_2}{C_1}}$

The advantage of using the Sallen and Key filter is simplicity, but in any application this must be weighed against the state-variable type filter for accuracy, practicality, and cost. Amplifier bandwidth limitations are much more apparent at moderate frequencies and Q values with this filter design. (For accuracy, amplifier gain-bandwidth product should be $\gg f_C \times Q^2$). The wide bandwidth of the HA-4602/4605 is particularly advantageous in this design even at audio frequencies.

In this filter all component values affect both Q and f_C. Precision, temperature stable resistors and capacitors must be used.

For economy, this filter could be used in the low Q stages of multiple-pole filter design, while the state variable type is used in the more critical stages.

INSTRUMENTATION AMPLIFIER



Instrumentation amplifiers (differential amplifiers) are specifically designed to extract and amplify small differential signals from much larger common mode voltages.

To serve as building blocks in instrumentation amplifiers, op amps must have very low offset voltage drift, high gain and wide bandwidth. The HA-4602/4605 is ideally suited for this application, delivering superior input and speed characteristics.

The optional circuitry makes use of the fourth amplifier section as a shield driver which enhances the AC common mode rejection by nullifying the effects of capacitance-to-ground mismatch between input conductors.

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HA-4622/4625

Wide Band, High Performance Quad Operational Amplifier

FEATURES

- Wide Gain Bandwidth Product 70MHz
- High Slew Rate ±20V/μs
- Low Offset Voltage 0.3mV
- Fast Settling (0.01%, 10V Step) 2.5μs
- Total Harmonic Distortion <.01% to 30kHz
- Low Drift 2μV/°C
- Low Power Consumption 35mW/Amp
- Supply Range ±5V to ±20V

APPLICATIONS

- High Q Wide Band Filters
- Pulse Amplifiers
- Audio Amplifiers
- Data Acquisition Systems
- Absolute Value Circuits
- Video and R.F. Amplifiers

DESCRIPTION

The HA-4622 and HA-4625 are wide band quad operational amplifiers featuring high slew rate, wide bandwidth and fast settling time specifications complemented by low input offset voltage, low drift and input noise voltage.

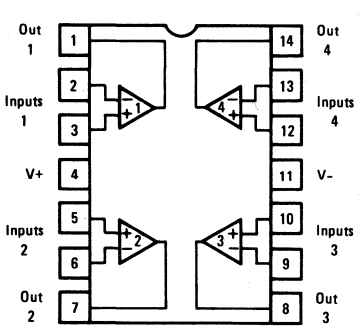
These dielectrically isolated devices are optimized to offer excellent features suitable for applications where a gain of 10 or greater is to be used. The 35mW/amp and a 70MHz gain-bandwidth-product make these monolithic amplifiers valuable components for many active filter circuits. HA-4622/4625 offer 0.3mV offset voltages and 2 μV/°C offset voltage drift for very accurate signal conditioning designs. In high performance audio applications, these amplifiers deliver 260kHz full power bandwidth and 8nV/$\sqrt{\text{Hz}}$ noise voltage. For fast accurate data acquisition systems HA-4622/4625 offer 20Vμs slew rate and settling time of 2.5μsecs to 0.1% 10V step.

HA-4622 and HA-4625 are available in 14 pin CERDIP packages and are interchangeable with most other quad op amps. HA-4625 is also available in chip form. The HA-4622 specifications are given for operation from -55°C to +125°C while HA-4625 is specified for operation over the 0°C to +75°C range.

PINOUT

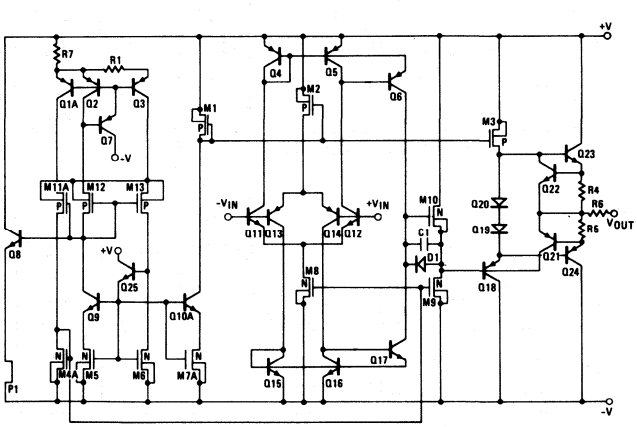
Package Code 4U

TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge.

SCHEMATIC



ONE FOURTH ONLY - HA-4622/4625

ABSOLUTE MAXIMUM RATINGS (Note 1)

T_A = +25°C Unless otherwise stated.

Voltage between V+ and V- Terminals	40.0V	Power Dissipation (Note 4)	880mW
Differential Input Voltage	±7V	Operating Temperature Range	
Input Voltage (Note 2)	±15.0V	HA-4622-2	$-55°C \leq T_A \leq +125°C$
Output Short Circuit Duration (Note 3)	Indefinite	HA-4625-5	$0°C \leq T_A \leq +75°C$
		Storage Temperature Range	$-65°C \leq T_A \leq +150°C$

ELECTRICAL CHARACTERISTICS

V+ = 15V, V- = -15V

PARAMETER	TEMP	HA-4622-2 -55°C to +125°C MIN	HA-4622-2 TYP	HA-4622-2 MAX	HA-4625-5 0°C to +75°C MIN	HA-4625-5 TYP	HA-4625-5 MAX	UNITS
INPUT CHARACTERISTICS								
*Offset Voltage	+25°C		0.3	2.5		0.5	3.5	mV
	Full			3.0			4.0	mV
Av. Offset Voltage Drift	Full		2			2		µV/°C
*Bias Current	+25°C		130	200		130	300	nA
	Full			325			400	nA
*Offset Current	+25°C		30	75		30	100	nA
	Full			125			120	nA
Common Mode Range	Full	±12			±12			V
Input Noise Voltage (f = 1kHz)	+25°C		8			8		$nV/\sqrt{Hz}$
Input Resistance	+25°C		500			500		KΩ
TRANSFER CHARACTERISTICS								
*Large Signal Voltage Gain (Note 5)	Full	100K	250K		75K	250K		V/V
*Common Mode Rejection Ratio (Note 6)	Full	86			80			dB
Channel Separation (Note 7)	+25°C		-108			-108		dB
Gain Bandwidth Products (Note 8)	+25°C		70			70		MHz
OUTPUT CHARACTERISTICS								
*Output Voltage Swing (R_L = 10K)	Full	±12	±13		±12	±13		V
(R_L = 2K)	Full	±10	±12		±10	±12		V
Full Power Bandwidth (Note 9)	+25°C		260			260		kHz
Output Current (Note 10)	Full	±10	±15		±8	±15		mA
Output Resistance	+25°C		200			200		Ω
TRANSIENT RESPONSE (Note 11)								
Rise Time	+25°C		38	60		38		ns
Overshoot	+25°C		45	60		45		%
Slew Rate	+25°C	±12	±20		±12	±20		V/µs
Settling Time (Note 12)	+25°C		2.5			2.5		µs
POWER SUPPLY CHARACTERISTICS								
*Supply Current (I+ or I-)	+25°C		4.6	5.5		5.0	6.5	mA
*Power Supply Rejection Ratio (NOTE 6)	Full	86			80			dB

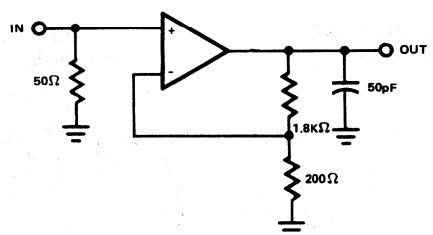
*100% tested for HA1-4622-8

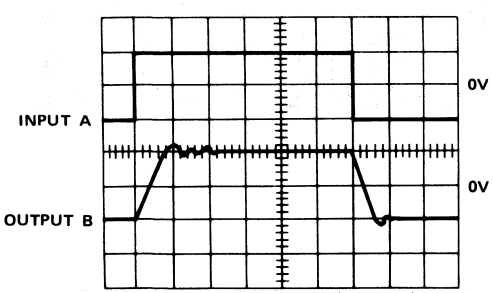
NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. For supply voltages $< \pm$ 15V, the absolute maximum input voltage is equal to the supply voltage.
3. Any one amplifier may be shorted to ground indefinitely.
4. Derate 5.8mW/^{o}C above T_A = +25^{o}C.
5. $V_{OUT} = \pm 10V$, R_L = 2KΩ
6. $\Delta V = \pm 5.0V$.
7. Channel separation value is referred to the input of the amplifier. Input test conditions are: f = 10kHz; V_{IN} = 200mV peak to peak; R_S = 1kΩ . (Refer to Channel Separation vs. Frequency Curve for test circuits.)
8. A_V = 10; R_L = 2K; $C_L \leq$ 10pF.
9. Full power bandwidth is guaranteed by equation:
   $$\text{Full power bandwidth} = \frac{\text{Slew Rate}}{2\pi V_{Peak}}$$
10. Output current is measured with $V_{OUT} = \pm 5V$.
11. Refer to Test Circuits section of the data sheet.
12. Setting time is measured to 0.1% of final value for a 1 volt input step, and A_V = -10.

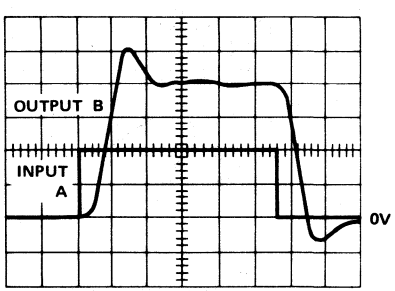
TEST CIRCUITS

LARGE AND SMALL
SIGNAL RESPONSE CIRCUIT



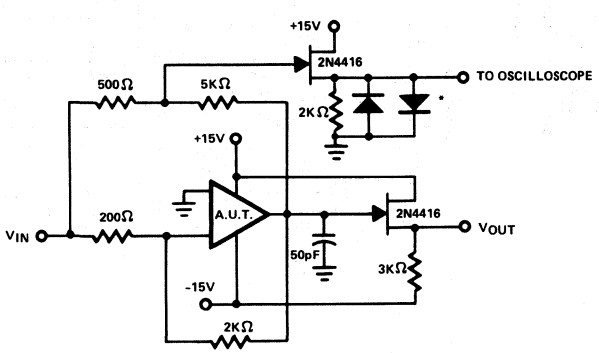


VOLTS: Input A: .5V/Div., Output B: 5V/Div.
TIME: 500ns/Div.



VOLTS: Input A: .01V/Div., Output B: 50mV/Div.
TIME: 50ns/Div.

SETTLING TIME CIRCUIT



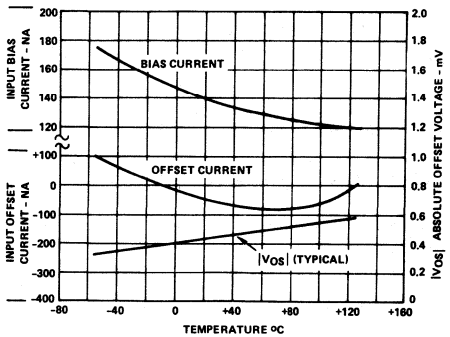
A_V = -10

Feedback and summing resistors should be 0.1%.

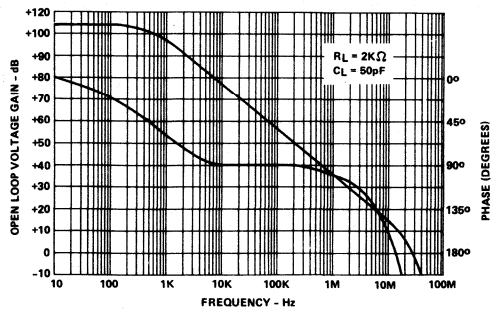
* Clipping diodes are optional. HP 5082-2810 recommended.

$V+ = +15V$, $T_A = +25^oC$ Unless otherwise stated.

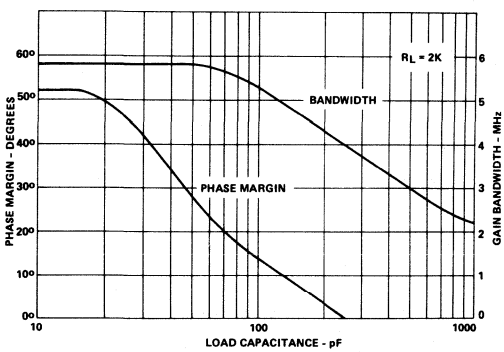
OFFSET VOLTAGE INPUT BIAS AND OFFSET CURRENT VS. TEMPERATURE



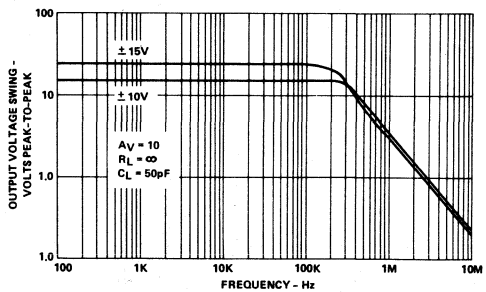
OPEN LOOP FREQUENCY RESPONSE



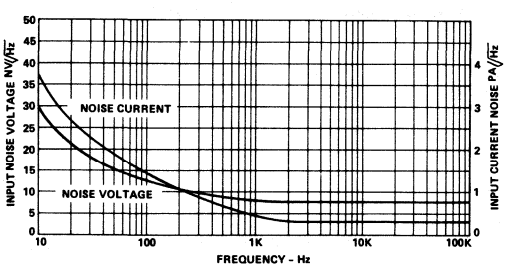
SMALL SIGNAL BANDWIDTH AND PHASE MARGIN VS. LOAD CAPACITANCE



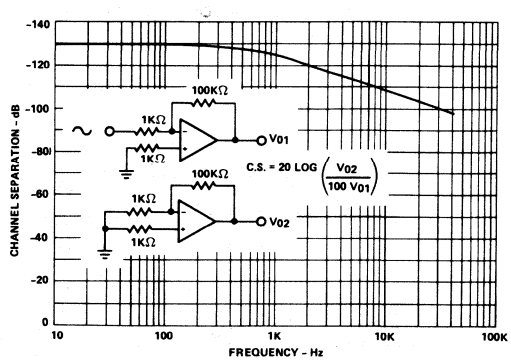
OUTPUT VOLTAGE SWING VS. FREQUENCY AND SUPPLY VOLTAGE



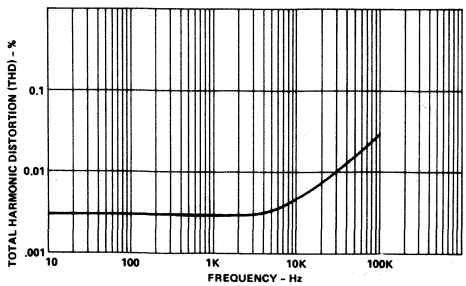
INPUT NOISE VS. FREQUENCY



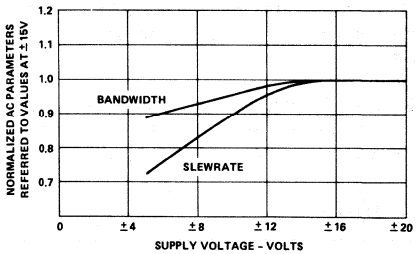
CHANNEL SEPARATION VS. FREQUENCY



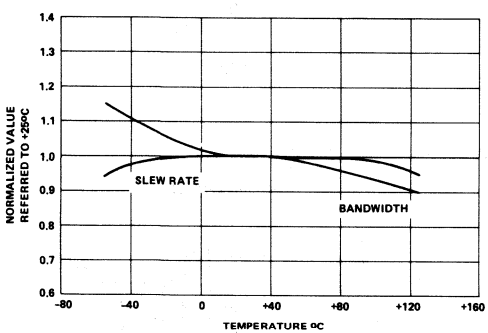
TOTAL HARMONIC DISTORTION VS. FREQUENCY



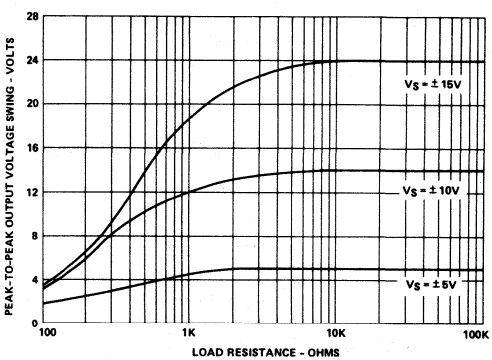
NORMALIZED AC PARAMETERS VS. SUPPLY VOLTAGE



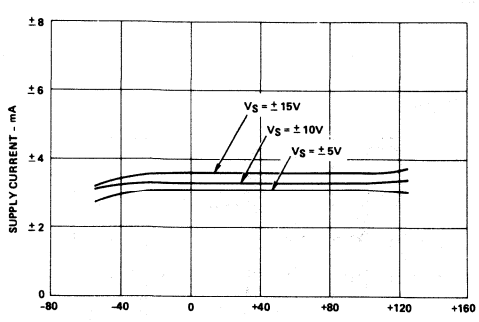
NORMALIZED AC PARAMETERS VS. TEMPERATURE



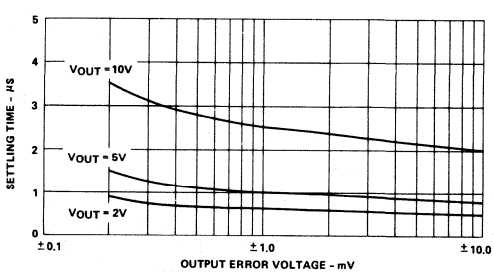
MAXIMUM OUTPUT VOLTAGE SWING VS. LOAD RESISTANCE AND SUPPLY VOLTAGE



POWER SUPPLY CURRENT VS. TEMPERATURE AND SUPPLY VOLTAGE



SETTLING TIME VS. OUTPUT AMPLITUDE (A_V = -10)



APPLYING THE HA-4622/4625

1. POWER SUPPLY DECOUPLING: Although not absolutely necessary, it is recommended that all power supply lines be decoupled with .01μF ceramic capacitors to ground. Decoupling capacitors should be located as near to the amplifier terminals as possible. If several amplifier sections are connected in series, it is recommended that every third or fourth section be decoupled.

2. UNUSED OP AMPS: Unused op amp sections should be connected in a non-inverting A_V = 10 configuration with the (+) input tied to ground in order to optimize performance of devices being used.

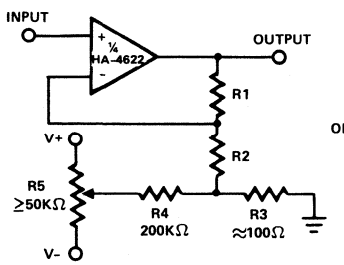
3. In high frequency applications where large value feedback resistors are used, a small capacitor (3pF) may be needed in parallel with the feedback resistor to neutralize the pole introduced by input capacitance.

4. When driving heavy capacitive loads (>100pF), a small value resistor should be connected in series with the output and inside the feedback loop.

APPLICATIONS

SUGGESTED METHODS FOR OFFSET NULLING

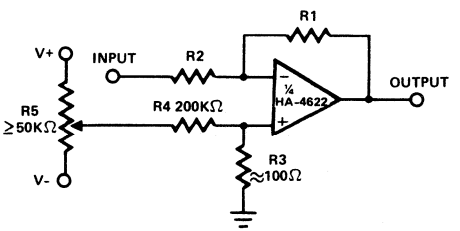
NON-INVERTING AMPLIFIER



NON-INVERTING AND INVERTING AMPLIFIERS RANGE OF ADJUSTMENT DETERMINED BY PRODUCT OF VSUPPLY AND R3/R4 RATIO

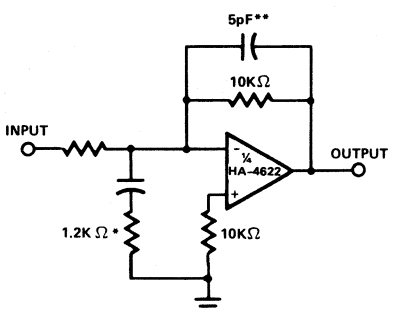
$$A_V = 1 + \frac{R1}{R2 + R3}$$

INVERTING AMPLIFIER

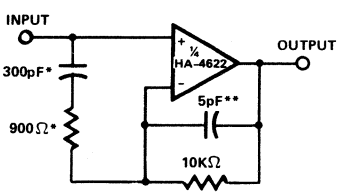


SUGGESTED COMPENSATION FOR UNITY GAIN STABILITY

INVERTING



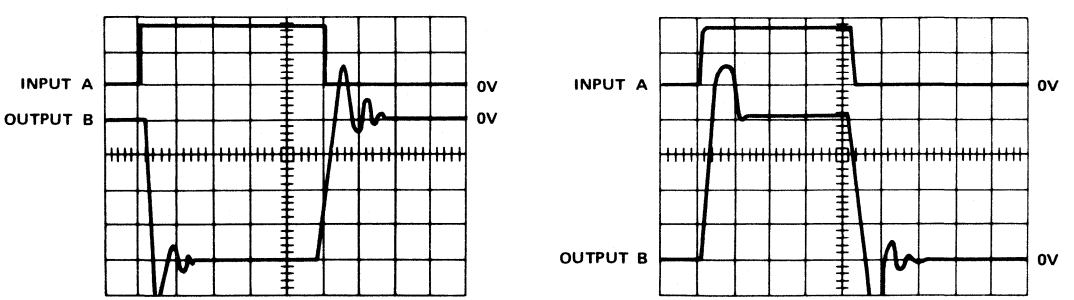
NON-INVERTING



* VALUES WERE DETERMINED EXPERIMENTALLY FOR OPTIMUM SPEED AND SETTLING TIME

** OPTIONAL

LARGE SIGNAL RESPONSE



VOLTS: Input A: 5V/Div., Output B: 2V/Div.
TIME: 1μs/Div.

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HA-4741

Quad Operational Amplifier

FEATURES

- SLEW RATE 1.6V/μs (TYP.)
- BANDWIDTH 3.5MHz (TYP.)
- INPUT VOLTAGE NOISE 9nV/$\sqrt{Hz}$ (TYP.)
- INPUT OFFSET VOLTAGE 0.5mV (TYP.)
- INPUT BIAS CURRENT 60nA (TYP.)
- SUPPLY RANGE ±2V TO ±20V
- NO CROSSOVER DISTORTION
- STANDARD QUAD PIN-OUT

APPLICATIONS

- UNIVERSAL ACTIVE FILTERS
- D3 COMMUNICATIONS FILTERS
- AUDIO AMPLIFIERS
- BATTERY-POWERED EQUIPMENT

DESCRIPTION

The HA-4741, which contains four amplifiers on a monolithic chip, provides a new measure of performance for general purpose operational amplifiers. Each amplifier in the HA-4741 has operating specifications that equal or exceed those of the 741-type amplifier in all categories of performance.

HA-4741 is well suited to applications requiring accurate signal processing by virtue of its low values of input offset voltage (0.5mV), input bias current (60nA) and input voltage noise (9nV/ $\sqrt{Hz}$ at 1kHz). 3.5MHz bandwidth, coupled with high open-loop gain, allow the HA-4741 to be used in designs requiring amplification of wide band signals, such as audio amplifiers. Audio application is further enhanced by the HA-4741's negligible output crossover distortion. These excellent dynamic characteristics also make the HA-4741 ideal for a wide range of active filter designs. Performance integrity of multi-channel designs is assured by a high level of amplifier-to-amplifier isolation (108dB at 1kHz).

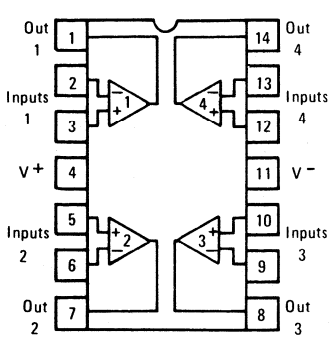
A wide range of supply voltages (±2V to ±20V) can be used to power the HA-4741, making it compatible with almost any system including battery-powered equipment.

The HA-4741 has guaranteed operation over -55°C to +125°C and can be furnished to meet MIL-STD-883 (HA-4741-8). The HA-4741-5 is guaranteed over 0°C to +75°C and is available in ceramic and plastic dual-in-line packages and in dice form.

PINOUT

Package Code 4U, 3M, LA

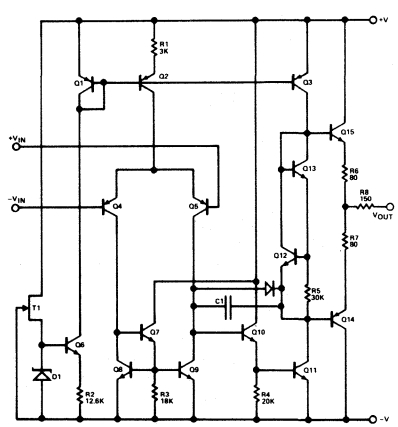
TOP VIEW



QUAD OP AMP

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

SCHEMATIC



(¼) HA-4741

ABSOLUTE MAXIMUM RATINGS

T_A = +25°C Unless Otherwise Stated		Power Dissipation For Epoxy Package. (Note 3)	880mW
Voltage Between V+ and V- Terminals	40.0V	Operating Temperature Range	
Differential Input Voltage	±30.0V	HA-4741-2	$-55°C \leq T_A \leq +125°C$
Input Voltage (Note 1)	±15.0V	HA-4741-5	$0°C \leq T_A \leq +75°C$
Output Short Circuit Duration (Note 2)	Indefinite	Storage Temperature Range	$-65°C \leq T_A \leq +150°C$

ELECTRICAL CHARACTERISTICS

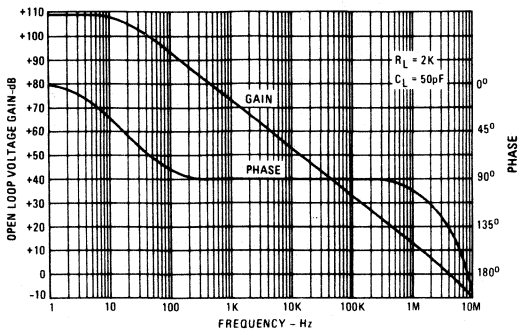
V+ = 15V, V- = -15V		HA-4741-2 -55°C to +125°C			HA-4741-5 0°C to +75°C			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS								
* Offset Voltage	+25°C		0.5	3.0		1.0	5.0	mV
	Full		4.0	5.0		5.0	6.5	mV
Av. Offset Voltage Drift	Full		5			5		µV/°C
* Bias Current	+25°C		60	200		60	300	nA
	Full			325			400	nA
* Offset Current	+25°C		15	30		30	50	nA
	Full			75			100	nA
Common Mode Range	Full	±12			±12			V
Differential Input Resistance	+25°C		5			5		MΩ
Input Noise Voltage (f = 1KHz)	+25°C		9			9		$nV/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
* Large Signal Voltage Gain (Note 4)	+25°C	50K	100K		25K	50K		V/V
	Full	25K			15K			V/V
* Common Mode Rejection Ratio (Note 8)	+25°C	80			80			dB
	Full	74			74			dB
Channel Separation (Note 5)	+25°C	90	-108		90	-108		dB
Small Signal Bandwidth	+25°C	2.5	3.5		2.5	3.5		MHz
OUTPUT CHARACTERISTICS								
* Output Voltage Swing (R_L = 10K)	Full	±12	±13.7		±12	±13.7		V
(R_L = 2K)	Full	±10	±12.5		±10	±12.5		V
Full Power Bandwidth (Notes 4 & 9)	+25°C	14	25		14	25		kHz
Output Current (Note 6)	Full	±5	±15		±5	±15		mA
Output Resistance	+25°C		300			300		Ω
TRANSIENT RESPONSE (Notes 7 &10)								
Rise Time (Note 11)	+25°C		75	140		75	140	ns
Overshoot (Note 11)	+25°C		25	40		25	40	%
Slew Rate (Note 12)	+25°C		±1.6			±1.6		V/µs
POWER SUPPLY CHARACTERISTICS								
* Supply Current (I^+ or I^-)	+25°C			5.0			7.0	mA
* Power Supply Rejection Ratio (Note 8)	Full	80			80			dB

NOTES:
1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. One amplifier may be shorted to ground indefinitely.
3. Derate 5.8mW/°C above T_A = +25°C.
4. V_{OUT} = ±10, R_L = 2K
5. Referred to input; f = 10KHz, R_S = 1K
6. V_{OUT} = ±10
7. See pulse response characteristics
8. ΔV = ±5.0V
9. Full power bandwidth guaranteed based upon slew rate measurement FPBW = S.R./2πVpeak
10. R_L = 2K, C_L = 50pf.
11. V_{OUT} = ±200mV
12. V_{OUT} = ±5V

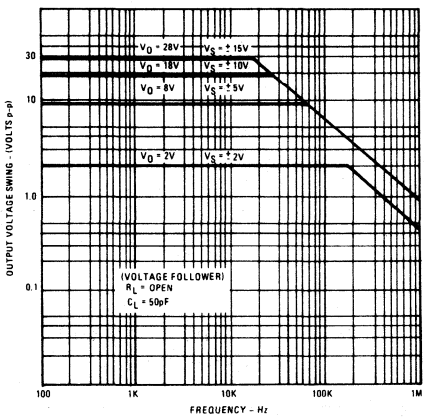
*100% Tested for DASH 8.

$V+ = +15V, V^- = -15V, T_A = +25^oC$
Unless Otherwise Stated.

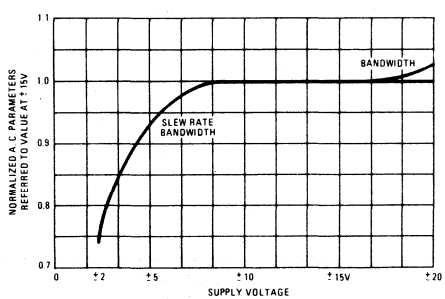
OPEN LOOP FREQUENCY RESPONSE



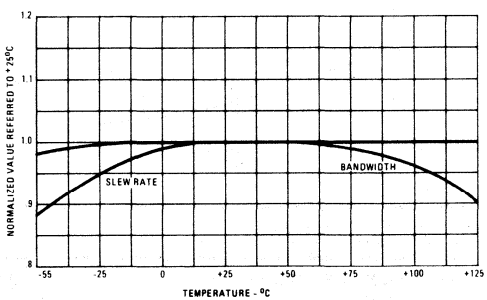
OUTPUT VOLTAGE SWING VS. FREQUENCY



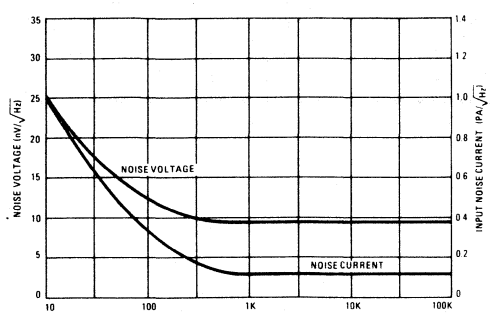
NORMALIZED AC PARAMETERS VS. SUPPLY VOLTAGE



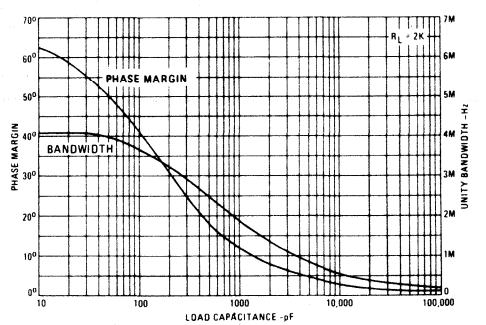
NORMALIZED AC PARAMETERS VS. TEMPERATURE



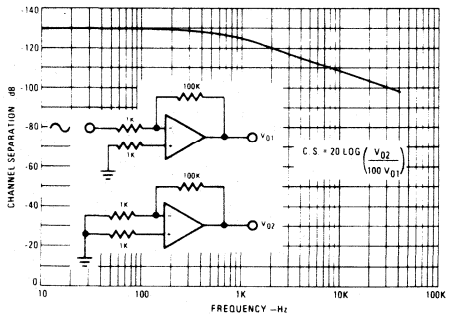
INPUT NOISE VS. FREQUENCY



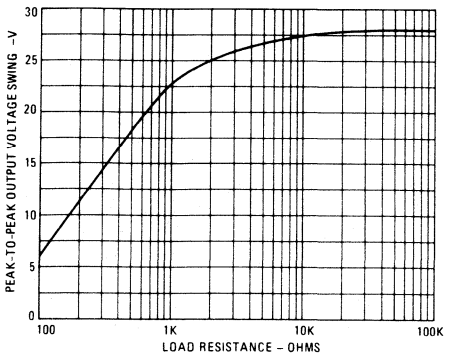
SMALL SIGNAL BANDWIDTH AND PHASE MARGIN VS. LOAD CAPACITANCE



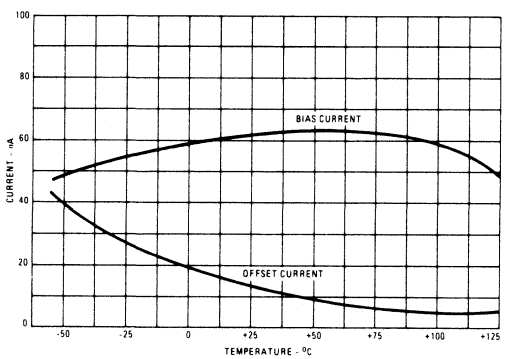
CHANNEL SEPARATION VS. FREQUENCY



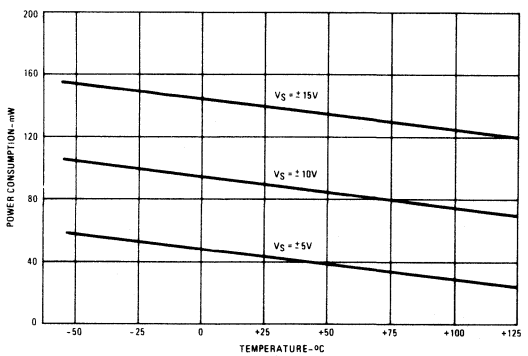
MAXIMUM OUTPUT VOLTAGE SWING VS. LOAD RESISTANCE



INPUT BIAS AND OFFSET CURRENT VS. TEMPERATURE

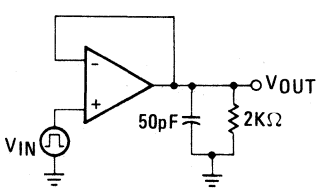


POWER CONSUMPTION VS. TEMPERATURE

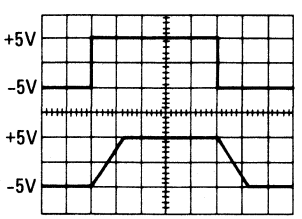


PULSE RESPONSE

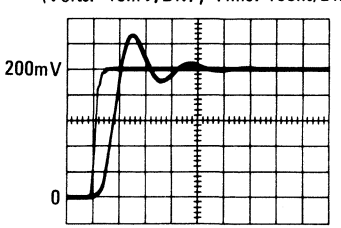
TRANSIENT RESPONSE/SLEW RATE CIRCUIT



SLEW RESPONSE
(Volts: 5V/Div, Time: 5 μs/Div)



TRANSIENT RESPONSE
(Volts: 40mV/Div., Time: 100ns/Div.)



HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HA-4900/4905

Precision Quad Comparator

FEATURES

- FAST RESPONSE TIME 130ns
- LOW OFFSET VOLTAGE 2.0mV
- LOW OFFSET CURRENT 10nA
- SINGLE OR DUAL-VOLTAGE SUPPLY OPERATION
- SELECTABLE OUTPUT LOGIC LEVELS
- ACTIVE PULL-UP/PULL-DOWN OUTPUT CIRCUIT - NO EXTERNAL RESISTORS REQUIRED

APPLICATIONS

- THRESHOLD DETECTOR
- ZERO-CROSSING DETECTOR
- WINDOW DETECTOR
- ANALOG INTERFACES FOR MICROPROCESSORS
- HIGH STABILITY OSCILLATORS
- LOGIC SYSTEM INTERFACES

DESCRIPTION

The HA-4900/4905 are monolithic, quad, precision comparators offering fast response time, low offset voltage, low offset current, and virtually no channel-to-channel crosstalk for applications requiring accurate, high speed, signal level detection. These comparators can sense signals at ground level while being operated from either a single +5 volt supply (digital systems) or from dual supplies (analog networks) up to ±15 volts. The HA-4900/4905 contains a unique current driven output stage which can be connected to logic system supplies (V_{Logic}+ and V_{Logic}-) to make the output levels directly compatible (no external components needed) with any standard logic or special system logic levels. In combination analog/digital systems, the design employed in the HA-4900/4905 input and output stages prevents troublesome ground coupling of signals between analog and digital portions of the system.

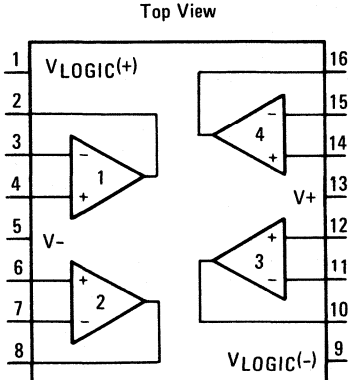
These comparators' combination of features makes them ideal components for signal detection and processing in data acquisition systems, test equipment, and microprocessor/analog signal interface networks.

Both devices are available in 16 pin dual-in-line ceramic packages. The HA-4900 operates from -55°C to +125°C and the HA-4905 operates over a 0°C to +75°C temperature range.

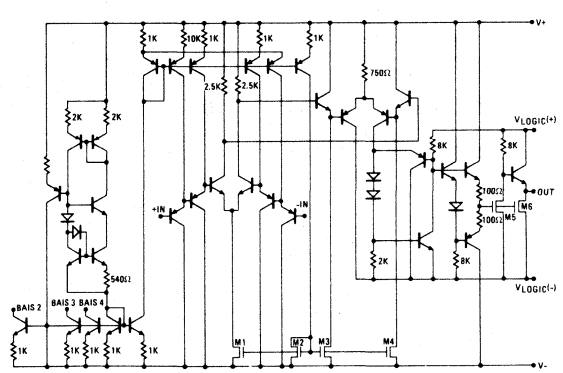
PIN OUT

Package Code 4Z

Top View



SCHEMATIC



One Fourth Only (HA-4900/4905)

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage Between V+ and V-	33V
Voltage Between $V_{Logic}(+)$ and $V_{Logic}(-)$	18V
Differential Input Voltage	±15V
Peak Output Current	±50mA
Internal Power Dissipation (Note 7, 8)	880mW
Storage Temperature Range	$-65^{o}C \leq T_A \leq 150^{o}C$

ELECTRICAL CHARACTERISTICS (Note 9)

V+ = +15.0V
V- = -15.0V
$V_{Logic}(+)$ = 5.0V
$V_{Logic}(-)$ = GND.

PARAMETER	TEMP.	HA-4900 -55°C to +125°C MIN.	HA-4900 -55°C to +125°C TYP.	HA-4900 -55°C to +125°C MAX.	HA-4905 0°C to +75°C MIN.	HA-4905 0°C to +75°C TYP.	HA-4905 0°C to +75°C MAX.	UNITS
INPUT CHARACTERISTICS								
* Offset Voltage (Note 2)	25°C		2.0	3.0		4.0	7.5	mV
	Full			4.0			10.0	mV
* Offset Current	25°C		10	25		25	50	nA
	Full			35			70	nA
* Bias Current (Note 3)	25°C		50	75		100	150	nA
	Full			150			300	nA
Input Sensitivity (Note 4)	25°C			0.3			0.5	mV
	Full			0.7			0.7	mV
* Common Mode Range	Full	V-		V+ -2.4	V-		V+ -2.4	V
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain	25°C		400K			400K		V/V
Response Time (T_{pd0})(Note 5)	25°C		130	200		130	200	ns
Response Time (T_{pd1})(Note 5)	25°C		180	215		180	215	ns
OUTPUT CHARACTERISTICS								
* Output Voltage Level								
Logic "Low State" (V_{OL})(Note6)	Full		0.2	0.4		0.2	0.4	V
Logic "High State" (V_{OH})(Note6)	Full	3.5	4.2		3.5	4.2		V
Output Current								
I_{Sink}	Full	3.5			3.5			mA
I_{Source}	Full	3.0			3.0			mA
POWER SUPPLY CHARACTERISTICS								
* Supply Current, $I_{ps}(+)$	25°C		6.5	20		7	20	mA
* Supply Current, $I_{ps}(-)$	25°C		4	8		5	8	mA
* Supply Current, I_{ps}(Logic) (Note 10)	25°C		2.0	4		2.0	4	mA
Supply Voltage Range								
$V_{Logic}(+)$ (Note 7)	Full	0		+15.0	0		+15.0	V
$V_{Logic}(-)$ (Note 7)	Full	-15.0		0	-15.0		0	V

*100% tested for HA1-4900-8.

NOTES

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

2. Minimum differential input voltage required to ensure a defined output state.

3. Input bias currents are essentially constant with differential input voltages up to ±9 volts. With differential input voltages from ±9 to ±15 volts, bias current on the more negative input can rise to approximately 500 μA.

4. $R_S \leq$ 200 ohms. Input sensitivity is the differential voltage required at the input to make the output change state, after the offset has been nulled.

5. See Test Circuit below.

6. For V_{OH} and V_{OL}: I_{Sink} = 3.5mA, I_{Source} = 3.0mA. For other values of V_{Logic}; V_{OH} (min.) = V_{Logic} + -1.5V.

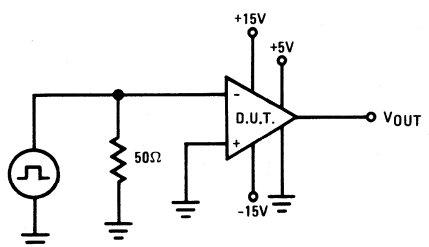
7. Total Power Dissipation (T.P.D.) is the sum of individual dissipation contributions of V+, V- and V_{Logic} shown in curves of Power Dissipation vs. Supply Voltages (see page 5). The calculated T.P.D. is then located on the graph of Maximum Allowable Package Dissipation vs. Ambient Temperature (see page 5) to determine ambient temperature operating limits imposed by the calculated T.P.D.. For instance, the combination of +15V, -15V, +5V, 0V (V+, V-, V_{Logic}+, V_{Logic}-) gives a T.P.D. of 350mW which allows operation to +125°C; the combination +15V, -15V, +15V, 0V gives a T.P.D. of 450mW and an operating limit of T_A = +95°C.

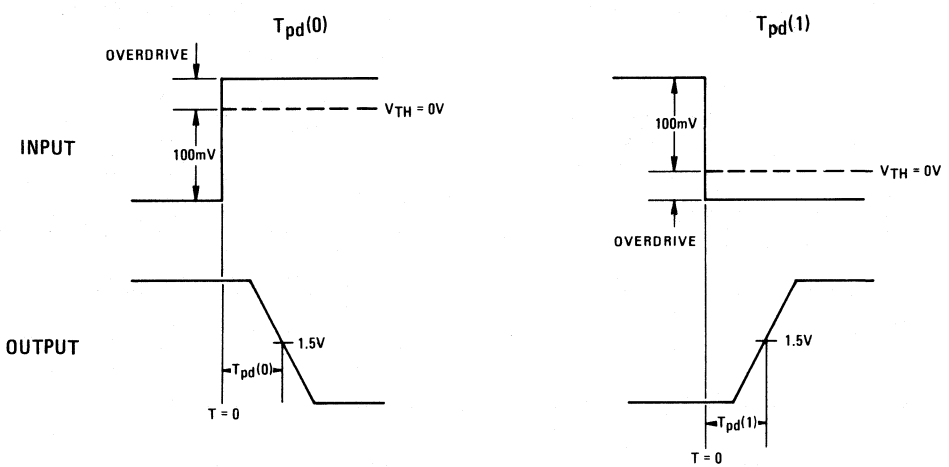
8. Derate by 5.8mW/°C above T_A = +75°C.

9. Electrical characteristics are guaranteed only under supply conditions shown.

10. Supply current (Logic) is guaranteed under either logic high or low state.

RESPONSE TIME TEST CIRCUITS



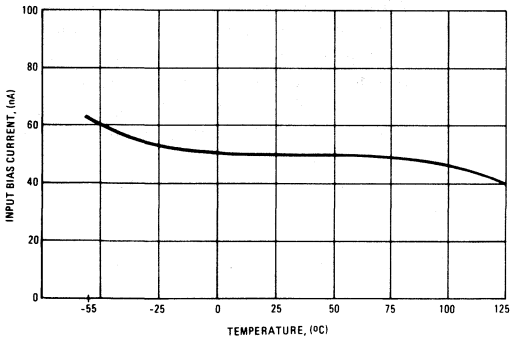


Input and output voltage waveforms for various input overdrives is shown on page 5.

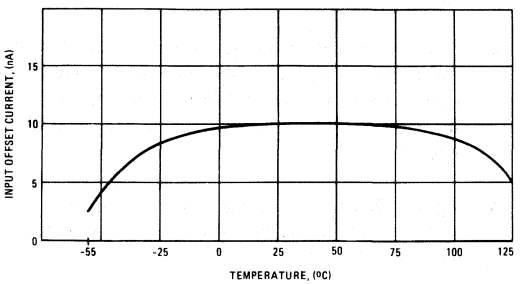
PERFORMANCE CURVES

$V+ = 15V$, $V- = -15V$, $V_{Logic}(+) = 5.0V$, $V_{Logic}(-) = 0V$, $T_A = +25^oC$, Unless Otherwise Stated.

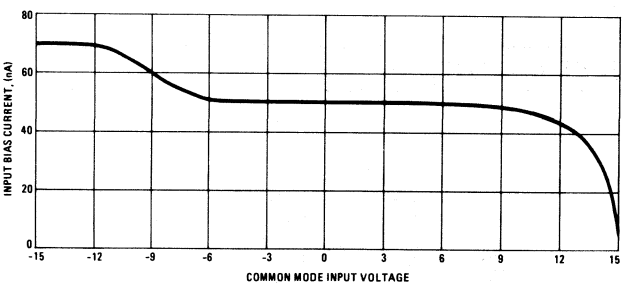
INPUT BIAS CURRENT vs. TEMPERATURE



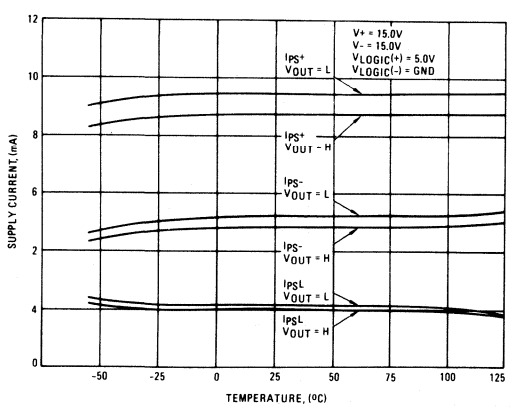
INPUT OFFSET CURRENT vs. TEMPERATURE



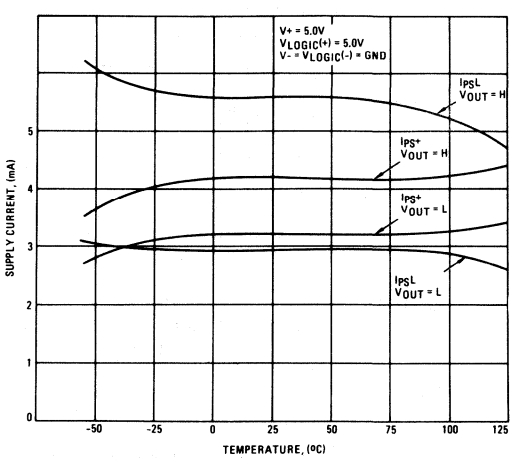
INPUT BIAS CURRENT vs. COMMON MODE INPUT VOLTAGE
($V_{DIFF.} = 0V$)



SUPPLY CURRENT vs. TEMPERATURE
FOR ±15V SUPPLIES AND +5V LOGIC SUPPLY

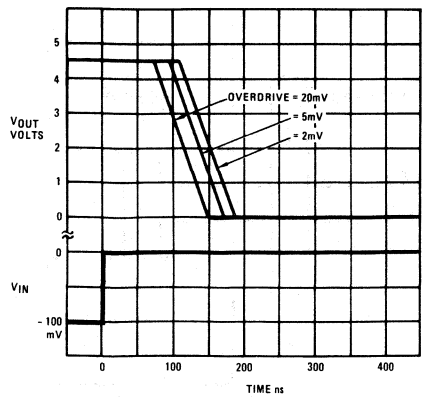


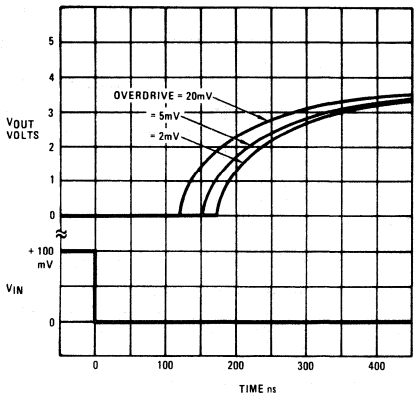
SUPPLY CURRENT vs. TEMPERATURE
FOR SINGLE +5V OPERATION



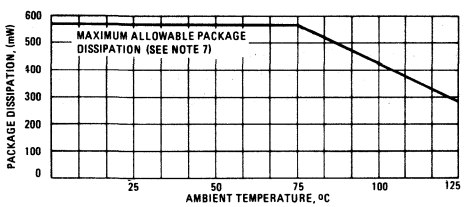
PERFORMANCE CURVES (continued)

RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

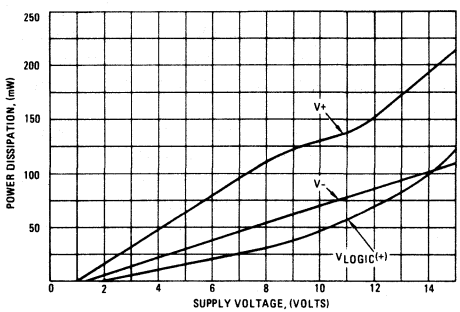




MAXIMUM PACKAGE DISSIPATION vs. $T_{AMBIENT}$



MAXIMUM POWER DISSIPATION vs. SUPPLY VOLTAGE (NO LOAD CONDITION)



APPLYING THE HA-4900/4905 COMPARATORS

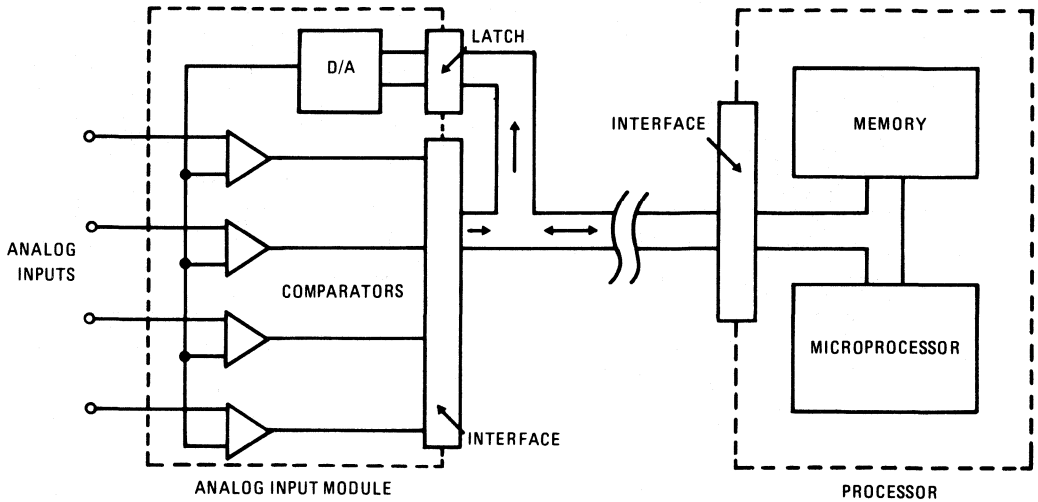
1. SUPPLY CONNECTIONS: This device is exceptionally versatile in working with most available power supplies. The voltage applied to the V+ and V- terminals determines the allowable input signal range; while the voltage applied to the V_L+ and V_L- determines the output swing. In systems where dual analog supplies are available, these would be connected to V+ and V-, while the logic supply and return would be connected to V_{Logic}+ and V_{Logic}-. The analog and logic supply commons can be connected together at one point in the system, since the comparator is immune to noise on the logic supply ground. A negative output swing may be obtained by connecting V_L+ to ground and V_L- to a negative supply. Bipolar output swings (15V P-P, max.) may be obtained using dual supplies. In systems where only a single logic supply is available (+5V to +15V), V+ and V_{Logic}+ may be connected together to the positive supply while V- and V_{Logic}- are grounded. If an input signal could swing negative with respect the V- terminal, a resistor should be connected in series with the input to limit input current to $< 5mA$ since the C-B junction of the input transistor would be forward biased.

2. UNUSED INPUTS: Inputs of unused comparator sections should be tied to a differential voltage source to prevent output "chatter".

3. CROSSTALK: Simultaneous high frequency operation of all other channels in the package will not affect the output logic state of a given channel, provided that its differential input voltage is sufficient to define a given logic state ($\Delta V_{IN} \geq \pm V_{OS}$). Low level or high impedance input lines should be shielded from other signal sources to reduce crosstalk and interference.

4. POWER SUPPLY DECOUPLING: Decouple all power supply lines with .01 μ F ceramic capacitors to a ground line located near the package to reduce coupling between channnels or from external sources.

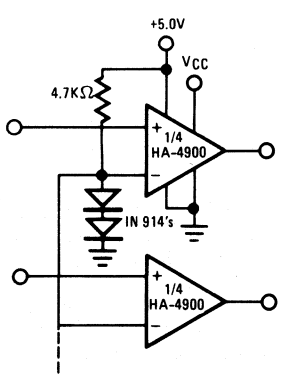
5. RESPONSE TIME: Fast rise time ($<$ 200ns) input pulses of several volts amplitude may result in delay times somewhat longer than those illustrated for 100mV steps. Operating speed is optimized by limiting the maximum differential input voltage applied, with resistor-diode clamping networks.



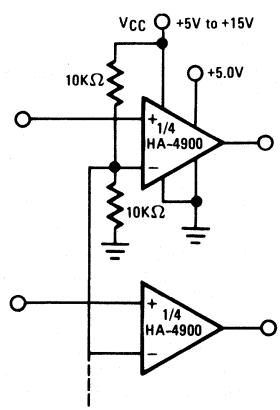
DATA ACQUISITION SYSTEM

In this circuit the HA-4900/4905 is used in conjunction with a D to A converter to form a simple, versatile, multi-channel analog input for a data acquisition system. In operation the processor first sends an address to the D to A, then the processor reads the digital word generated by the comparator outputs.

To perform a simple comparison, the processor sets the D to A to a given reference level, then examines one or more comparator outputs to determine if their inputs are above or below the reference. A window comparison consists of two such cycles with 2 reference levels set by the D to A. One way to digitize the inputs would be for the processor to increment the D to A in steps. The D to A address, as each comparator switches, is the digitized level of the input. While stairstepping the D to A is slower than successive approximation, all channels are digitized during one staircase ramp.



TTL TO CMOS

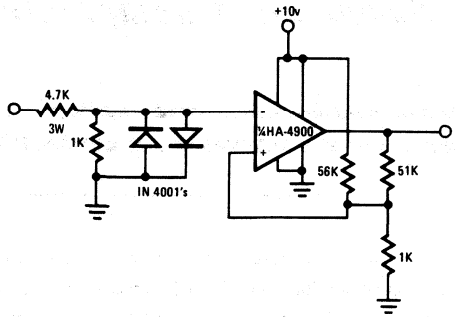


CMOS TO TTL

LOGIC LEVEL TRANSLATORS

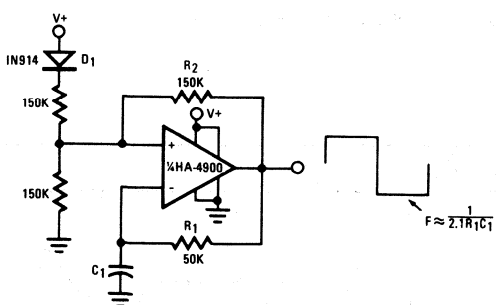
The HA-4900/4905 comparators can be used as versatile logic interface devices as shown in the circuits above. Negative logic devices may also be interfaced with appropriate supply connections.

If separate supplies are used for V- and V_{Logic}-, these logic level translators will tolerate several volts of ground line differential noise.



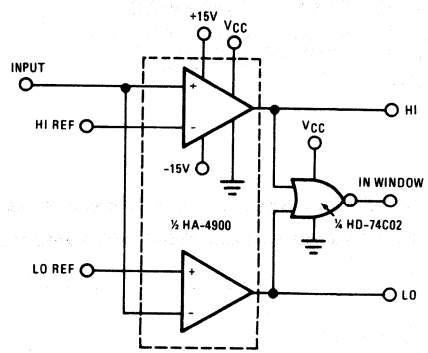
RS-232 TO CMOS LINE RECEIVER

This RS-232 type line receiver to drive CMOS logic uses a Schmitt trigger feedback network to give about 1 volt input hysteresis for added noise immunity. A possible problem in an interface which connects two equipments, each plugged into a different AC receptacle, is that the power line voltage may appear at the receiver input when the interface connection is made or broken. The two diodes and a 3 watt input resistor will protect the inputs under these conditions.



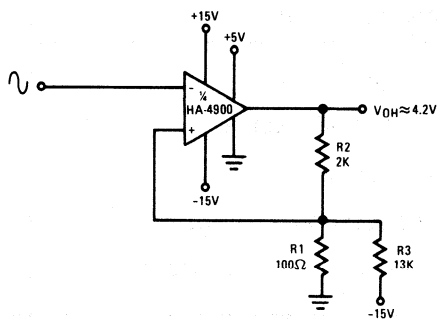
OSCILLATOR/CLOCK GENERATOR

This self-starting fixed frequency oscillator circuit gives excellent frequency stability. R_1 and C_1 comprise the frequency determining network while R_2 provides the regenerative feedback. Diode D_1 enhances the stability by compensating for the difference between V_{OH} and V_{Supply}. In applications where a precision clock generator up to 100kHz is required, such as in automatic test equipment, C_1 may be replaced by a crystal.



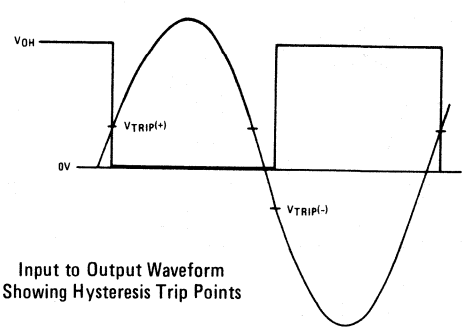
WINDOW DETECTOR

The high switching speed, low offset current and low offset voltage of the HA-4900/4905 makes this window detector circuit extremely well suited to applications requiring fast, accurate, decision-making. The circuit above is ideal for industrial process system feedback controllers or "out-of-limit" alarm indicators.



SCHMITT TRIGGER (ZERO CROSSING DETECTOR WITH HYSTERESIS)

This circuit has a 100mV hysteresis which can be used in applications where very fast transition times are required at the output even though the signal input is very slow. The hysteresis loop also reduces false triggering due to noise on the input. The waveforms below show the trip points developed by the hysteresis loop.



Input to Output Waveform
Showing Hysteresis Trip Points

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HA-4920/4925

High Speed Quad Comparator

2

FEATURES

- FAST RESPONSE TIME
- LOW OFFSET VOLTAGE
- STANDARD POWER SUPPLIES
- ACTIVE PULL-UP/PULL-DOWN OUTPUT CIRCUIT – NO EXTERNAL RESISTORS REQUIRED
- TTL AND ECL COMPATIBLE

APPLICATIONS

- A/D CONVERTERS
- THRESHOLD DETECTOR
- ZERO-CROSSING DETECTOR
- LOGIC SYSTEM INTERFACES
- HIGH FREQUENCY OSCILLATORS

DESCRIPTION

HA-4920/4925 are monolithic, quad, high speed comparators offering a combination of speed, precision, and flexibility never before available in a quad comparator. 40ns response time and 2.0mV offset voltage makes these comparators ideally suited for precise signal level detection and fast response times to large and small input signal levels. These dielectrically isolated devices employ unique input/output stages which prevent troublesome ground coupling inherent in combined analog/digital systems.

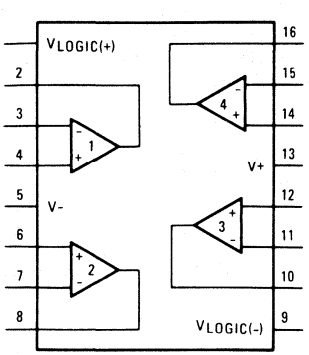
The flexibility/speed of HA-4920/4925 assures easy application in fast data acquisition systems, analog to logic interface networks, and test equipment.

Both devices are available in 16 pin dual-in-line ceramic packages. The HA-4920 operates from -55°C to +125°C and the HA-4925 operates over a 0°C to +75°C temperature range.

PINOUT

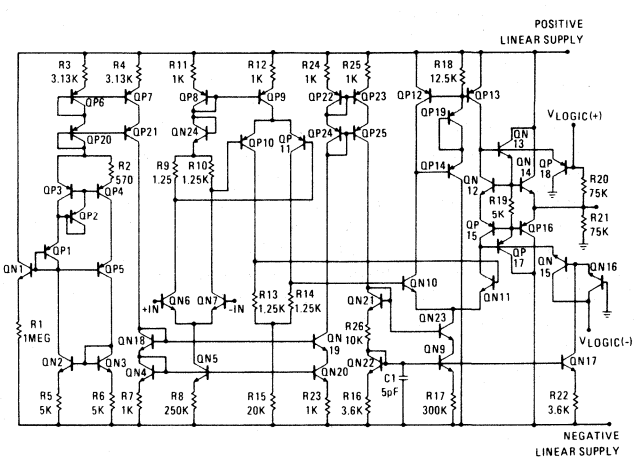
Package Code 4Z

QUAD COMPARATOR



TOP VIEW

SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage between V+ and V-	40V
Voltage between $V_{Logic}(+)$ and $V_{Logic}(-)$	7V
Differential Input Voltage	±6V
Peak Ouput Current	50mA
Internal Power Dissipation (Note 2)	850mW
Storage Temperature Range	$-65^oC \leq T_A \leq 150^oC$
Positive and Negative Voltage Clamp	5V below Supply Voltage

ELECTRICAL CHARACTERISTICS

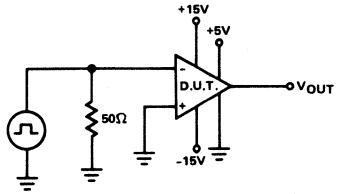
V+ = +15.0V $V_{Logic}(+)$ = 5.0V
V- = -15.0V $V_{Logic}(-)$ = GND

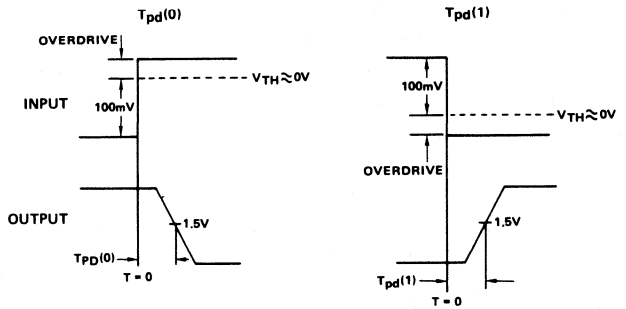
		HA-4920: -55°C/+125°C			HA-4925: 0°C/+75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 3)	+25°C		2.0	3.0		4.0	6.0	mV
	Full			4.0			8.0	mV
Input Offset Current	+25°C		.5	1.5		1.5	2.0	μa
	Full			2.0			3.0	
Input Bias Current	+25°C		.8	6.0		2.0	8.0	μa
	Full			8.0			10.0	μa
Input Sensitivity (Note 4)	Full		.4	.6		.7	.8	mV
Common Mode Range (CMR)	Full	±10			±10			V
Large Signal Voltage Gain	+25°C		25K			25K		V/V
Response Time Tpd0 (Note 5)	+25°C		35	50		35	50	ns
Response Time Tpd1 (Note 5)	+25°C		30	50		30	50	ns
Output Voltage Level (Note 6) V_{OL}	Full		.15	.4		.15	.4	V
Output Voltage Level (Note 6) V_{OH}	Full	3.5	4.2		3.5	4.2		V
Output Current I_{Sink} (Note 7)	Full	3.2			3.2			mA
Output Current I_{Source} (Note 7)	Full	3.2			3.2			mA
Power Supply Current I_{CC+}	+25°C		14	20		14	20	mA
Power Supply Current I_{CC-}	+25°C		10	20		10	20	mA
Power Supply Current I_{Logic+}	+25°C		4.8	8.0		4.8	8.0	mA

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Derate by 5.8 mW/°C above +75°C.
3. Minimum differential input voltage required to ensure a defined output state.
4. $R_S \leq 200$ ohms; $V_{in} \leq$ Common Mode Range. Input sensitivity is the worst case minimum differential input voltage required to guarantee a given output logic state, after offset voltage is nulled. This parameter includes the effects of offset current, common mode rejection, and voltage gain.
5. For $T_{pd}(1)$; 100mV input step, -5mV overdrive. For $T_{pd}(0)$; -100mV input step, +5mV overdrive. Frequency ≈100Hz; Duty Cycle ≈50%; Inverting input driven. See Test Circuit below.
6. For V_{OH} and V_{OL}: I_{Sink} = 3.5mA, I_{Source} = 3.0mA. For other values of V_{Logic}; V_{OH} (min.) = V_{Logic} + -1.5V.
7. Per Comparator.

RESPONSE TIME TEST CIRCUITS



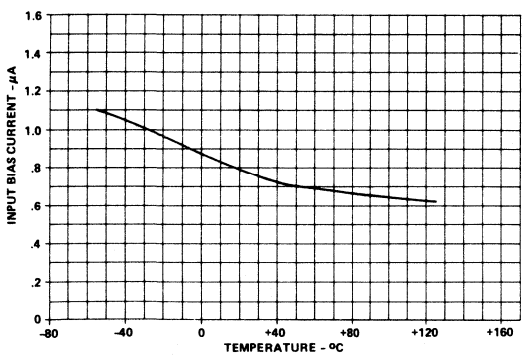


Input and output voltage waveforms for various input overdrives are shown on the following page.

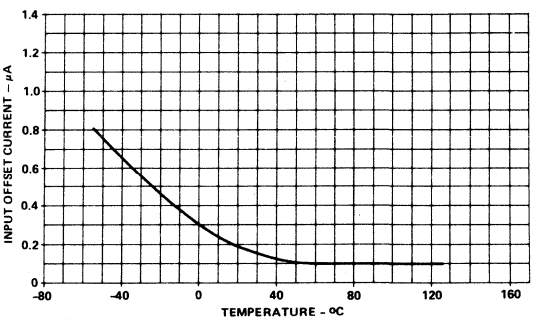
PERFORMANCE CURVES

V+ = 15V, V- = -15V, $V_{Logic}(+)$ = 5.0V, $V_{Logic}(-)$ = 0V, T_A = +25°C, Unless Otherwise Stated.

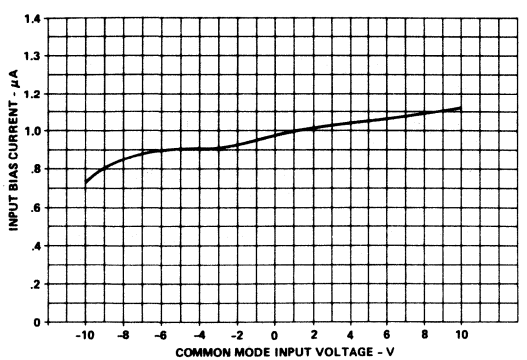
INPUT BIAS CURRENT VS. TEMPERATURE



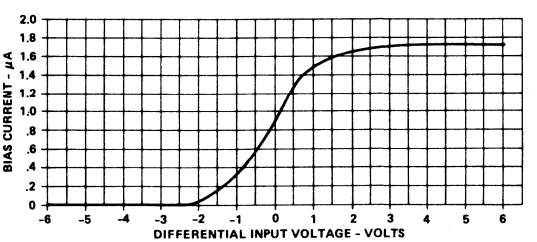
INPUT OFFSET CURRENT VS. TEMPERATURE



INPUT BIAS CURRENT VS. COMMON MODE VOLTAGE

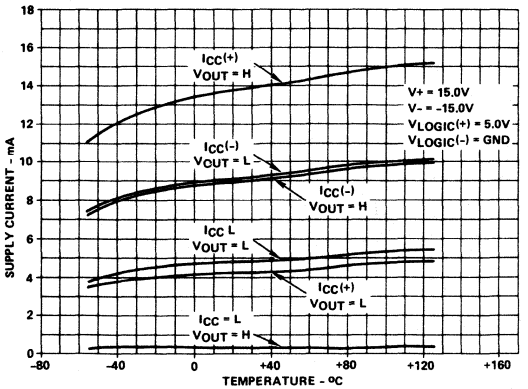


INPUT BIAS CURRENT VS. DIFFERENTIAL INPUT VOLTAGE

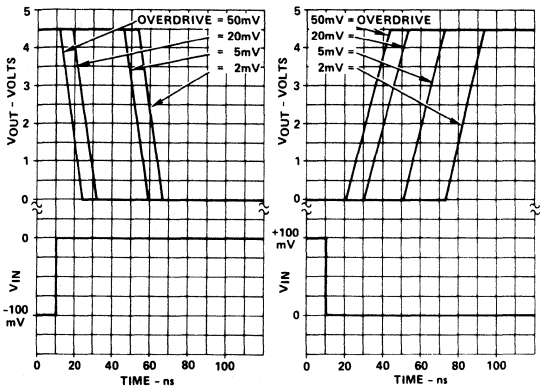


PERFORMANCE CURVES (cont'd)

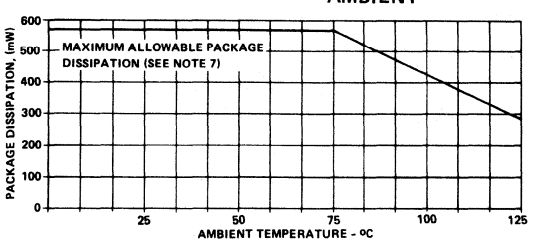
SUPPLY CURRENT VS. TEMPERATURE FOR ±15V SUPPLIES AND +5V LOGIC SUPPLY



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



MAXIMUM PACKAGE DISSIPATION VS. $T_{AMBIENT}$



APPLYING THE HA-4920/25

1. SUPPLY CONNECTIONS: This device is exceptionally versatile in working with most available power supplies. The voltage applied to the V+ and V- terminals determines the allowable input signal range; while the voltage applied to the V_L+ and V_L- determines the output swing. In systems where dual analog supplies are available, these would be connected to V+ and V-, while the logic supply and return would be connected to V_{Logic}+ and V_{Logic}-. The analog and logic supply commons can be connected together at one point in the system, since the comparator is immune to noise on the logic supply ground. A negative output swing may be obtained by connecting V_L+ to ground and V_L- to a negative supply. Bipolar output swings (5V P-P, max.) may be obtained using dual supplies. Applied input signals should not exceed V_{Supply} and the maximum differential input voltage values.

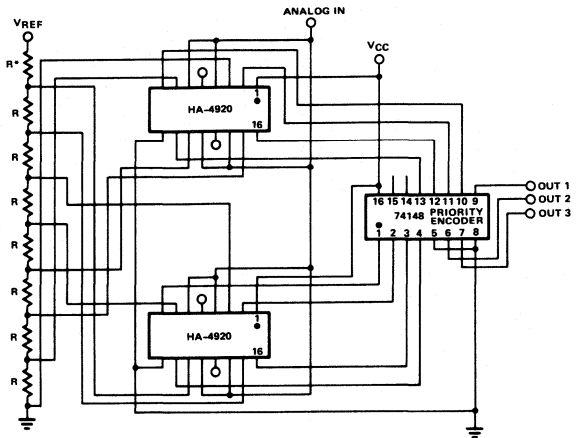
2. UNUSED INPUTS: Inputs of unused comparator sections should be tied to a differential voltage source to prevent output "chatter". Differential voltage values should exceed the offset voltage plus input sensitivity voltage values for a particular device.

3. CROSSTALK: Simultaneous high frequency operation of all other channels in the package will not affect the output logic state of a given channel, provided that its differential input voltage is sufficient to define a given logic state ($\Delta V_{IN} \geq \pm V_{OS}$). Low level or high impedance input lines should be shielded from other signal sources to reduce crosstalk and interference.

4. POWER SUPPLY DECOUPLING: Decouple all power supply lines with .01 μF ceramic capacitors to a ground line located near the package to reduce coupling between channels or from external sources.

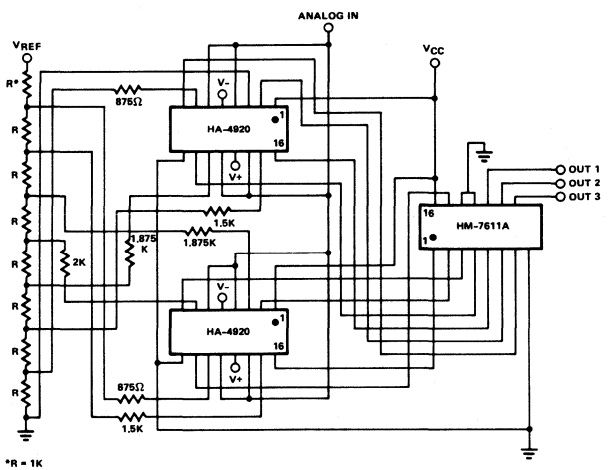
5. R.F.I.: High speed comparators may generate high frequency oscillations when the applied differential input voltage is less that the offset voltage plus input sensitivity value. This can be minimized by adding positive feedback hysteresis networks (see Harris App. Note 505). Alternately, ferrite beads surrounding the input and output lines will help reduce RF interference to other circuitry.

3 BIT PARALLEL COMPARATOR A/D CONVERTER USING TTL LOGIC



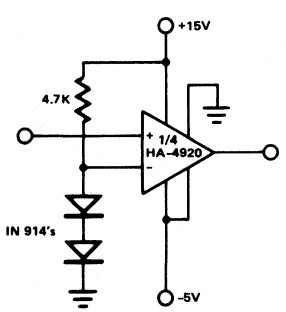
*R = 1K
Input Balancing Resistors Optional
(See Next Figure)
Experimental Results ≈ 50ns

3 BIT PARALLEL COMPARATOR A/D CONVERTER USING 256 x 4 PROM



*R = 1K

LOGIC LEVEL TRANSLATOR TTL TO ECL



TRUTH TABLE FOR 3 BIT PARALLEL COMPARATOR A/D CONVERTER

ENCODER/PROM INPUTS							OUTPUTS		
1	2	3	4	5	6	7	0	1	2
0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	1	1	0
1	1	1	1	0	0	0	0	0	1
1	1	1	1	1	0	0	1	0	1
1	1	1	1	1	1	0	0	1	1
1	1	1	1	1	1	1	1	1	1

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HA-4950

Precision High Speed Comparator

Preliminary

FEATURES

- FAST RESPONSE TIME 40ns
- TOTAL UNCERTAINTY BAND 1/8 LSB
- LOW OFFSET VOLTAGE 1mV
- STROBE AND OUTPUTS TTL COMPATIBLE

APPLICATIONS

- HIGH SPEED A/D CONVERTERS
- ZERO-CROSSING DETECTOR
- THRESHOLD DETECTOR
- ANALOG INTERFACES FOR MICROPROCESSORS

DESCRIPTION

HA-4950 is a very fast precision comparator incorporating a strobe controlled, digital output buffer. Constructed using the Harris high frequency bipolar dielectric isolation process, this device offers unprecedented specifications for input offset voltage, total uncertainty band (1/8 LSB, 10 volt full scale output, 12 bit system) and response time, (50nsec).

This monolithic comparator consists of three amplifier stages, a latch, strobe control circuitry and a digital output stage (TTL compatible). In operation and with the strobe input TTL logic level high, both outputs remain high while the amplifiers sense, amplify, and track differential input signals. With a strobe transition of high to low state, the latch is activated and its output is transferred to the complementary output stages, and digital outputs (Q and $\overline{Q}$) will reflect the polarity of the differential input signal (see Timing Diagram and Truth Table).

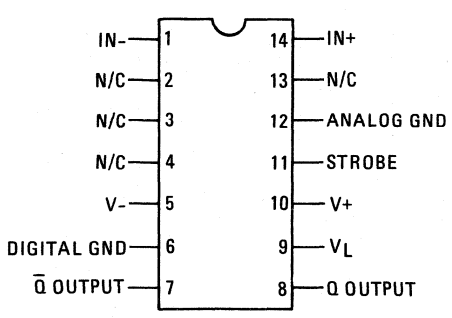
The HA-4950 is ideally suited for applications requiring accurate and fast detection of low level signals such as high speed A/D converters. Other applications include zero-crossing and threshold detectors.

This device is available in a 14 pin dual-in-line ceramic package. HA-4950-2 operates from -55°C to +125°C while the HA-4950-5 operates from 0°C to +75°C.

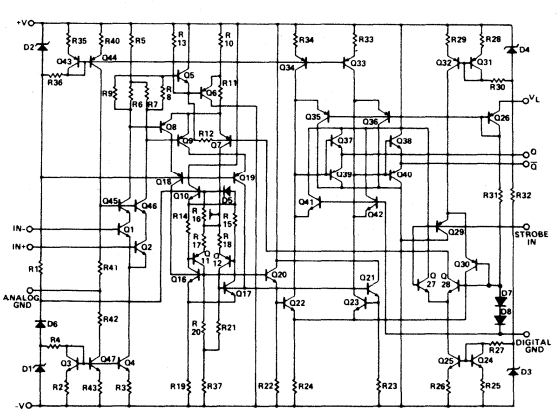
PINOUT

Package Code 4D, LA

TOP VIEW



SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage Between V+ and V-	40V	Power Dissipation (Note 2)	549mW
Logic Supply Voltage	V+	Operating Temperature Range	
Differential Input Voltage	±6V	HA-4950-2	-55°C to +125°C
Strobe Input High	+7V	HA-4950-5	0°C to +75°C
Low	-5V	Storage Temperature Range	-65°C ≤ T_A ≤ +150°C
Peak Output Current	±10mA		

ELECTRICAL CHARACTERISTICS

V+ = 15V
V- = -15V
V_L = 5V

		HA-4950-2 -55°C to +125°C			HA-4950-5 0°C to +75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Characteristics								
Offset Voltage (Note 3)	25°C		1.0	2.25		1.0	2.25	mV
	Full			2.8			2.8	mV
Offset Current	25°C		0.25	1.5		0.25	1.5	μA
	Full			3.5			3.5	μA
Bias Current	25°C		1.25	3.0		1.25	3.0	μA
	Full			7.0			7.0	μA
Input Resistance	25°C	15	40		15	40		KΩ
Analog Input Signal Range (Note 4)	Full			±0.6			±0.6	V
Strobe Input Voltage								
Logic "1"	Full	2.0			2.0			V
Logic "0"	Full			0.8			0.8	V
Strobe Input Current								
Logic "1"	25°C		5	15		5	15	μA
	Full			30			30	μA
Logic "0"	25°C		-20	-60		-20	-60	μA
	Full			-120			-120	μA
Transfer Characteristics								
Total Uncertainty Band (Note 5) 12 Bits, 10V	Full			1/8			1/8	LSB
Strobe Response (Note 6)								
T_{pd0}	25°C		40	60		40	60	ns
	Full			65			65	ns
Strobe Recovery (Note 6)								
T_{pd1}	25°C		20	30		20	30	ns
	Full			35			35	ns
Response Time Difference Q to $\overline{Q}$ (Note 7)	Full			1			1	ns

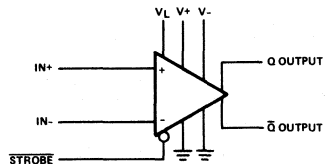
PARAMETER	TEMP	HA-4950-2 -55°C to +125°C MIN	TYP	MAX	HA-4950-5 0°C to +75°C MIN	TYP	MAX	UNITS
Output Characteristics								
Q, $\overline{Q}$ Output Voltage								
Logic "1" (I_{source} = 5mA)	Full	4.0			4.0			V
Logic "0" (I_{sink} = 5mA)	Full			0.45			0.45	V
Q, $\overline{Q}$ Output Current								
I_{source} (Logic "1" 4.0V)	Full	5			5			mA
I_{sink} (Logic "0" 0.8V)	Full	5			5			mA
Power Supply Characteristics								
Supply Voltage Range								
V+	Full	+13.5	+15	+16.5	+13.5	+15	+16.5	V
V-	Full	-13.5	-15	-16.5	-13.5	-15	-16.5	V
V_L	Full	+4.5	+5	+5.5	+4.5	+5	+5.5	V
Supply Current								
$I_{\pm}$ (Strobe High)	25°C		11	14		11	14	mA
$I_{\pm}$ (Strobe Low)	25°C		14	18		14	18	mA
I_L	25°C		1.4	1.7		1.4	1.7	mA
Power Supply Rejection Ratio	25°C		100			100		dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. No derating neccessary up to +125°C.
3. Minimum differential input voltage required to ensure a defined output state.
4. Includes any combination of differential and common mode input signals. With full range differential signal (±600mV) applied, common mode voltages from 0V to -8.4V can be tolerated.
5. Includes errors induced by dynamic uncertainty (thermal hysteresis) and quasi-static uncertainty (noise, etc.) after offset voltage has been nulled. Maximum value is referred to a 10V full scale output, 12 bit system.
6. See response time circuit and waveforms section of data sheet for conditions.
7. Time difference due to match between the Q, $\overline{Q}$ output stages.

FUNCTIONAL DIAGRAM/RESPONSE TIME TEST CIRCUIT

FUNCTIONAL DIAGRAM

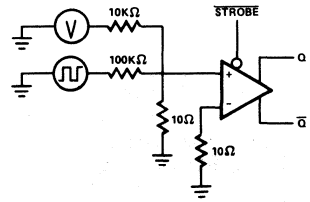


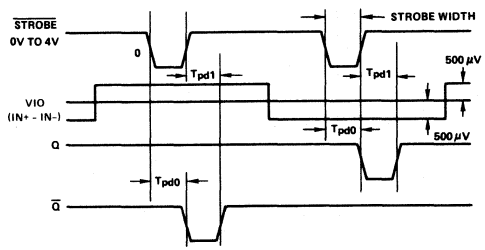
TRUTH TABLE

STROBE	INPUTS	OUTPUT Q	OUTPUT Q̄
H	Don't Care	H	H
↓	IN+ > IN-	H	L
↓	IN+ < IN-	L	H
L	Don't Care	Q_0	$\bar{Q}_0$

Q_0 – The Latched State

RESPONSE TIME TEST CIRCUIT

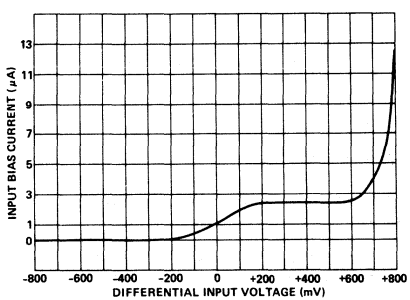




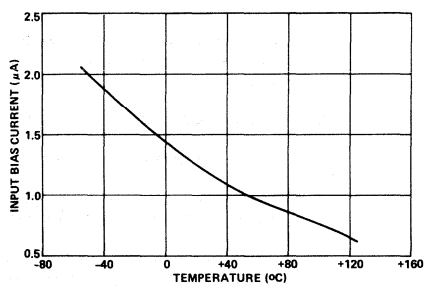
PERFORMANCE CURVES

V+ = 15V, V- = -15V, V_L = 5V, T_A = +25°C, Unless otherwise stated.

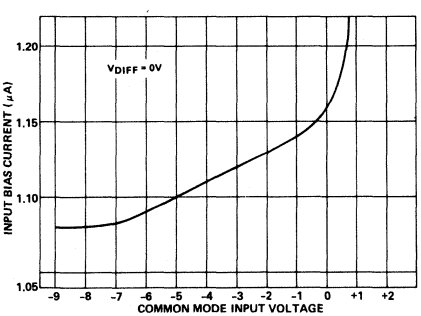
INPUT BIAS CURRENT VS. DIFFERENTIAL INPUT VOLTAGE



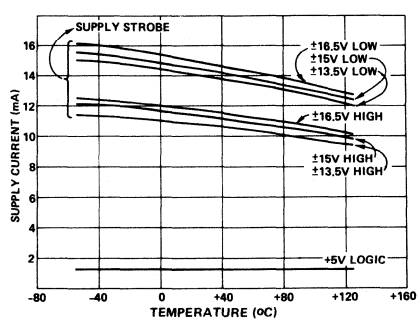
INPUT BIAS CURRENT VS. TEMPERATURE



INPUT BIAS CURRENT VS. COMMON MODE INPUT VOLTAGE



SUPPLY CURRENT VS. TEMPERATURE FOR ± 16.5V, ± 15V, ± 13.5V & +5V LOGIC



① MAXIMIZED SPEED/PRECISION

For optimized dynamic performance, the grounding and decoupling scheme shown in Figure 1, Applications Section, should be used. Decoupling capacitors should be connected close to the device (preferably to the device pins) and should be Tantalum or Electrolytics bypassed with ceramic types for best noise rejection. Alternately, suppression filters such as Erie 1201-052 can be used for decoupling with excellent results.

② INPUT SIGNAL CONDITIONING

In applications where input signals may exceed the input signal range specification, it is recommended that diode clamping schemes be used (see Figures 2 and 3, Applications Section). The diodes used should have low turn-on voltage and high switching speed characteristics such as Schottky Barrier diodes.

③ STROBE SIGNAL SHIELDING

To ensure HA-4950's maximum performance, point-to-point connections between strobe signal and strobe input should be minimized to prevent external transient interference. Alternately, shielded cable should be used if minimal distances cannot be obtained.

APPLICATIONS

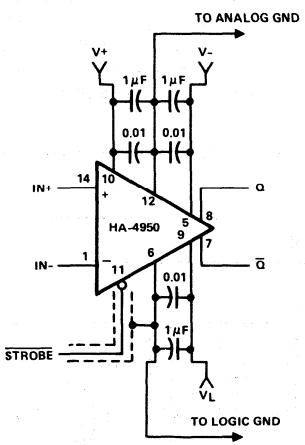


FIGURE 1.

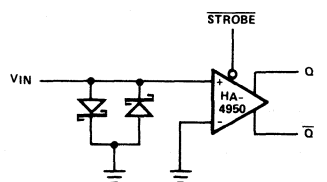


FIGURE 2. ZERO-CROSSING DETECTOR

HA-4950's 1mV offset voltage and very low total uncertainty band is extremely well suited for high speed zero crossing detection. Figure 2 shows HA-4950 as a simple zero crossing detector with input diode protection. Noise and system transients should be minimized at the reference input for best performance results. The Truth Table shown on page 2 applies to this circuits' operation.

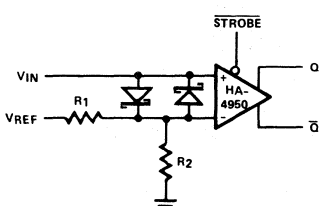


FIGURE 3. THRESHOLD DETECTOR

Similar to the zero crossing detector, this cirucit shows HA-4950 with input diode limiting comparing input signals to a voltage reference other than 0 volts. R_1 and R_2 establishes the reference input. Effects of bias current can be minimized by adding a resistor in series with the positive input and equal to R_2.

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
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HA-5100/5105

Wideband, JFET Input, Operational Amplifier

2

FEATURES

- LOW INPUT OFFSET VOLTAGE 0.5mV
- LOW OFFSET DRIFT . . . . . 5μV/^{o}C
- LOW INPUT BIAS CURRENT 50pA
- LARGE VOLTAGE GAIN . . . . . 150K V/V
- WIDE BANDWIDTH 18MHz
- HIGH SLEW RATE 8V/μsec
- FAST LARGE SIGNAL SETTLING TIME: 1.7μsec

APPLICATIONS

- PRECISION, HIGH SPEED, DATA ACQUISITION SYSTEMS
- PRECISION SIGNAL GENERATION
- PULSE AMPLIFICATION

GENERAL DESCRIPTION

The HA-5100/5105 are monolithic wideband operational amplifiers manufactured with FET/Bipolar technologies and dielectric isolation. Precision laser trimming of the input stage complements the amplifier high frequency capabilities with excellent input characteristics.

The HA-5100/5105 offer a number of important advantages over similar FET input op amps from other manufacturers. In addition to superior bandwidth and settling characteristics the Harris devices have quite constant slew rate, bandwidth, and settling characteristics over the operating range. This provides the user predictable performance in applications where settling time, full power bandwidth, closed loop bandwidth, or phase shift is critical. The slewing waveform is symmetrical to provide reduced distortion. Note also that Harris specifies all parameters at ambient (rather than junction) temperature to provide the designer meaningful data to predict actual operating performance.

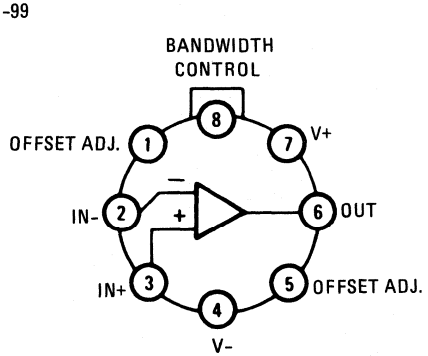
Complementing HA-5100/5105's predictable and excellent dynamic characteristics are very low input offset voltage, very low input bias current, and extremely high input impedance. This ideal combination of features make these amplifiers most suitable for precision, high speed, data acquisition system designs and for a wide variety of signal conditioning applications.*

* -2 denotes a range of -55^{o}C to +125^{o}C and -5 denotes a 0^{o}C to +75^{o}C range.

PINOUT

TOP VIEW **Package Code 2A**

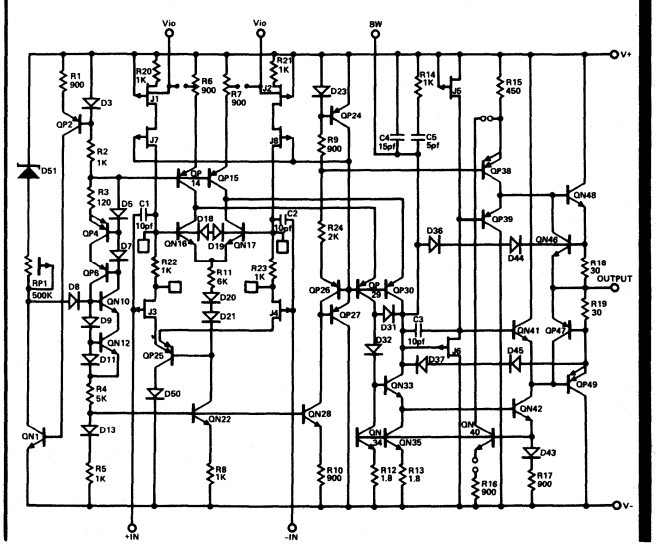
TO-99



CASE CONNECTED TO V-

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on page 1-4.

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage Between V+ and V-	40V
Differential Input Voltage	+40V
Peak Output Current	Full Short Circuit Protection
Internal Power Dissipation (Note 2)	300mW
Storage Temperature Range	-65°C to +150°C

ELECTRICAL CHARACTERISTICS

V+ = 15VDC; V- = -15VDC
Parameters are guaranteed at indicated ambient temperature after warm-up.

		HA-5100-2 -55°C to +125°C			HA-5100-5 0°C to +75°C			HA-5105-5 0°C to +75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS											
*Offset Voltage	+25°C		0.5	1.0		0.5	1.0		0.5	1.5	mV
	Full		0.50	2.0		0.50	2.0		0.75	3.5	mV
Offset Voltage Average Drift	Full		5			10			15		µV/°C
Bias Current	+25°C		20	50		20	50		50	100	pA
	Full		5	10			10		10	20	nA
Offset Current	+25°C		2	10		2	10		5	50	pA
	Full		2	5		2	5		5	10	nA
Input Resistance	+25°C		10^{12}			10^{12}			10^{12}		Ω
Common Mode Range	Full	±10	±11		±10	±11		±10	±10.5		V
TRANSFER CHARACTERISTICS											
*Large Signal Voltage (Note 3)	+25°C	75K	150K		75K	150K		50K	100K		V/V
	Full	60K	100K		60K	100K		40K	80K		V/V
*Common Mode Rejection Ratio (Note 4)	Full	80	86		80	86		80	86		dB
Gain Bandwidth Product at A_V = 10	Full		18			18			18		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 5)	+25°C	±12	±13		±12	±13		±11	±12		V
	Full	±12	±13		±12	±13		±11	±12		V
Short Circuit Output Current (Note 6)	Full	±10	±15		±10	±15		±8	±15		mA
Full Power Bandwidth (Note 7)	+25°C	90	150		90	150		75	125		kHz
Output Resistance (Note 8)	+25°C		30			30			40		Ω
TRANSIENT RESPONSE (Note 9)											
Rise Time	+25°C		15	35		15	35		20		nsec
Slew Rate	+25°C	6	8		6	8		5	8		V/µsec
Settling Time (Note 10)	+25°C		1.7			1.7			2.0		µsec
POWER SUPPLY CHARACTERISTICS											
*Supply Current	Full		5	7		5	7		6	8	mA
*P.S.R.R. (Note 11)	Full	80	86		80	86		80	86		dB

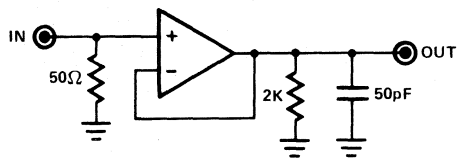
* 100% tested for Dash 8. All other parameters for design information only.

NOTES

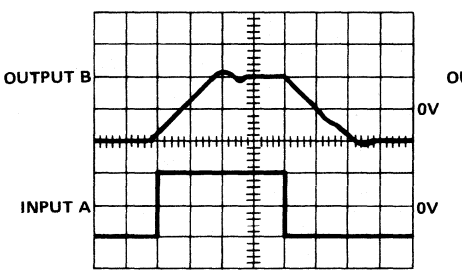
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Derate at 6.8 mW/°C for operation at ambient temperatures above +75°C.
3. $V_{OUT} = \pm 10V$; $R_L = 2K$.
4. $V_{CM} = \pm 10V$ D.C.
5. $R_L = 10K$.
6. $V_{OUT} = 0V$.
7. $R_L = 2K$; Full power bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{SLEW\ RATE}{2\pi V_{PEAK}}$.
8. Output resistance measured under open loop conditions.
9. Refer to test circuits section of the data sheet.
10. Settling time is measured to 0.1% of final value for a 10 volt output step and $A_V = -1$.
11. $V_{SUPP} = \pm 10V$ D.C. to $\mp 20V$ D.C.

TEST CIRCUITS

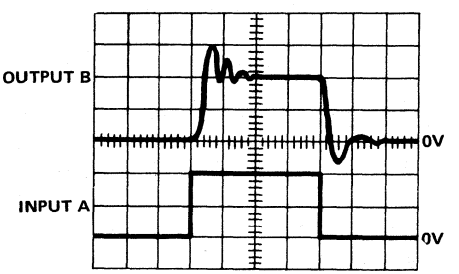
SLEW RATE AND TRANSIENT RESPONSE TEST CIRCUIT



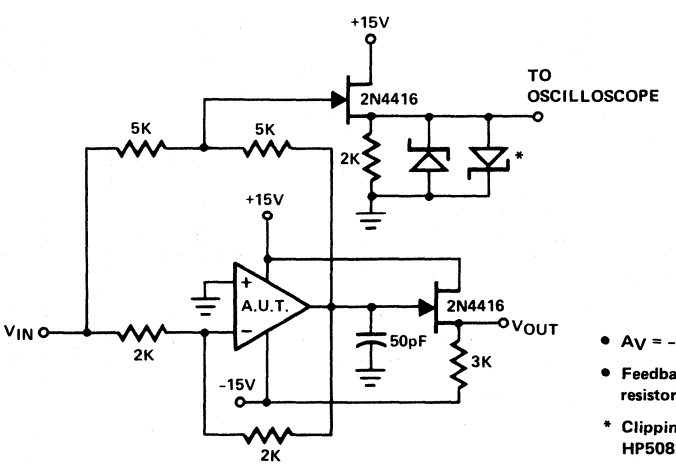
LARGE SIGNAL RESPONSE
Vertical Scale: (Volts: 5V/Div.)
Horizonal Scale: (Time: 500ns/Div.)



SMALL SIGNAL RESPONSE
Vertical Scale: (Volts: 100mV/Div.)
Horizonal Scale: (Time: 100ns/Div.)



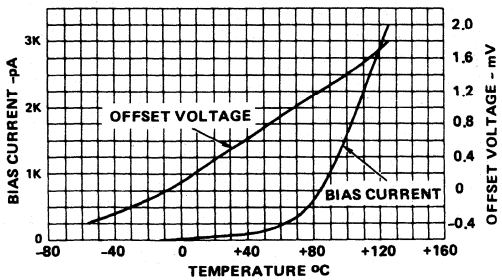
SETTLING TIME CIRCUIT



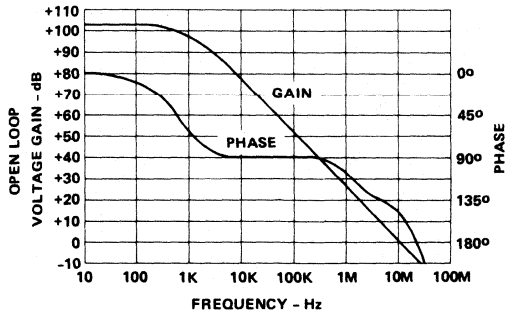
- $A_V = -1$.
- Feedback and summing resistors should be 0.1%.
- * Clipping diodes are optional. HP5082-2810 recommended.

V+ = +15V, V- = -15V, T_A = +25°C UNLESS OTHERWISE STATED.

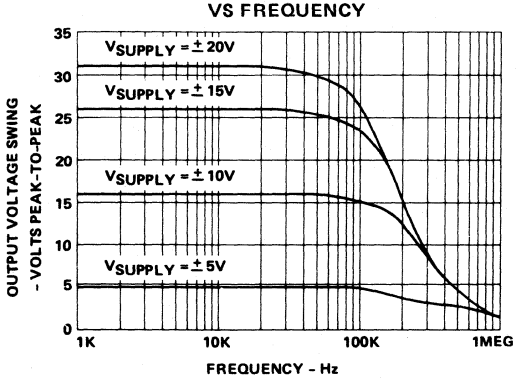
INPUT OFFSET VOLTAGE AND BIAS CURRENT VS TEMPERATURE



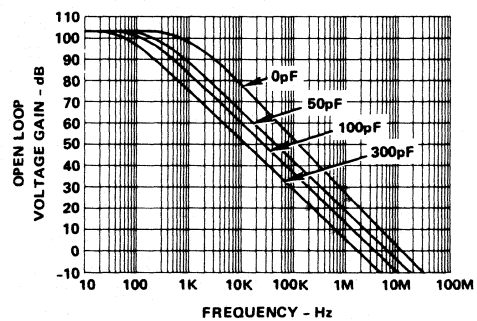
OPEN LOOP FREQUENCY RESPONSE



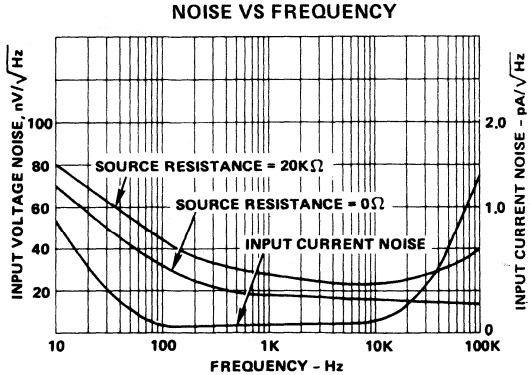
OUTPUT VOLTAGE SWING VS FREQUENCY



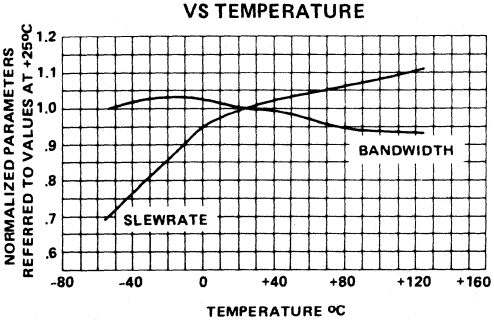
OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS BANDWIDTH CAPACITANCES



INPUT VOLTAGE AND CURRENT NOISE VS FREQUENCY

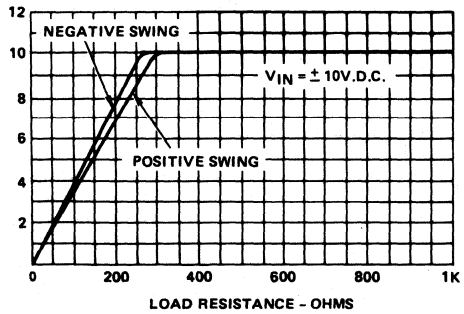


NORMALIZED AC PARAMETERS VS TEMPERATURE

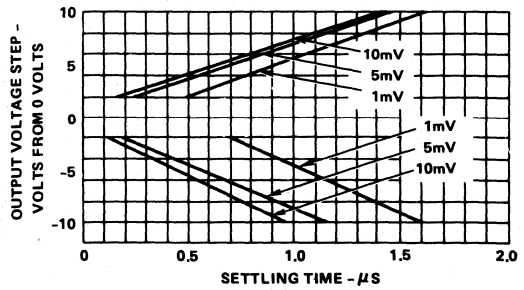


2

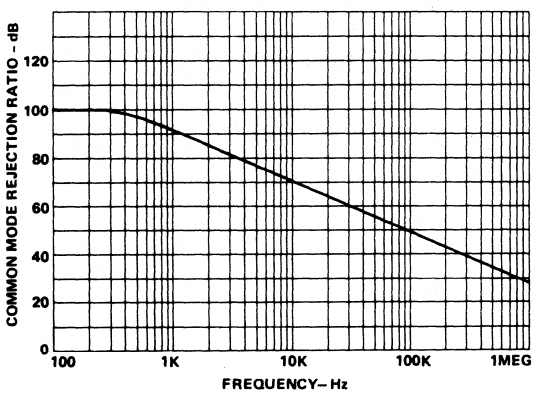
OUTPUT VOLTAGE SWING
VS LOAD RESISTANCE



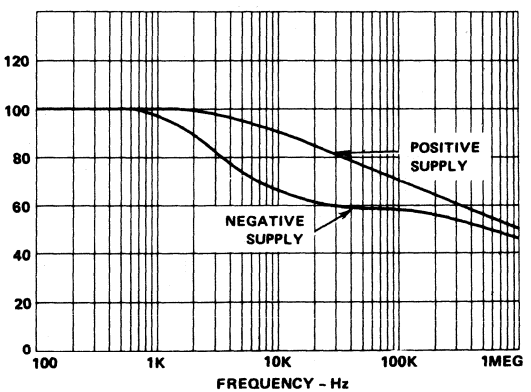
SETTLING TIME FOR VARIOUS
OUTPUT STEP VOLTAGES



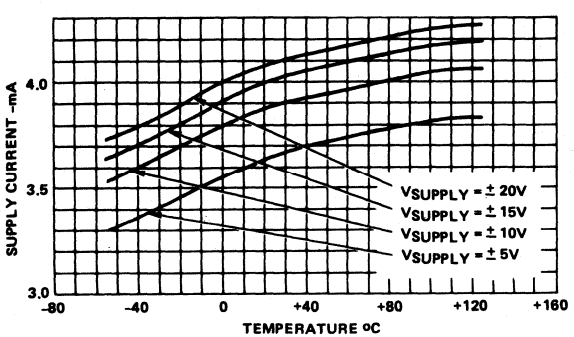
COMMON MODE REJECTION
RATIO VS FREQUENCY



POWER SUPPLY REJECTION
RATIO VS FREQUENCY



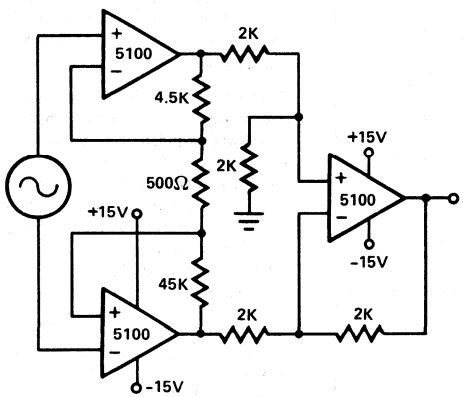
POWER SUPPLY CURRENT
VS TEMPERATURE



1. POWER SUPPLY DECOUPLING: Although not absolutely necessary, it is recommended that all power supply lines be decoupled with .01 μF ceramic capacitors to ground. Decoupling capacitors should be located as near to the amplifier terminals as possible.
2. STABILITY CONSIDERATIONS: In applications where large value feedback resistors are used, a small capacitor ($\approx$ 3pF) may be needed in parallel with the feedback resistor to neutralize the pole introduced by the input capacitance.
3. HEAVY CAPACITIVE LOADS: When driving heavy capacitive loads ($\geq$ 100pF) a small resistor ($\approx$100Ω) should be connected in series with the output and inside the feedback loop.
4. OFFSET VOLTAGE NULLING: Offset nulling, if required, is accomplished with a 100KΩ pot between pins 1 and 5; wiper to V+. Alteration of initial offset voltage may affect the temperature coefficient of the offset voltage.

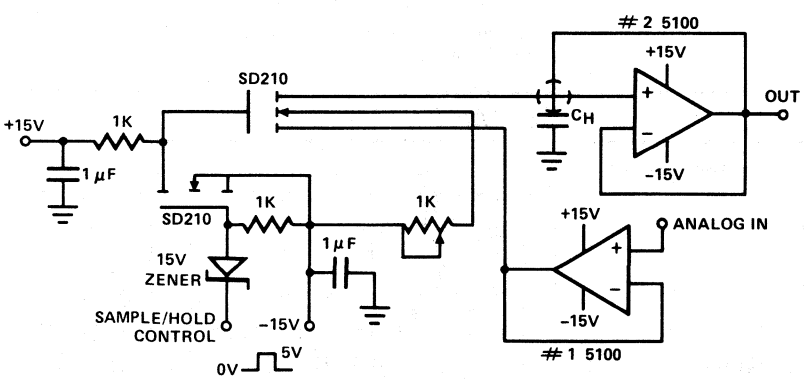
APPLICATIONS

PRECISION INSTRUMENTATION AMPLIFIER (A_V = 100)



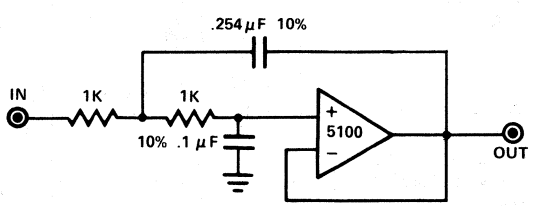
Experimental Results
Yielded 80dB CMRR.
V_{IO} drift < 20μV/°C.

PRECISION/FAST SAMPLE/HOLD CIRCUIT



Experimental Results:
V_{IN} = 10 volt step
C_H = 1000pF
Acquisition Time = 0.4μs (0.1%)
Charge Injection = 30pC
Drift Current = 320pA
Switching Spikes $\approx$ 200mV

1KHz SALLEN AND KEY FILTER



Experimental Results:
F_C = 1KHz
Q = 20
-3dB $\approx$ 1.1KHz
-20dB $\approx$ 3.4KHz

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HA-5110/5115

Wideband, JFET Input, Uncompensated, Operational Amplifier

2

FEATURES

- WIDE GAIN BANDWIDTH 60MHz
- HIGH SLEW RATE. 50V/μs
- SETTLING TIME. 850ns
- POWER BANDWIDTH. 800kHz
- OFFSET VOLTAGE 0.5mV
- BIAS CURRENT 50pA

APPLICATIONS

- VIDEO AND RF AMPLIFIERS
- DATA ACQUISITION
- PULSE AMPLIFIERS
- PRECISION SIGNAL GENERATION

DESCRIPTION

HA-5110/5115 are wideband, uncompensated, operational amplifiers manufactured with FET/Bipolar technologies and dielectric isolation. These monolithic amplifiers feature superior high frequency capabilities further enhanced by precision laser trimming of the input stage to provide excellent input characteristics. These devices are stable at closed loop gains greater than 10 without external compensation.

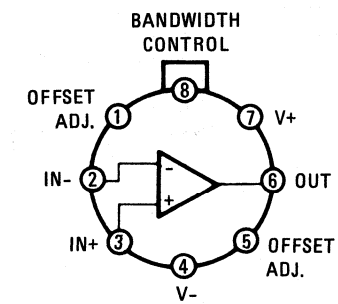
The HA-5110/5115 offer a number of important advantages over similar FET input op amps from other manufacturers. In addition to superior bandwidth and settling characteristics, the Harris devices have nearly constant slew rate, bandwidth, and settling characteristics over the operating temperature range. This provides the user predictable performance in applications where settling time, full power bandwidth, closed loop bandwidth, or phase shift is critical. The slewing waveform is symmetrical to provide reduced distortion. Note also that Harris specifies all parameters at ambient (rather than junction) temperature to provide the designer meaningful data to predict actual operating performance.

Complementing HA-5110/5115's predictable and excellent dynamic characteristics are very low input offset voltage, very low input bias current, and extremely high input impedance. This ideal combination of features make these amplifiers most suitable for precision, high speed, data acquisition system designs and for a wide variety of signal conditioning applications.*

*-2 denotes a range of -55°C to +125°C and -5 denotes a 0°C to +75°C range.

PINOUT

TOP VIEW — Package Code 2A

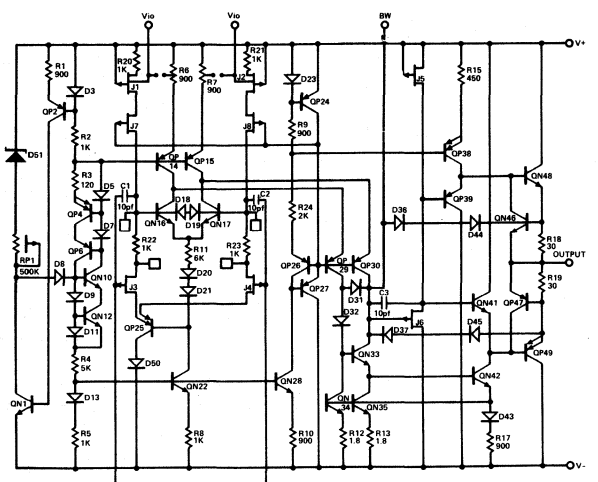


TO-99

CASE CONNECTED TO V-

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on page 1-4.

SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage Between V+ and V-	40V
Differential Input Voltage	±40V
Peak Output Current	Full Short Circuit Protection
Internal Power Dissipation (Note 2)	300mW
Storage Temperature Range	-65°C to +150°C

ELECTRICAL CHARACTERISTICS

V+ = 15VDC; V- = -15VDC
Parameters are guaranteed at indicated ambient temperature after warm-up.

		HA-5110-2 -55°C to +125°C			HA-5110-5 0°C to +75°C			HA-5115-5 0°C to +75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS											
*Offset Voltage	+25°C		0.5	1.0		0.5	1.0		0.5	1.5	mV
	Full		0.50	2.0		0.50	2.0		0.75	3.5	mV
Offset Voltage Average Drift	Full		5			10			15		µV/°C
*Bias Current	+25°C		20	50		20	50		50	100	pA
	Full		5	10			10		10	20	nA
*Offset Current	+25°C		2	10		2	10		5	50	pA
	Full		2	5		2	5		5	10	nA
Input Resistance	+25°C		$.10^{12}$			10^{12}			10^{12}		Ω
Common Mode Range	Full	±10	±11		±10	±11		±10	±10.5		V
TRANSFER CHARACTERISTICS											
*Large Signal Voltage Gain (Note 3)	+25°C	75K	150K		75K	150K		50K	100K		V/V
	Full	60K	100K		60K	100K		40K	80K		V/V
*Common Mode Rejection Ratio (Note 4)	Full	80	86		80	86		80	86		dB
Gain Bandwidth Product (A_V = 10)	Full		60			60			50		MHz
OUTPUT CHARACTERISTICS											
*Output Voltage Swing (Note 5)	+25°C	±12	±13		±12	±13		±11	±12		V
	Full	±12	±13		±12	±13		±11	±12		V
*Output Current (Note 6)	+25°C	±10	±15		±10	±15		±8	±15		mA
Full Power Bandwidth (Note 7)	+25°C	550	625		550	625		550	625		kHz
Output Resistance (Note 8)	+25°C		30			30			40		Ω
TRANSIENT RESPONSE (Note 9)											
Rise Time (A_V = 10)	+25°C		20			20			20		nsec
Slew Rate (A_V = 10)	+25°C	35	50		35	50		35	40		V/µsec
Settling Time (Note 10)	+25°C		.85			.85			1.0		µsec
POWER SUPPLY CHARACTERISTICS											
*Supply Current	Full		5	7		5	7		6	8	mA
*Power Supply Rejection Ratio (Note 11)	+25°C	80	94		80	94		80	94		dB

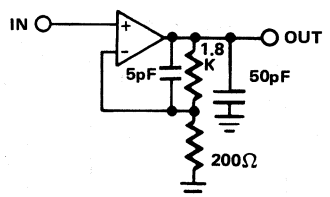
*100% tested for Dash 8. All other parameters for design information only.

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Derate at 6.8mW/°C for operation at ambient temperatures above +75°C.
3. $V_{OUT} = \pm 10V$. $R_L = 2K$
4. $V_{CM} = \pm 10$ V.D.C.
5. $R_L = 10K$
6. $V_{OUT} = 0V$
7. $R_L = 2K$; Full power bandwidth guaranteed, based on slew rate measurement using $FPBW = \frac{SLEW\ RATE.}{2\pi V_{PEAK}}$
8. Output resistance measured under open loop conditions.
9. Refer to Test Circuits section of the data sheet.
10. Settling Time is measured to 0.1% of final value for a 10 volt output step and $A_V = -10$.
11. $V_{SUPP} = \pm 10$ V.D.C. to ∓ 20 V.D.C.

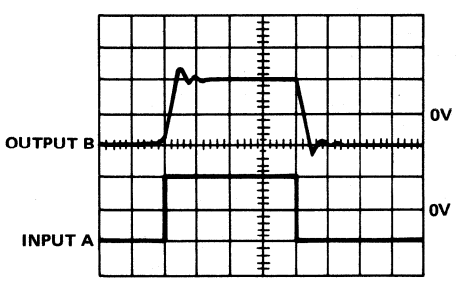
TEST CIRCUITS

LARGE AND SMALL SIGNAL RESPONSE CIRCUIT



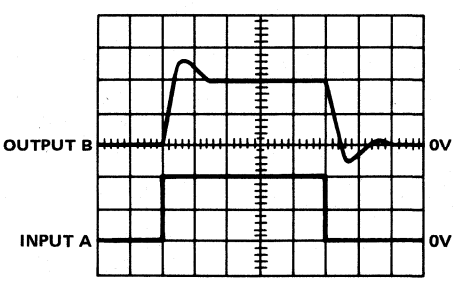
LARGE SIGNAL RESPONSE

Vertical Scale: (Volts: A=.5V/Div,B=5V/Div.)
Horizontal Scale: (Time: 500ns/Div.)

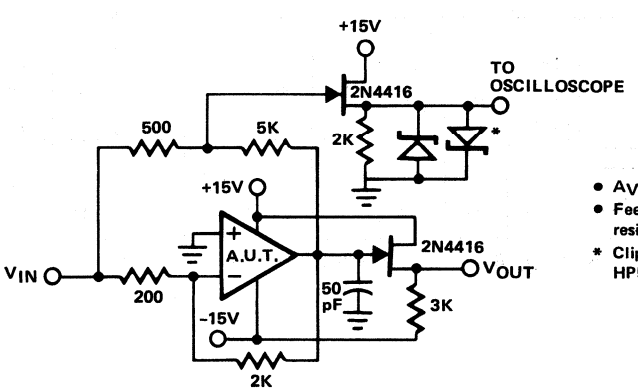


SMALL SIGNAL RESPONSE

Vertical Scale: (Volts: A=10mV/Div., B=100mV/Div.)
Horizontal Scale: (Time: 100ns/Div.)



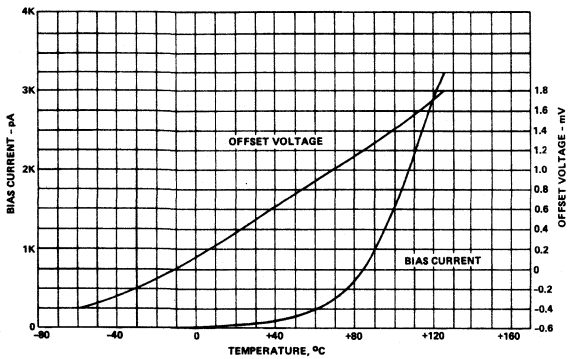
SETTLING TIME CIRCUIT



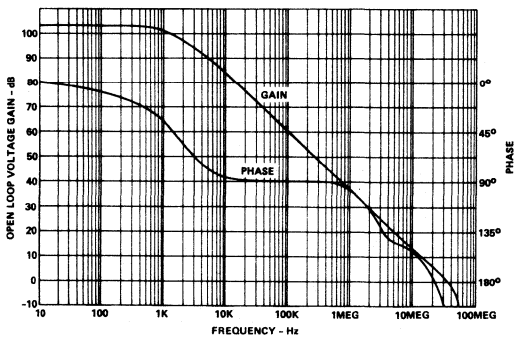
- $A_V = -10$
- Feedback and summing resistors should be 0.1%.
- * Clipping Diodes are optional. HP5082-2810 recommended.

V+ = +15V, V- = -15V, T_A = +25°C Unless Otherwise Stated.

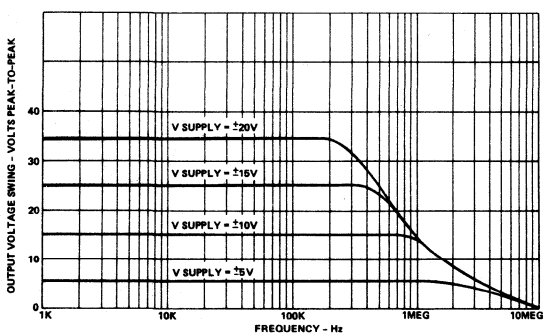
INPUT OFFSET VOLTAGE AND BIAS CURRENT VS TEMPERATURE



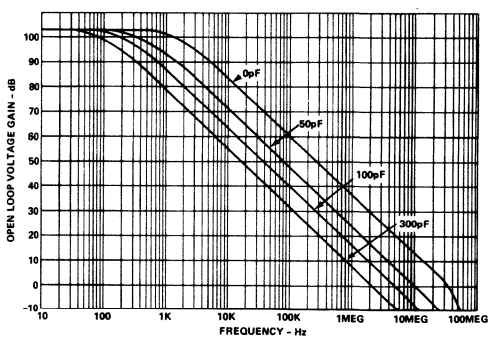
OPEN LOOP FREQUENCY RESPONSE



OUTPUT VOLTAGE SWING VS FREQUENCY

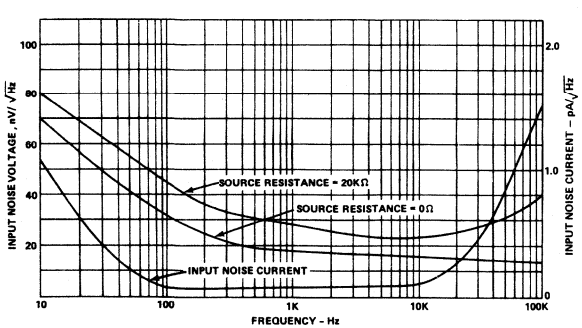


OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS BANDWIDTH CONTROL CAPACITANCES

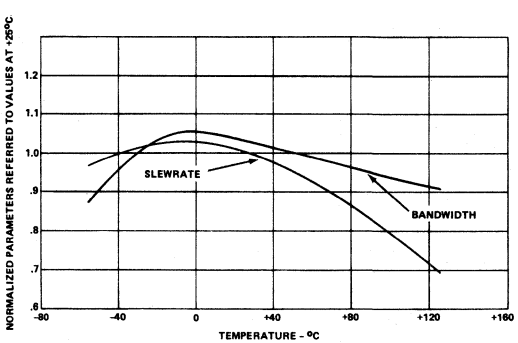


NOTE: External compensation components are not required for closed loop gains > 10, but may be added to reduce bandwidth if desired.

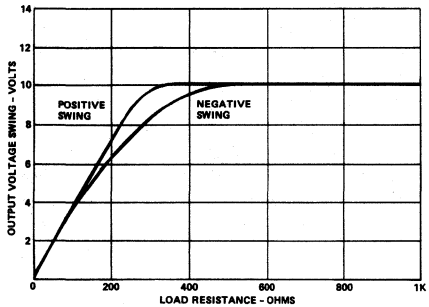
INPUT NOISE VOLTAGE AND NOISE CURRENT VS FREQUENCY



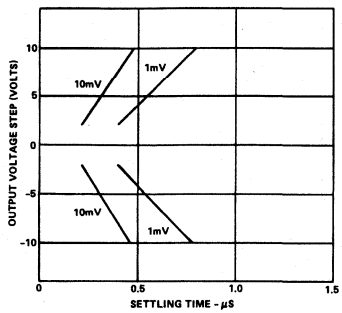
NORMALIZED AC PARAMETERS VS TEMPERATURE



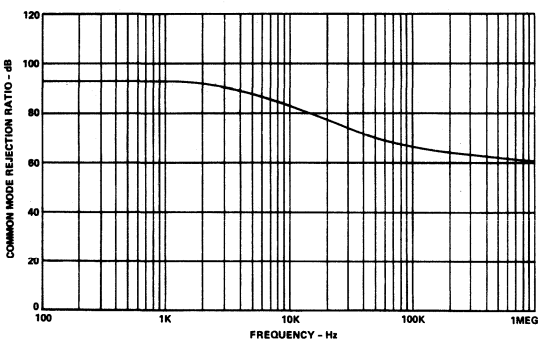
OUTPUT VOLTAGE SWING VS LOAD RESISTANCE



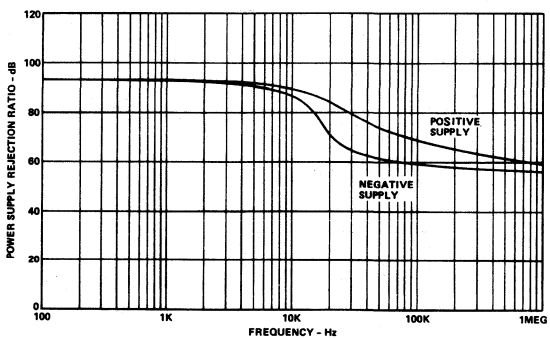
SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES



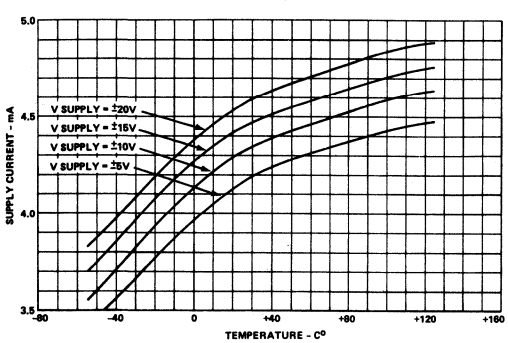
COMMON MODE REJECTION RATIO VS FREQUENCY



POWER SUPPLY REJECTION RATIO VS FREQUENCY



POWER SUPPLY CURRENT VS TEMPERATURE



APPLYING THE HA-5110/5115

1. POWER SUPPLY DECOUPLING: Although not absolutely necessary, it is recommended that all power supply lines be decoupled with .01 μF ceramic capacitors to ground. Decoupling capacitors should be located as near to the amplifier terminals as possible.

2. STABILITY CONSIDERATIONS: In applications where large value feedback resistors are used, a small compacitor ($\approx$ 3pF) may be needed in parallel with the feedback resistor to neutralize the pole introduced by the input capacitance.

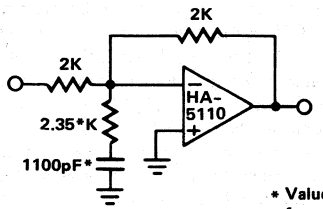
3. HEAVY CAPACITIVE LOADS: When driving heavy capacitive loads ($\geq$100pF) a small resistor ($\approx$100Ω) should be connected in series with the output and inside the feedback loop.

4. OFFSET VOLTAGE NULLING: Offset nulling, if required, is accomplished with a 100KΩ pot between pins 1 and 5; wiper to V+. Alteration of initial offset voltage may affect the temperature coefficient of the offset voltage.

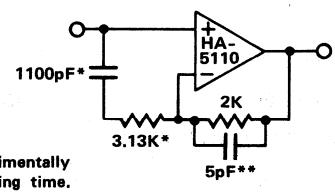
APPLICATIONS

SUGGESTED COMPENSATION FOR UNITY GAIN STABILITY

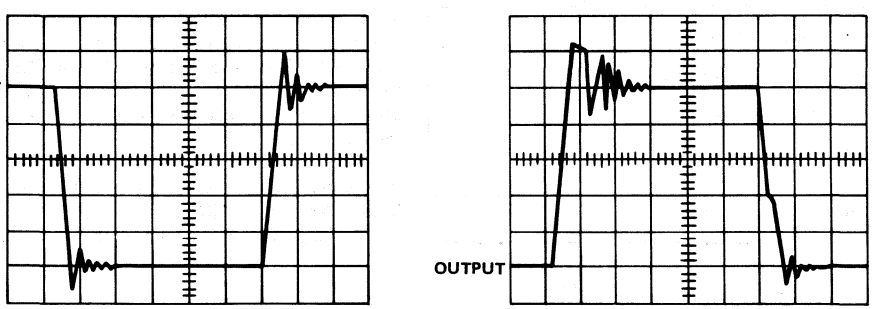
INVERTING



NON-INVERTING

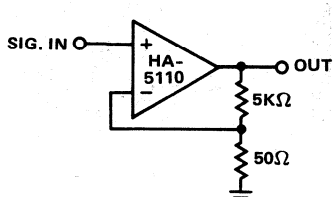


* Values were determined experimentally for optimum speed and settling time.
** Optional

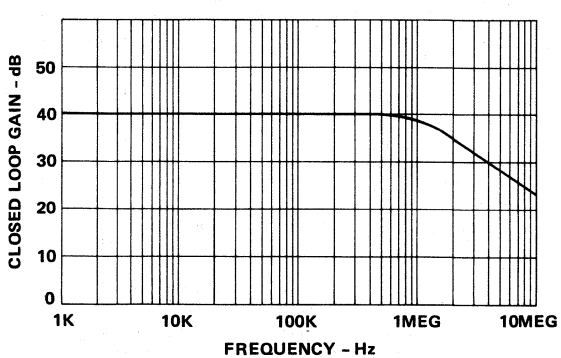


Vertical Scale: (Volts: 2V/Div.)
Horizonal Scale: (Time: 500ns/Div.)

40dB, 1MHz BANDWIDTH AMPLIFIER



CLOSED LOOP FREQUENCY RESPONSE (A_V = 100)



HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HA-5190/5195

Wideband, Fast Settling Operational Amplifiers

JANUARY 1979

2

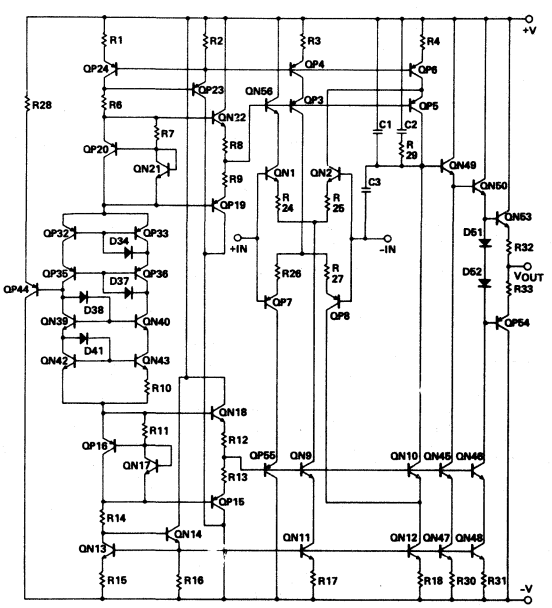
FEATURES

- FAST SETTLING TIME — 70ns
- VERY HIGH SLEW RATE — 200V/μs
- WIDE GAIN-BANDWIDTH — 150MHz
- POWER BANDWIDTH — 6.5MHz
- LOW OFFSET VOLTAGE — 5mV
- INPUT VOLTAGE NOISE — 15nV/$\sqrt{Hz}$
- MONOLITHIC BIPOLAR CONSTRUCTION

APPLICATIONS

- FAST, PRECISE D/A CONVERTERS
- HIGH SPEED SAMPLE-HOLD CIRCUITS
- PULSE AND VIDEO AMPLIFIERS
- WIDEBAND AMPLIFIERS

SCHEMATIC



GENERAL DESCRIPTION

HA-5190/5195 are monolithic operational amplifiers featuring an ultimate combination of speed, precision, and bandwidth. Employing monolithic bipolar construction coupled with dielectric isolation, these devices are capable of delivering an unparalleled 200V/μs slew rate with a settling time of 70ns (0.1%, 5V output step.) These truly differential amplifiers are designed to operate at gains ≥ 5 without the need for external compensation. Other outstanding HA-5190/5195 features are 150MHz gain-bandwidth-product and 6.5MHz full power bandwidth. In addition to these dynamic characteristics, these amplifiers also have excellent input characteristics such as 5mV offset voltage and 15nV input voltage noise (at 1kHz).

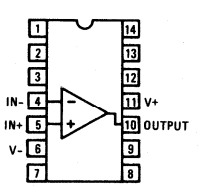
With 200V/μs slew rate and 70ns settling time, these devices make ideal output amplifiers for accurate, high speed D/A converters or the main components in high speed sample/hold circuits. 150MHz gain-bandwidth-product, 6.5MHz power bandwidth, and 5mV offset voltage make HA-5190/5195 ideally suited for a variety of pulse and wideband video amplifier applications.

At temperatures above +75°C, a heat sink is required for HA-5190. (See note 2.) HA-5190 is specified over the -55°C to +125°C range while HA-5195 is specified from 0°C to +75°C.

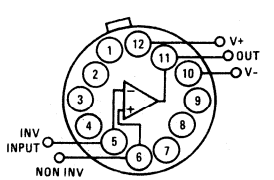
PINOUTS

Package Code 6G, 4D

TOP VIEW



TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on page 1-4.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage between V+ and V- Terminals	35V
Differential Input Voltage	6V
Output Current	50mA (Peak)
Internal Power Dissipation (Note 2)	870mW (Cerdip); 1W (TO-8) Free Air
Operating Temperature Range: (HA-5190)	$-55^{o}C \leq T_A \leq +125^{o}C$
(HA-5195)	$0^{o}C \leq T_A \leq +75^{o}C$
Storage Temperature Range	$-65^{o}C \leq T_A \leq +150^{o}C$

ELECTRICAL CHARACTERISTICS $V_{SUPPLY} = \pm 15$ Volts; $R_L = 200$ ohms, unless otherwise specified.

		HA-5190 -55°C to +125°C			HA-5195 0°C to +75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		3.0	5.0		3.0	6	mV
	FULL			10.0			10.0	mV
Average Offset Voltage Drift	FULL		20			20		µV/°C
Bias Current	+25°C		5	15		5	15	µA
	FULL			20			20	µA
Offset Current	+25°C		1	4		1	4	µA
	FULL			6			6	µA
Input Resistance	+25°C		10			10		Kohms
Input Capacitance	+25°C		1.0			1.0		pF
Common Mode Range	FULL	±5			±5			V
Input Noise Voltage (f = 1kHz, $R_g = 0\Omega$)	+25°C		15			15		$nV/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 3)	+25°C	15K	30K		10K	30K		V/V
	FULL	5K			5K			V/V
Common-Mode Rejection Ratio (Note 4)	FULL	74	100		74	100		dB
Gain-Bandwidth-Product (Notes 5 & 6)	+25°C		150			150		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 3)	FULL	±5	±8		±5	±8		V
Output Current (Note 3)	+25°C	25	30		25	30		mA
Output Resistance	+25°C		TBD			TBD		Ohms
Full Power Bandwidth (Note 3 & 7)	+25°C	5	6.5		5	6.5		MHz
TRANSIENT RESPONSE (Note 8)								
Rise Time	+25°C		13	18		13	18	ns
Overshoot	+25°C		8			8		%
Slew Rate	+25°C	160	200		160	200		V/µs
Settling Time:								
5V Step to 0.1%	+25°C		70			70		ns
5V Step to 0.01%	+25°C		100			100		ns
2.5V Step to 0.1%	+25°C		50			50		ns
2.5V Step to 0.01%	+25°C		80			80		ns
POWER REQUIREMENTS								
Supply Current	FULL		19	28		19	28	mA
Power Supply Rejection Ratio (Note 9)	FULL	70	90		70	90		dB

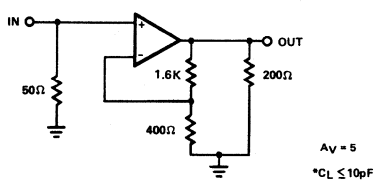
* 100% tested for DASH 8. All other parameters for design information only.

NOTES

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Derate at 8.7mW/°C for operation at ambient temperatures above +75°c. Heat sinking required at temperatures above +75°c. T_{JA} = 115°C/W; T_{JC} = 35°C/W. Thermalloy model 6007 heat sink recommended.
3. $R_L = 200\Omega$, $C_L < 10pF$, $V0 = \pm 5V$.
4. $V_{CM} = \pm 5V$.
5. $V_O = 90mV$.
6. $A_V = 10$.
7. Full power bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{\text{Slew Rate}}{2\pi V_{peak}}$.
8. Refer to Test Circuits section of data sheet.
9. $V_{SUPPLY} = \pm 10$ V.D.C. to ± 15 V.D.C.

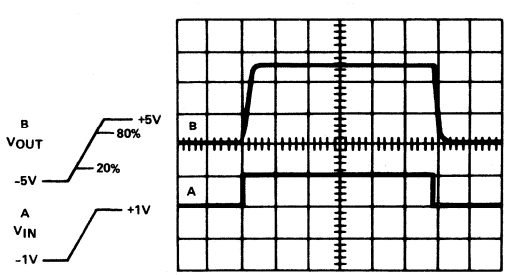
TEST CIRCUITS

LARGE AND SMALL SIGNAL RESPONSE TEST CIRCUIT*



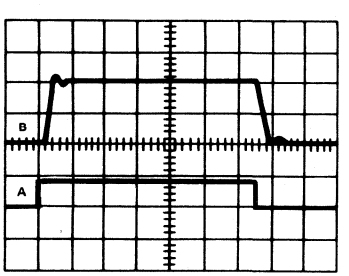
LARGE SIGNAL RESPONSE

Vertical Scale: (Volts: A = 0.5V/Div., B = 4.0V/Div.)
Horizontal Scale: (Time: 100ns/Div.)

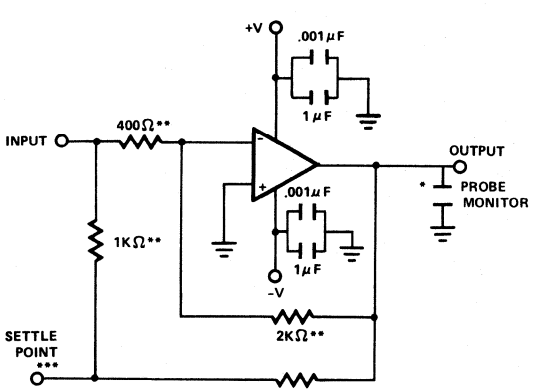


SMALL SIGNAL RESPONSE

Vertical Scale: (Volts: A=50mV/Div., B=100mV/Div.)
Horizontal Scale: (Time: 100ns/Div.)



SETTLING TIME TEST CIRCUIT



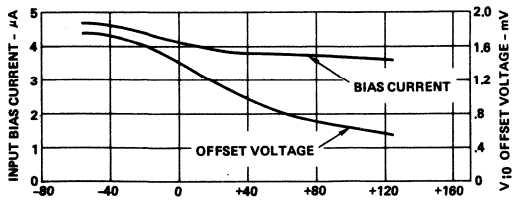
* Load Capacitance should be less than 10pF.

** It is recommended that resistors be carbon composition and that feedback and summing network ratios be matched.

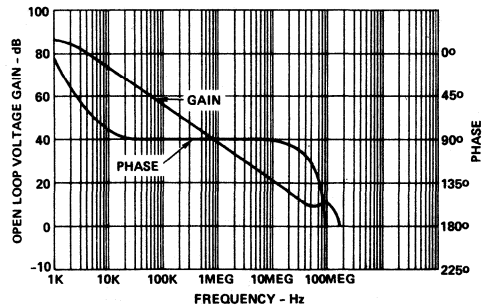
*** SETTLE POINT (Summing Node) capacitance should be less than 10pF. For optimum settling time results, it is recommended that the test circuit be constructed directly onto the device pins. A Tektronix 568 Sampling Oscilloscope with S-3A sampling heads is recommended as a settle point monitor.

V+ = +15V, V- = -15V, T_A = +25°C unless otherwise stated.

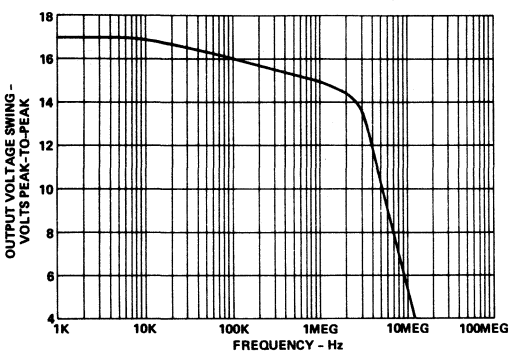
INPUT OFFSET VOLTAGE AND BIAS CURRENT VS. TEMPERATURE



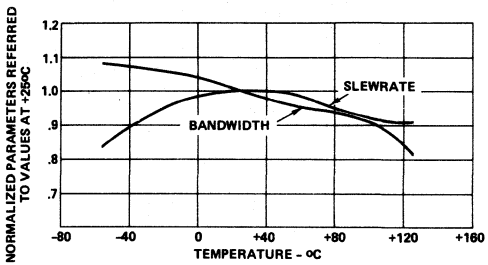
OPEN LOOP FREQUENCY RESPONSE



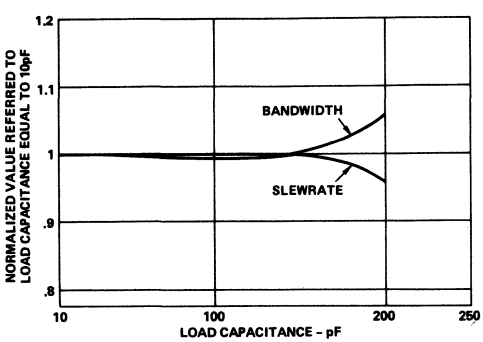
OUTPUT VOLTAGE SWING VS. FREQUENCY



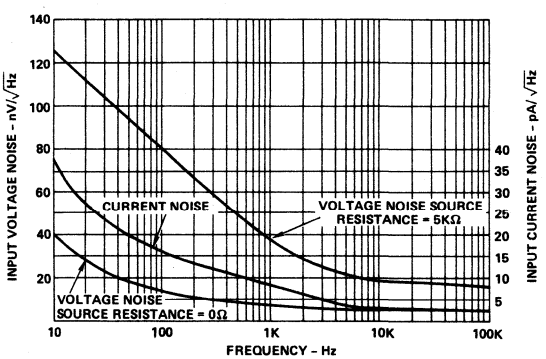
NORMALIZED AC PARAMETERS VS. TEMPERATURE



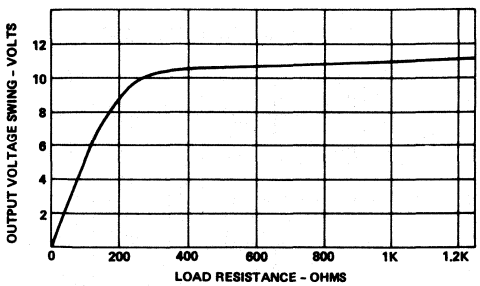
NORMALIZED AC PARAMETERS VS. LOAD CAPACITANCE



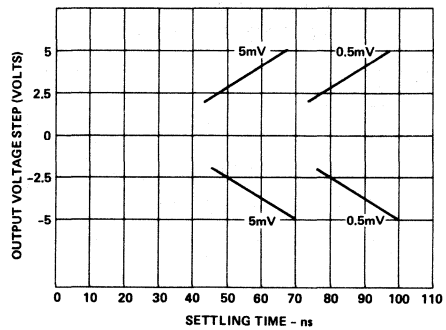
INPUT NOISE VOLTAGE AND NOISE CURRENT VS. FREQUENCY



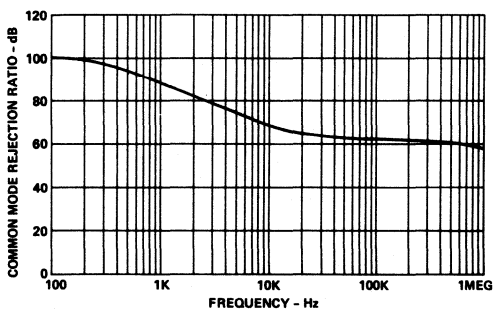
OUTPUT VOLTAGE SWING VS. LOAD RESISTANCE



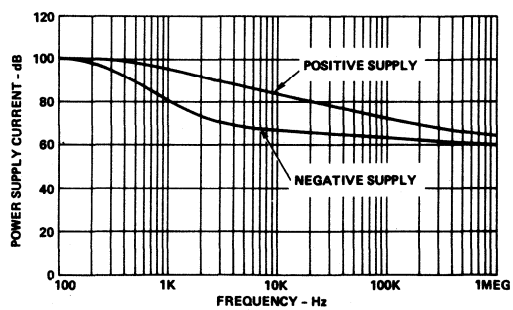
SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES



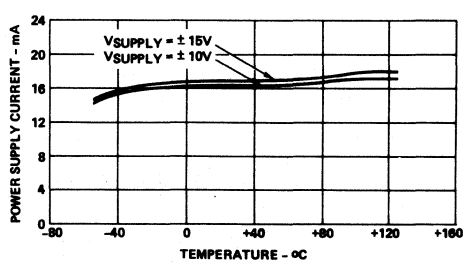
COMMON MODE REJECTION RATIO VS. FREQUENCY



POWER SUPPLY REJECTION RATIO VS. FREQUENCY



POWER SUPPLY CURRENT VS. TEMPERATURE



APPLYING THE HA-5190/5195

1. POWER SUPPLY DECOUPLING: Although not absolutely necessary, it is recommended that all power supply lines be decoupled with .01μF ceramic capacitors to ground. Decoupling capacitors should be located as near to the amplifier terminals as possible.

2. STABILITY CONSIDERATIONS: HA-5190/5195 is stable at gains ≥ 5. Gains < 5 are covered elsewhere in this data sheet. Feedback resistors should be of carbon composition located as near to the input terminals as possible.

3. WIRING CONSIDERATIONS: Video pulse circuits should be built on a ground plane. Minimum point to point connections directly to the amplifier terminals should be used. When ground planes cannot be used, good single point grounding techniques should be applied.

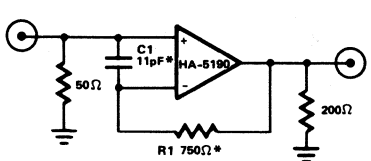
4. OUTPUT SHORT CIRCUIT: HA-5190/5195 does not have output short circuit protection. Short circuits to ground can be tolerated for approximately 10 seconds. Short circuits to either supply will result in immediate destruction of the device. In applications where short circuiting is possible, current limiting resistors in the supply lines are recommended.

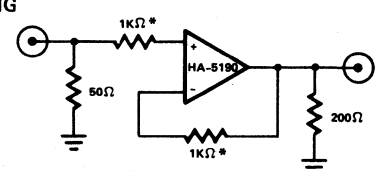
5. HEAVY CAPACITIVE LOADS: When driving heavy capacitive loads ($\geq$100pF) a small resistor ($\approx$100Ω) should be connected in series with the output and inside the feedback loop.

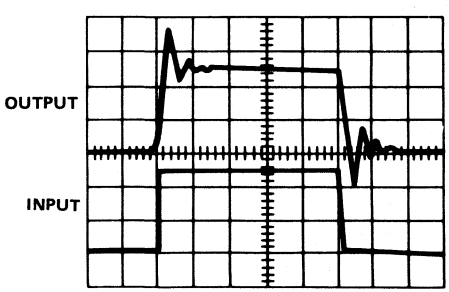
APPLICATIONS

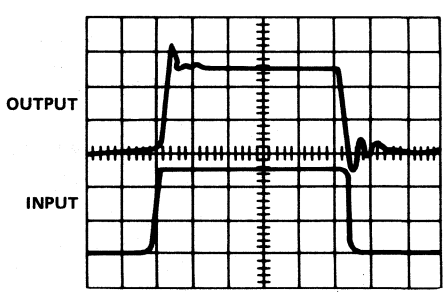
SUGGESTED COMPENSATION FOR UNITY GAIN STABILITY

NON-INVERTING







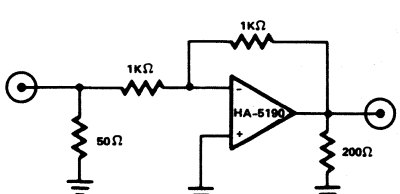


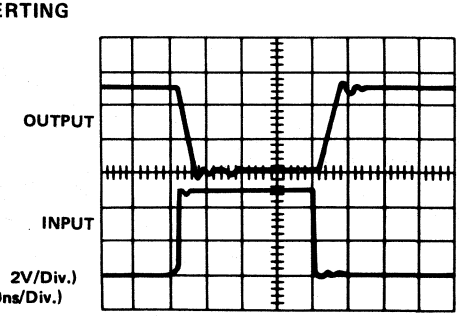
Vertical Scale: (Volts: 2V/Div.)
Horizontal Scale: (Time: 100ns/Div.)

* Values were determined experimentally for optimum speed and settling time.

R1 and C1 should be optimized for each particular application to ensure best overall frequency response.

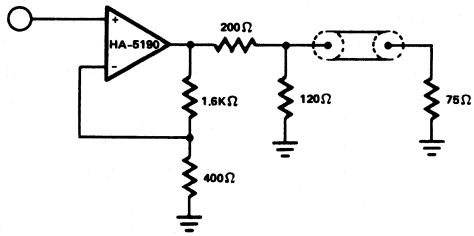
INVERTING



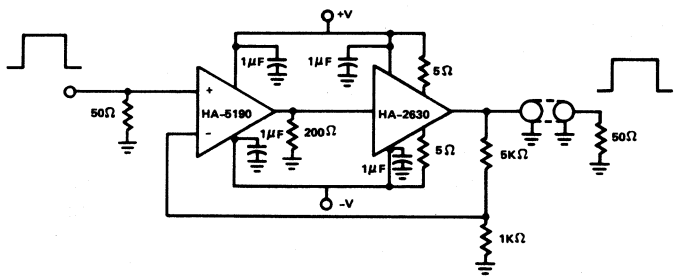


Vertical Scale: (Volts: 2V/Div.)
Horizontal Scale: (50ns/Div.)

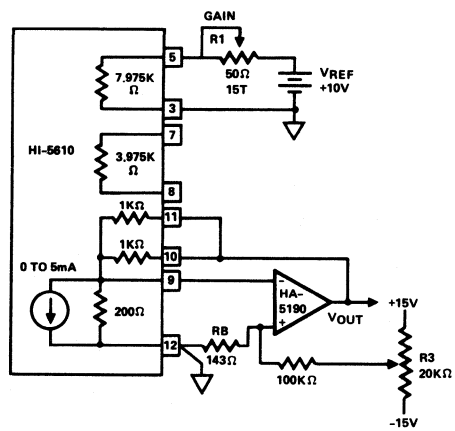
VIDEO PULSE AMPLIFIER/75Ω COAXIAL DRIVER

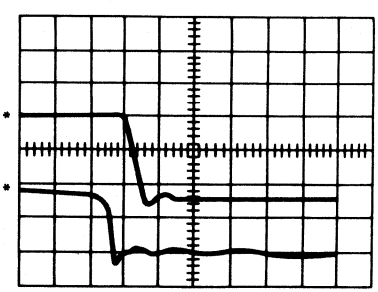


VIDEO PULSE AMPLIFIER COAXIAL LINE DRIVER



FAST DAC OUTPUT BUFFER





Vertical Scale: (Volts: 2V/Div.)
Horizontal Scale: (Time: 50ns/Div.)

$B = V_{OUT}$ C = DIGITAL INPUT

* Time delay between B and C represents total time delay for 0V to +5V full scale coded change.

CMOS Analog Switches and Multiplexers

3

ABSOLUTE MAXIMUM RATINGS

As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Characteristics" are the only conditions recommended for satisfactory operation.

CMOS Switches Selection Guide

FUNCTION	DEVICE	$R_{ON}(\Omega)$ (TYP)	$I_{D(OFF)}$(NA) (TYP)	$t_{(ON)}$(NS) (TYP)	$t_{(OFF)}$(NS) (TYP)	P_D(mW) (TYP)	PAGE
SPST	HI-5040	50	0.5	370	280	1.5	20
2 x SPST	HI-200	55	1	240	180	15	4
	HI-5048	25	0.5	370	280	1.5	20
	HI-5041	50	0.5	370	280	1.5	20
4 x SPST	HI-201	65	2	180	155	15	10
SPDT	HI-5050	25	0.5	370	280	1.5	20
	HI-5042	50	0.5	370	280	1.5	20
2 x SPDT	HI-5051	25	0.5	370	280	1.5	20
	HI-5043	50	0.5	370	280	1.5	20
DPST	HI-5044	50	0.5	370	280	1.5	20
2 x DPST	HI-5049	25	0.5	370	280	1.5	20
	HI-5045	50	0.5	370	280	1.5	20
2 x DPST (3 ADDRESS)	HI-1800A	125	0.02	500	300	10	16
DPDT	HI-5046A	25	0.5	370	280	1.5	20
	HI-5046	50	0.5	370	280	1.5	20
4PST	HI-5047A	25	0.5	370	280	1.5	20
	HI-5047	50	0.5	370	280	1.5	20

NOTE: All data typical room temperature specifications at $\pm$15V supplies. For guaranteed and tested specifications consult the device data sheet.

CMOS Multiplexers Selection Guide

FUNCTION	DEVICE	FEATURE	TTL "HIGH" MIN(V)	$R_{ON}(\Omega)$ (TYP)	$I_{D(OFF)}$ (nA) (TYP)	$t_{(ON)}$ (ns) (TYP)	$t_{(OFF)}$ (ns) (TYP)	P_D(mW) (TYP)	PAGE
4-CHANNEL DIFFERENTIAL	HI-1828A	LOW R_{ON} LOW LEAKAGE	4.0	250	0.05	350	250	5	52
	HI-509A	ANALOG INPUT OVERVOLTAGE PROTECTION	4.0	1200	1.0	300	300	7.5	40
8-CHANNEL	HI-1818A	LOW R_{ON} LOW LEAKAGE	4.0	250	0.1	350	250	5	52
	HI-508A	ANALOG OVERVOLTAGE PROTECTION	4.0	1200	1.0	300	300	7.5	40
8-CHANNEL DIFFERENTIAL	HI-507	LOW R_{ON}	2.4	170	1.0	300	300	30	28
	HI-507A	ANALOG OVERVOLTAGE PROTECTION	4.0	1200	1.0	300	300	7.5	34
16-CHANNEL	HI-506	LOW R_{ON}	2.4	170	1.0	300	300	30	28
	HI-506A	ANALOG OVERVOLTAGE PROTECTION	4.0	1200	1.0	300	300	7.5	34
	HI-1840	HIGH-Z OVERVOLTAGE PROTECTION	4.0	2000	1.0	300	300	0.6	56
8-CHANNEL/ 4 DIFFERENTIAL	HI-518	HIGH SPEED LOW LEAKAGE	2.4	620	0.035	100	80	525	49
16-CHANNEL/ 8 DIFFERENTIAL	HI-516	HIGH SPEED LOW LEAKAGE	2.4	480	0.1	80	60	360	46

NOTE: All data typical room temperature specifications at $\pm$ 15V supplies. For guaranteed and tested specifications consult the device data sheet.

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HI-200

Dual SPST CMOS Analog Switch

3

FEATURES

- ANALOG VOLTAGE RANGE ±15V
- ANALOG CURRENT RANGE 80mA
- TURN-ON TIME 240ns
- LOW R_{ON} 55Ω
- LOW POWER DISSIPATION 15mW
- TTL/CMOS COMPATIBLE
- NO DIGITAL INPUT CURRENT SPIKE

APPLICATIONS

- HIGH FREQUENCY ANALOG SWITCHING
- SAMPLE AND HOLD CIRCUITS
- DIGITAL FILTERS
- OP AMP GAIN SWITCHING NETWORKS

DESCRIPTION

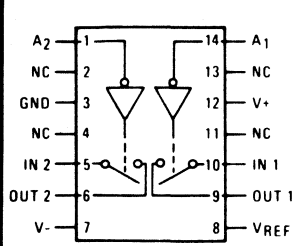
HI-200 is a monolithic device comprising two independently selectable SPST switches which feature fast switching speeds (290ns) combined with low power dissipation (15mW at 25°C). Each switch provides low "ON" resistance operation for input signal voltages up to the supply rails and for signal currents up to 80mA. Employing Dielectric Isolation and Complementary CMOS processing, HI-200 operates without any applications problems induced by latch-up or SCR mode phenomena.

All devices provide break-before-make switching and are TTL and CMOS compatible for maximum application versatility. HI-200 is an ideal component for use in high frequency analog switching. Typical applications include signal path switching, sample and hold circuit, digital filters and op amp gain switching networks.

HI-200 is available in DIP and metal (TO-100) cans. HI-200-2 is specified from -55°C to +125°C while HI-200-5 operates from 0°C to +75°C. HI-200 is functionally and pin compatible with other available "200 series" switches.

PINOUT

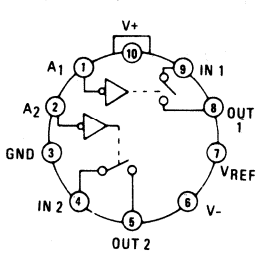
Package Code 4U
3M



TO-116

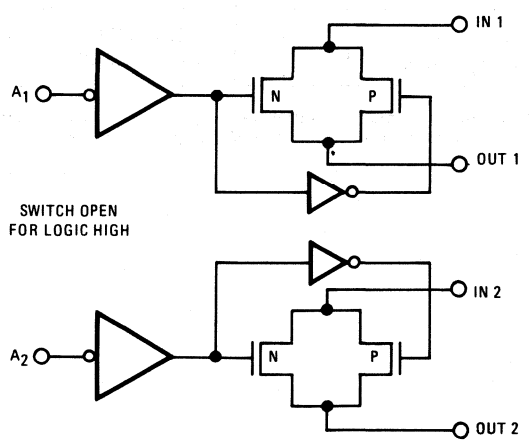
Package Code 2D, 4U, 3M, LA

Top View



TO-100

FUNCTIONAL DIAGRAM



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Between Pins 6 and 10	+40V	Total Power Dissipation*	450mW
V_{REF} to Ground	+20V, -5V	Operating Temperature	
Digital Input Voltage:	$+V_{Supply}$ +4V	HI-200-2	-55°C to +125°C
	$-V_{Supply}$ -4V	HI-200-4	-20°C to +85°C
Analog Input Voltage (One Switch)	$+V_{Supply}$ +2.0V	HI-200-5	0°C to +75°C
	$-V_{Supply}$ -2.0V	Storage Temperature	-65°C to +150°C

*Derate 6mW/°C Above T_A = 75°C

ELECTRICAL CHARACTERISTICS

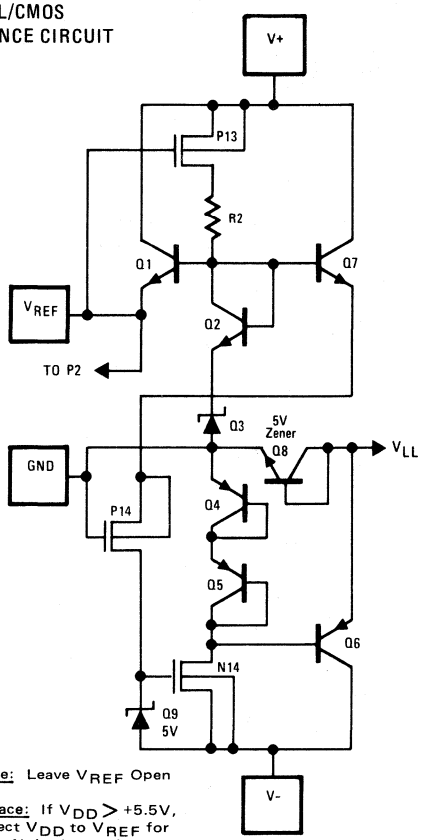
Unless Otherwise Specified
Supplies = +15V, -15V; V_{REF} = Open; V_{AH}(Logic Level High) = 3.0V V_{AL}(Logic Level Low) = +0.8V
For Test Conditions, consult Performance Characteristics

		HI-200-2 -55°C to +125°C			HI-200-5 ** 0°C to +75°C			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
ANALOG SWITCH CHARACTERISTICS								
* V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
* R_{ON}, On Resistance (Note 1)	+25°C		55	70		55	80	Ω
	Full		80	100		72	100	Ω
* $I_{S(OFF)}$, Off Input Leakage Current	+25°C		1			1		nA
(Note 6)	Full		100	500		10	500	nA
* $I_{D(OFF)}$, Off Output Leakage Current	+25°C		1			1		nA
(Note 6)	Full		100	500		10	500	nA
* $I_{D(ON)}$, On Leakage Current (Note 6)	+25°C		.02			.02		nA
	Full		6	500		6	500	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold	Full			0.8			0.8	V
V_{AH}, Input High Threshold	Full	3.0			3.0			V
* I_A, Input Leakage Current (High or Low) (Note 2)	Full			1.0			1.0	μA
SWITCHING CHARACTERISTICS								
t_{OPEN}, Break - Before Make Delay (Note 3)	+25°C		60			60		ns
t_{on}, Switch on Time	+25°C		240	500		240		ns
t_{off}, Switch off Time	+25°C		330	500		500		ns
"Off Isolation" (Note 4)	+25°C		70			70		dB
$C_{S(OFF)}$, Input Switch Capacitance	+25°C		5.5			5.5		pF
$C_{D(OFF)}$, Output Switch Capacitance	+25°C		5.5			5.5		pF
$C_{D(ON)}$, Output Switch Capacitance	+25°C		11			11		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
$C_{DS(OFF)}$, Drain-To-Source Capacitance	+25°C		0.5			0.5		pF
POWER REQUIREMENTS (Note 5)	+25°C		15			15		mW
P_D, Power Dissipation	Full			60			60	mW
* I^+, Current (Pin 10)	+25°C		0.5			0.5		mA
	Full			2.0			2.0	mA
* I^-, Current (Pin 6)	+25°C		0.5			0.5		mA
	Full			2.0			2.0	mA

NOTES:
1. V_{OUT} = ±10V I_{OUT} = 1mA
2. Digital Inputs Are MOS Gates - Typical Leakage is Less Than 1nA
3. V_{AH} = 4.0V
4. V_A = +3V, R_L = 1KΩ, C_L = 10pF, V_S = 3VRMS, f, 100 kHz
5. V_A = +3V or V_A = OV For Both Switches
6. Refer to leakage current measurement diagram on page (3-8)

* 100% Tested for Dash 8 at +25°C and +125°C Only.
** Note: HI-200-4 has same specifications as HI-200-5 over the temperature range -20°C to +85°C.

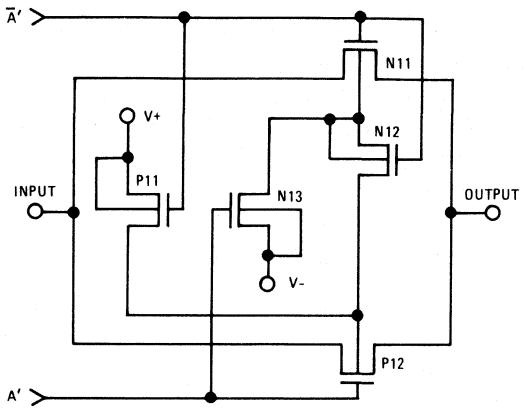
TTL/CMOS
REFERENCE CIRCUIT



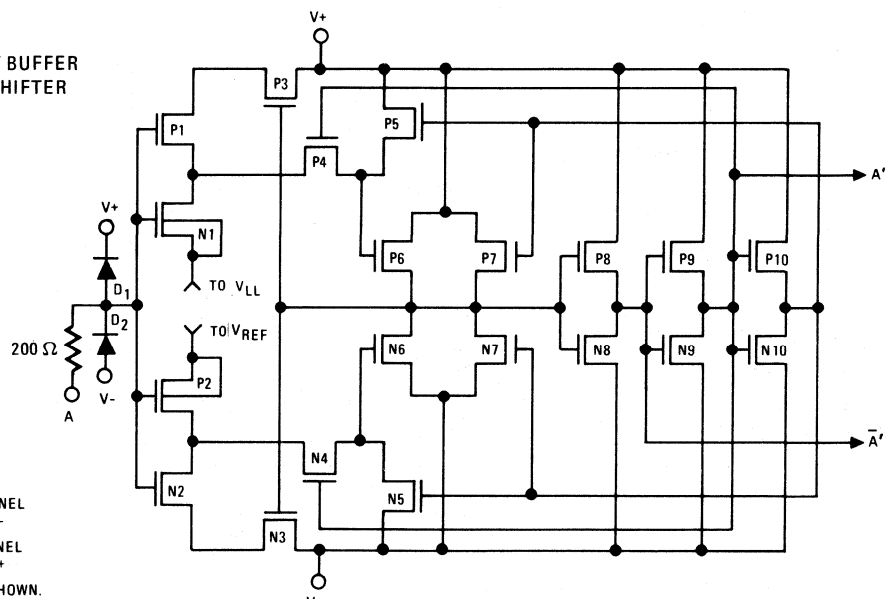
*TTL Interface: Leave V_{REF} Open

*CMOS Interface: If $V_{DD} > +5.5V$, Connect V_{DD} to V_{REF} for Higher Noise Immunity; Otherwise Leave Open.

SWITCH CELL



DIGITAL INPUT BUFFER
AND LEVEL SHIFTER



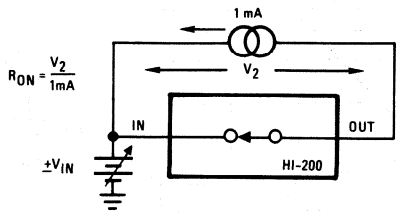
ALL N-CHANNEL BODIES TO V-

ALL P-CHANNEL BODIES TO V+

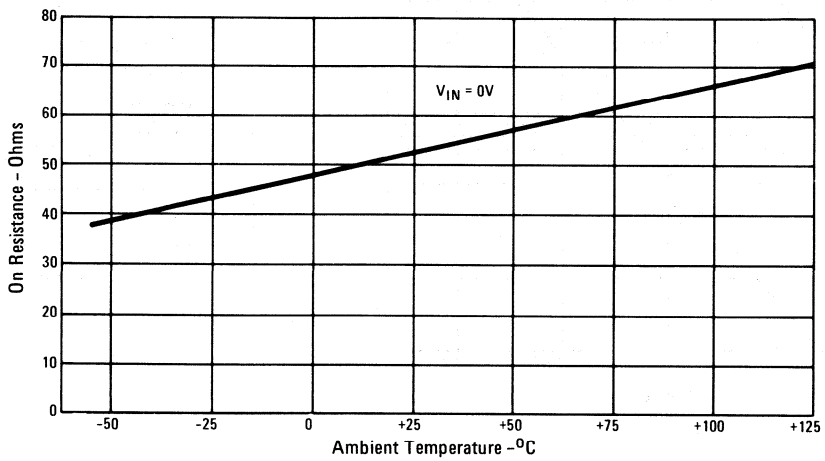
EXCEPT AS SHOWN.

(UNLESS OTHERWISE SPECIFIED $T_A = 25^oC$, $V_{SUPPLY} = \pm 15V$, $V_{AH} = 3.0V$ $V_{AL} = 0.8V$ AND V_{REF} = OPEN).

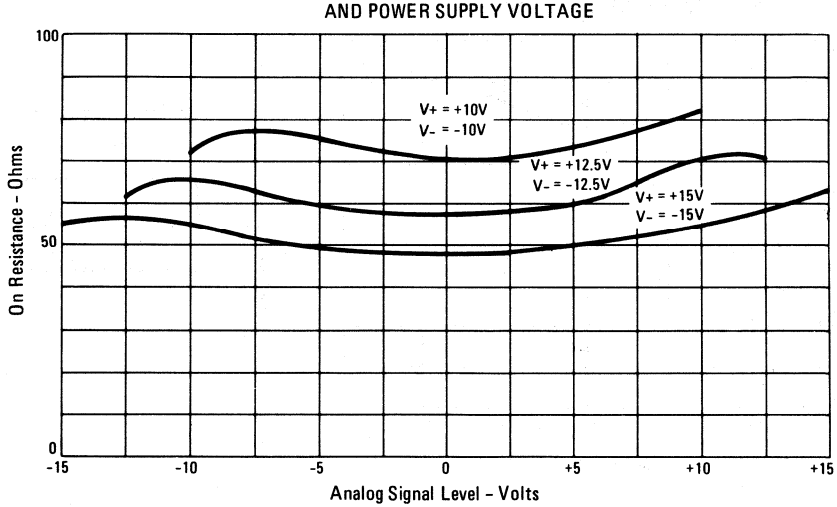
ON RESISTANCE vs. ANALOG SIGNAL LEVEL,
SUPPLY VOLTAGE AND TEMPERATURE



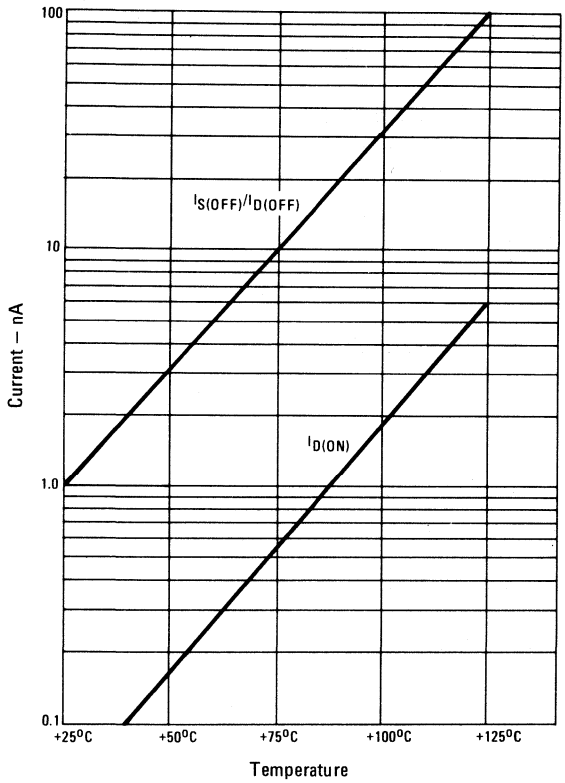
ON RESISTANCE vs. TEMPERATURE



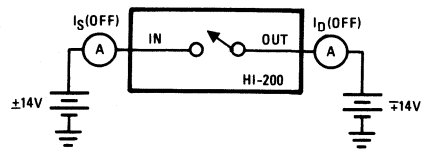
(HI-200)
ON RESISTANCE vs. ANALOG SIGNAL LEVEL
AND POWER SUPPLY VOLTAGE



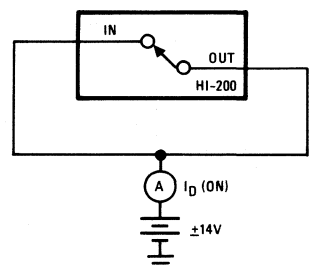
SWITCH LEAKAGE CURRENT vs. TEMPERATURE (HI-200)



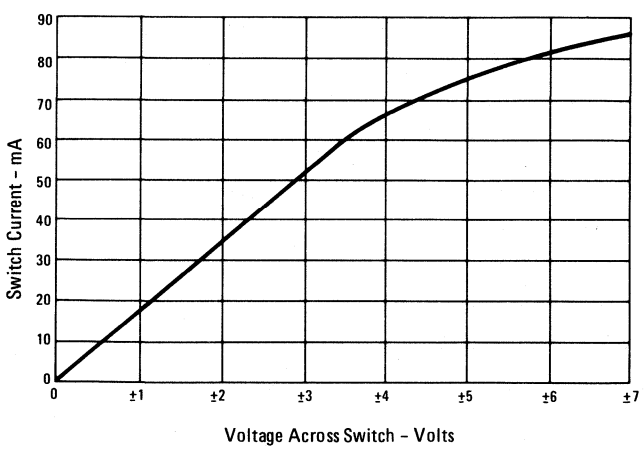
OFF LEAKAGE CURRENT vs. TEMPERATURE



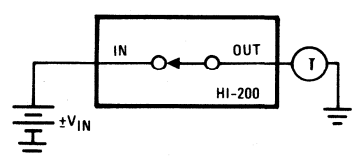
ON LEAKAGE CURRENT vs. TEMPERATURE



SWITCH CURRENT vs. VOLTAGE

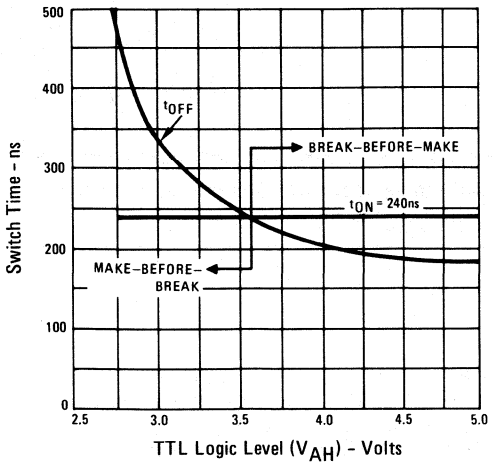


SWITCH CURRENT vs. VOLTAGE

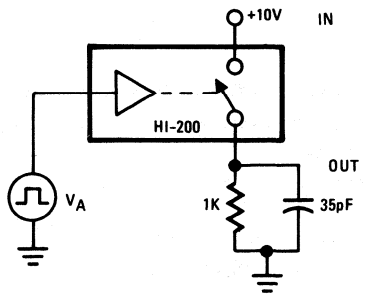


PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS (continued)

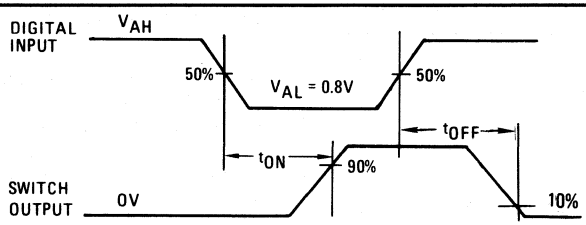
(HI-200)
SWITCH TIME vs. TTL LOGIC LEVEL



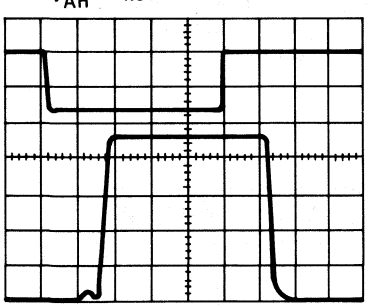
ON/OFF SWITCH TIME vs.
LOGIC LEVEL



SWITCHING WAVEFORMS

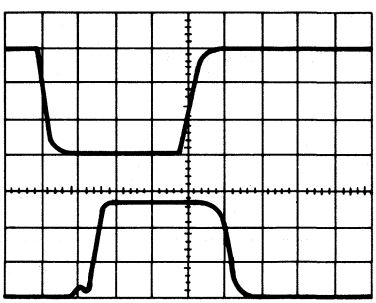


t_{ON}, t_{OFF} (TTL INPUT)
V_{AH} = +4.0V



Top: TTL Input
Bottom: Output
Vertical: 2V/Div.
Horizontal: 200ns/Div.

t_{ON}, t_{OFF}(CMOS INPUT)
V_{REF} = OPEN, V_{AH} = +15V



Top: CMOS Input
Bottom: Output
Vertical: 5V/Div.
Horizontal: 200ns/Div.

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HI-201

Quad SPST CMOS Analog Switch

3

FEATURES

- ANALOG VOLTAGE RANGE ±15V
- ANALOG CURRENT RANGE 80mA
- TURN-ON TIME 185ns
- LOW R_{ON} 65Ω
- LOW POWER DISSIPATION 15mW
- TTL/CMOS COMPATIBLE
- NO DIGITAL INPUT CURRENT SPIKE

APPLICATIONS

- HIGH FREQUENCY ANALOG SWITCHING
- SAMPLE AND HOLD CIRCUITS
- DIGITAL FILTERS
- OP AMP GAIN SWITCHING NETWORKS

DESCRIPTION

HI-201 is a monolithic device comprising four independently selectable SPST switches which feature fast switching speeds (185ns) combined with low power dissipation (15mW at 25°C). Each switch provides low "ON" resistance operation for input signal voltages up to the supply rails and for signal currents up to 80mA. Employing Dielectric Isolation and Complementary CMOS processing, HI-201 operates without any applications problems induced by latch-up or SCR-mode phenomena.

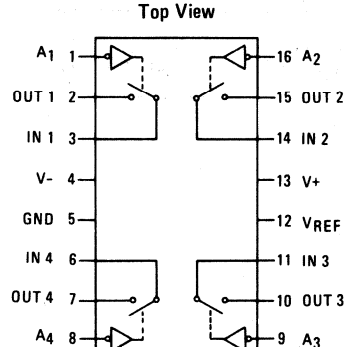
All devices provide break-before-make switching and are TTL and CMOS compatible for maximum application versatility. HI-201 is an ideal component for use in high frequency analog switching. Typical appliations include signal path switching, sample and hold circuit, digital filters and op amp gain switching networks.

HI-201 is available in a 16 lead dual-in-line package. HI-201-2 is specified from -55°C to +125°C while HI-201-5 operates from 0°C to +75°C. HI-201 is functionally and pin compatible with other available "200 series" switches.

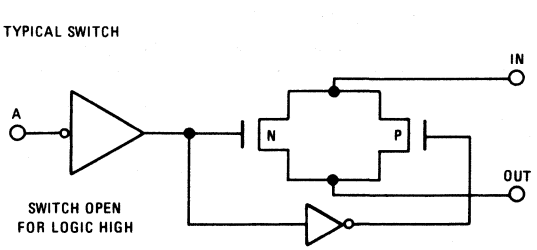
PIN OUT

Package Code 4B, 3C, LA

Top View



FUNCTIONAL DIAGRAM



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Between Pins 4 and 13	+40V	Total Power Dissipation*	750mW
V_{REF} to Ground	+20V, -5V	Operating Temperature	
Digital Input Voltage:	V_{Supply}(+) +4V	HI-201-2	-55°C to +125°C
	V_{Supply}(-) -4V	HI-201-4	-20°C to +85°C
Analog Input Voltage (One Switch)	$+V_{Supply}$ +2.0V	HI-201-5	0°C to +75°C
	$-V_{Supply}$ -2.0V	Storage Temperature	-65°C to +150°C

*Derate 8mW/°C Above T_A = +75°C

ELECTRICAL CHARACTERISTICS

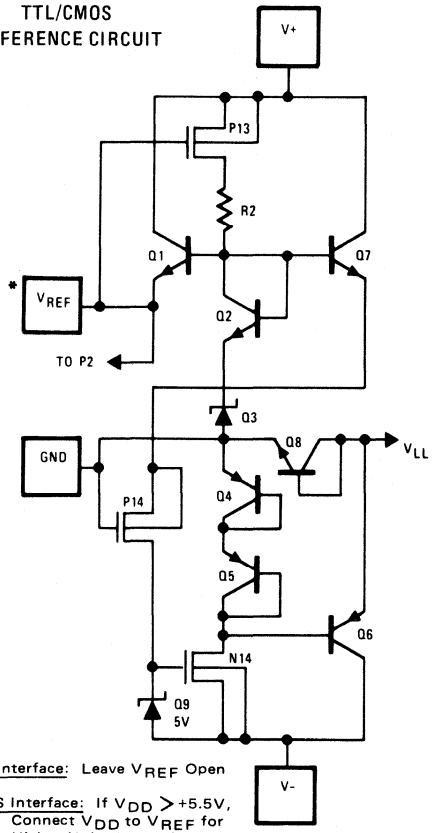
Unless Otherwise Specified
Supplies = +15V, -15V; V_{REF} = Open; V_{AH} (Logic Level High) = 3.0V V_{AL} (Logic Level Low) = +0.8V
For Test Conditions, consult Performance Characteristics

		HI-201-2 -55°C to +125°C			HI-201-5 ** 0°C to +75°C			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
ANALOG SWITCH CHARACTERISTICS								
*V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
*R_{ON}, On Resistance (Note 1)	+25°C		65	80		65	100	Ω
	Full		85	125		75	125	Ω
*$I_{S(OFF)}$, Off Input Leakage Current	+25°C		2			2		nA
(Note 6)	Full			500			250	nA
*$I_{D(OFF)}$, Off Output Leakage Current	+25°C		2			2		nA
(Note 6)	Full			500			250	nA
*$I_{D(ON)}$, On Leakage Current (Note 6)	+25°C		2			2		nA
	Full			500			250	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold	Full			0.8			0.8	V
V_{AH}, Input High Threshold	Full	3.0			3.0			V
*I_A, Input Leakage Current (High or Low) (Note 2)	Full			1.0			1.0	μA
SWITCHING CHARACTERISTICS								
t_{OPEN}, Break - Before Make Delay (Note 3)	+25°C		30			30		ns
t_{on}, Switch ON Time	+25°C		185	500		185		ns
t_{off}, Switch OFF Time	+25°C		220	500		220		ns
"Off Isolation" (Note 4)	+25°C		80			80		dB
$C_{S(OFF)}$, Input Switch Capacitance	+25°C		5.5			5.5		pF
$C_{D(OFF)}$, Output Switch Capacitance	+25°C		5.5			5.5		pF
$C_{D(ON)}$, Output Switch Capacitance	+25°C		11			11		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
$C_{DS(OFF)}$, Drain-To-Source Capacitance	+25°C		0.5			0.5		pF
POWER REQUIREMENTS (Note 5)	+25°C		15			15		mW
P_D, Power Dissipation	Full			60			60	mW
*I+, Current (Pin 13)	+25°C		0.5			0.5		mA
	Full			2.0			2.0	mA
*I- Current (Pin 4)	+25°C		0.5			0.5		mA
	Full			2.0			2.0	mA

NOTES:
1. V_{OUT} = ±10V I_{OUT} = 1mA
2. Digital Inputs Are MOS Gates - Typical Leakage is Less Than 1nA
3. V_{AH} = 4.0V
4. V_A = 5V, R_L = 1KΩ, C_L = 10pF, V_S = 3VRMS, f = 100KHz
5. V_A = +3V or V_A = 0V For all Switches
6. Refer to leakage current measurement diagram on page (3-14)

* 100% Tested for Dash 8 at +25°C and +125°C Only.
** Note: HI-201-4 has same specifications as HI-201-5 over the temperature range -20°C to +85°C.

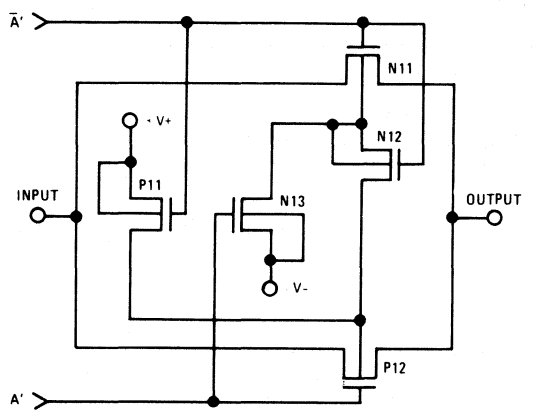
TTL/CMOS
REFERENCE CIRCUIT



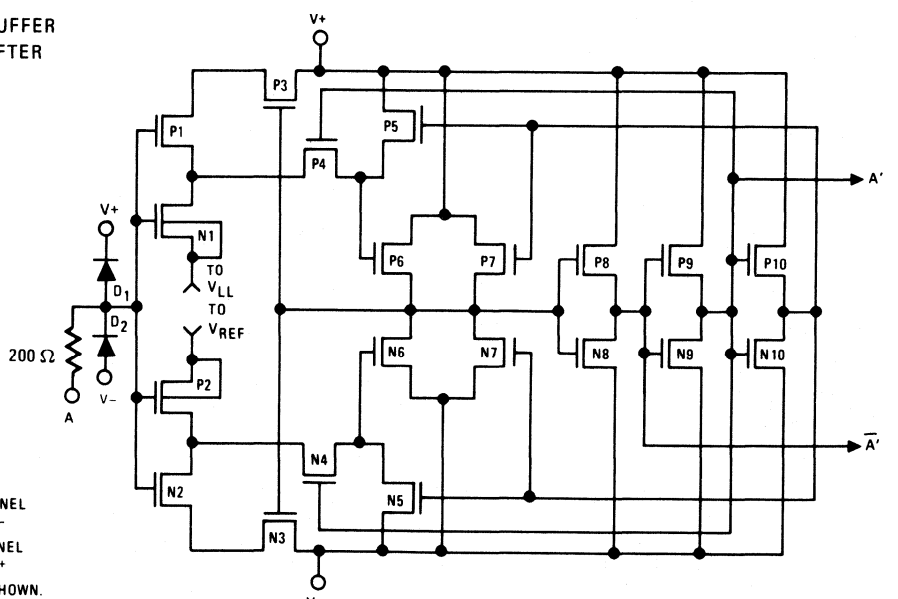
*TTL Interface: Leave V_{REF} Open

*CMOS Interface: If $V_{DD} > +5.5V$, Connect V_{DD} to V_{REF} for Higher Noise Immunity; Otherwise Leave Open.

SWITCH CELL



DIGITAL INPUT BUFFER
AND LEVEL SHIFTER



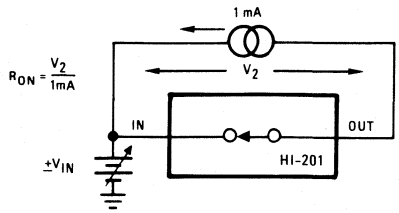
ALL N-CHANNEL
BODIES TO V-

ALL P-CHANNEL
BODIES TO V+

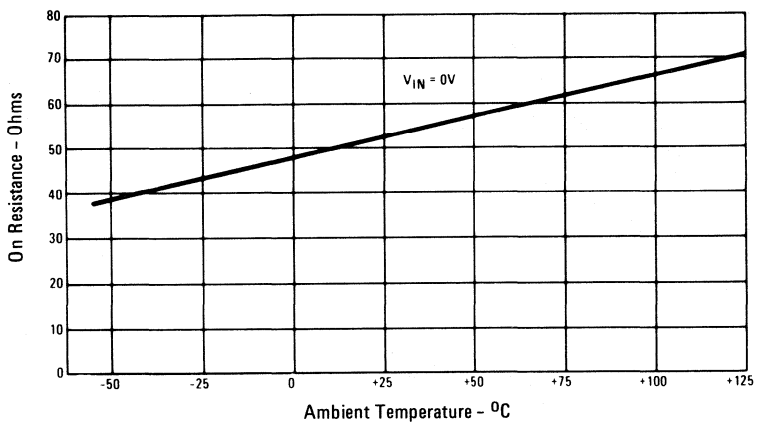
EXCEPT AS SHOWN.

(UNLESS OTHERWISE SPECIFIED $T_A = 25^oC$, $V_{SUPPLY} = \pm 15V$, $V_{AH} = 3.0V$ $V_{AL} = 0.8V$ AND V_{REF} = OPEN).

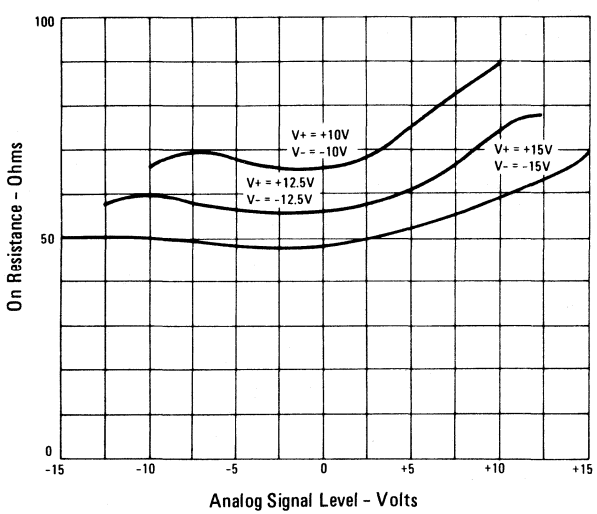
ON RESISTANCE vs. ANALOG SIGNAL LEVEL,
SUPPLY VOLTAGE AND TEMPERATURE



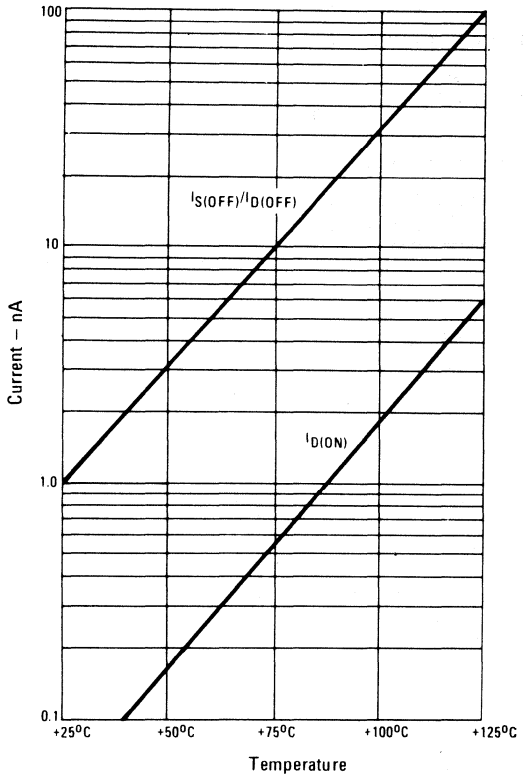
ON RESISTANCE vs. TEMPERATURE



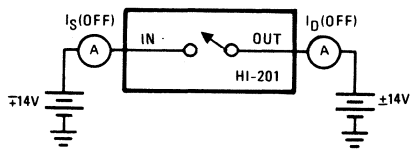
(HI-201)
ON RESISTANCE vs. ANALOG SIGNAL LEVEL
AND POWER SUPPLY VOLTAGE



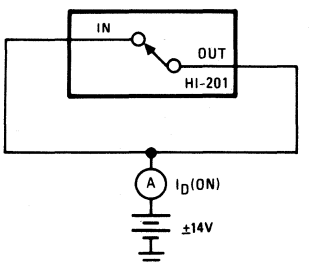
SWITCH LEAKAGE CURRENT vs. TEMPERATURE (HI-201)



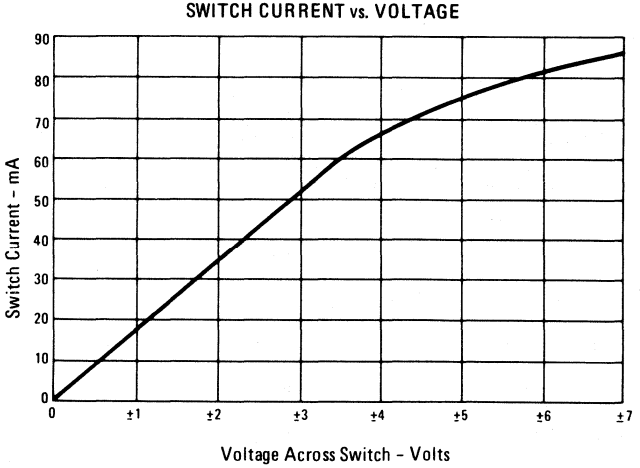
OFF LEAKAGE CURRENT vs. TEMPERATURE



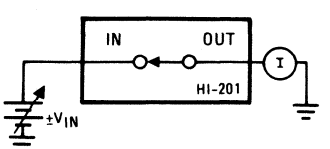
ON LEAKAGE CURRENT vs. TEMPERATURE



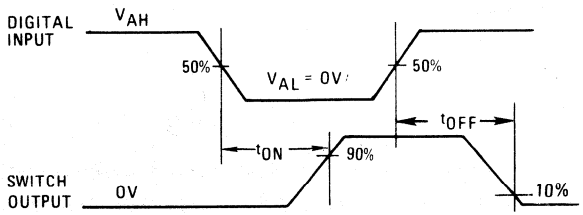
SWITCH CURRENT vs. VOLTAGE



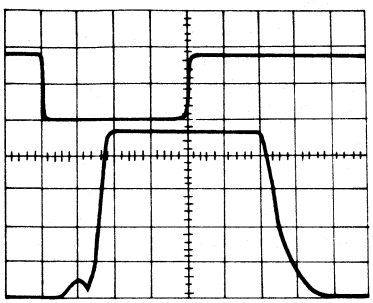
SWITCH CURRENT vs. VOLTAGE



SWITCHING WAVEFORMS



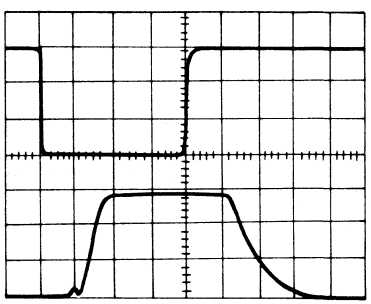
t_{ON}, t_{OFF}(TTL INPUT)
V_{IN} = 3.5V



Top: TTL Input
Bottom: Output

Horizontal: 100ns/Div.
Vertical: 2V/Div.

t_{ON}, t_{OFF}(CMOS INPUT)
V_{REF} = OPEN, V_{IN} = +15V



Top: CMOS Input
Bottom: Output

Vertical: 5V/Div.
Horizontal: 100ns/Div.

HARRIS
SEMICONDUCTOR
PROGRAMS DIVISION
A DIVISION OF HARRIS CORPORATION

HI-1800A

Low Leakage Dual DPST Analog Switch

3

FEATURES

- LEAKAGE (TYP.) 40nA
- SIGNAL RANGE ±15V
- "ON" RESISTANCE (TYP.) 125Ω
- ACCESS TIME (TYP.) 500ns
- DTL/TTL COMPATIBLE ADDRESS

APPLICATIONS

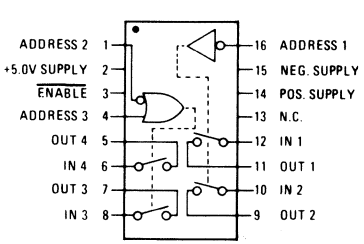
- SIGNAL SELECTOR
- CHOPPER
- SAMPLE AND HOLD
- GAIN SWITCHING

DESCRIPTION

The HI-1800A is a general purpose analog switch which may be used as a signal selector, multiplexer, chopper, or cross-point switch for signals from D.C. to R.F. The configuration is two independent DPST switches with versatile TTL compatibile addressing logic which allows connection as two SPDT, or as a single DPDT, SPDT, or SPST switch by connection of external jumpers. ON resistance decreases correspondingly when switching elements are connected in parallel. The HI-1800A is fabricated on a single dielectrically isolated chip using complementary N and P channel MOS devices. This unique process produces exceptionally low leakage currents, constant ON resistance, low power dissipation, and fast switching. The HI-1800A is available in a hermetic 16 pin dual-in-line package.

PINOUT

Package Code 4B, LA



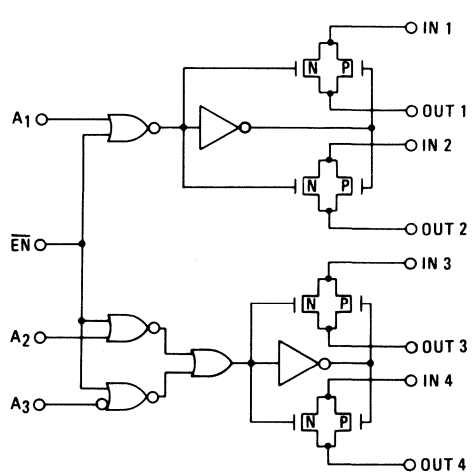
TRUTH TABLE

INPUT ADDRESS				SWITCH CHANNELS			
A1	A2	A3	$\overline{EN}$	1	2	3	4
L	X	X	L	ON	ON		
H	X	X	L	OFF	OFF		
X	L	X	L			ON	ON
X	X	H	L			ON	ON
X	H	L	L			OFF	OFF
X	X	X	H	OFF	OFF	OFF	OFF

H ≥ +4.0V L ≤ +0.4V

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage Between Pins 14 and 15	40.0V	Digital Input Voltage	V^-Supply, V^+Supply
Logic Supply Voltage, Pin 2	30.0V	Total Power Dissipation	780 mW (Note 2)
Analog Input Voltage: V^+Supply +2V	V^-Supply -2V	Storage Temperature Range	-65^oC to $+150^oC$

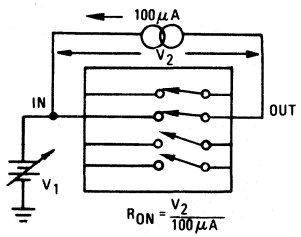
ELECTRICAL CHARACTERISTICS

Supplies = +15V, -15V, +5.0V

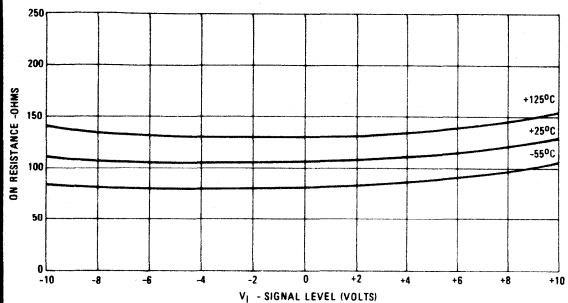
PARAMETER	TEMP.	HI-1800A-5 0°C to +75°C MIN.	TYP.	MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS					
V_{IN}, Analog Signal Range	Full	-15		+15	V
R_{ON}, ON Resistance (Note 3)	+25°C		125	200	Ω
	Full			250	Ω
I_S (OFF), Input Leakage Current	Full		40	100	nA
I_D (OFF), Output Leakage Current	Full		40	100	nA
I_D (ON), On Channel Leakage Current	Full		40	100	nA
DIGITAL INPUT CHARACTERISTICS					
V_{IL}, Input Low Threshold	Full			0.4	V
V_{IH}, Input High Threshold (Note 4)	Full	4.0			V
I_{IN}, Input Leakage Current	Full		.01	1	μA
SWITCHING CHARACTERISTICS					
t_A, Access Time (Note 5)	+25°C		500		ns
Break-Before-Make Delay	+25°C		200		ns
C_{IN}, Channel Input Capacitance	+25°C		8		pF
C_{OUT}, Channel Output Capacitance	+25°C		8		pF
C_D, Digital Input Capacitance	+25°C		5		pF
POWER REQUIREMENTS					
P_D, Power Dissipation	Full		10		mW
P_{DS}, Standby Power (Note 6)	Full		10		mW
I_+, Current Pin 14	Full		0.001	1	mA
I_-, Current Pin 15	Full		0.5	2	mA
I_L, Current Pin 2	Full		0.5	2	mA

NOTES:
1. Voltage ratings apply when voltages at all other pins are within their nominal operating ranges.
2. Derate 9.25 mW/°C above t_A = +75°C
3. $V_{OUT} = \pm 10V$ $I_{OUT} = -100\mu A$.
4. To drive from DTL/TTL circuits, 1K pullup resistors to +5.0V supply are recommended.
5. Time measured to 90% of final output level; V_{OUT} = -5.0V to +5.0V, Digital Inputs = 0.4V to +4.0V.
6. Voltage at Pin 3, $\overline{\text{ENABLE}} \geq +4.0V$.

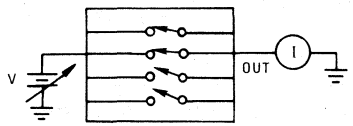
ON RESISTANCE vs ANALOG SIGNAL LEVEL



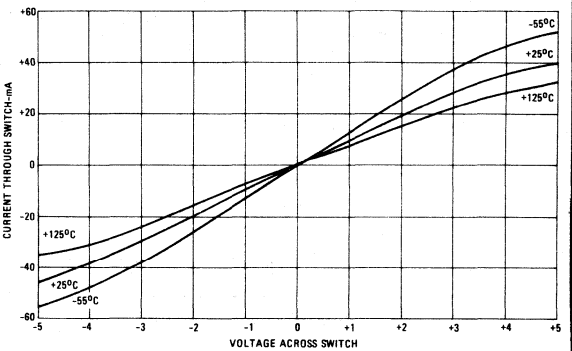
Test Circuit



ON CHANNEL CURRENT vs VOLTAGE

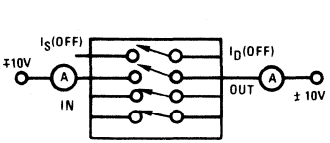


Test Circuit

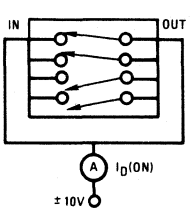


ON/OFF LEAKAGE CURRENTS vs TEMPERATURE

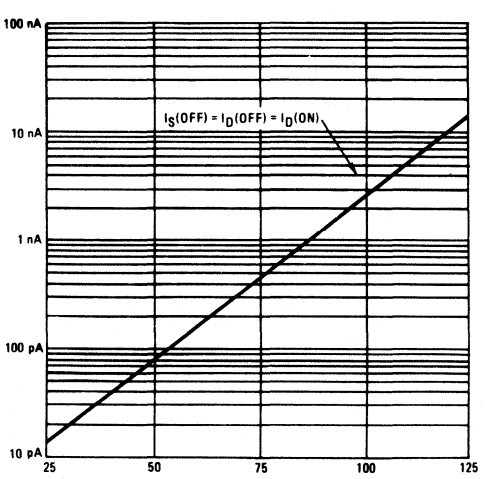
OFF LEAKAGE



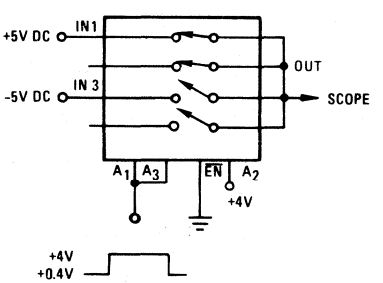
ON LEAKAGE

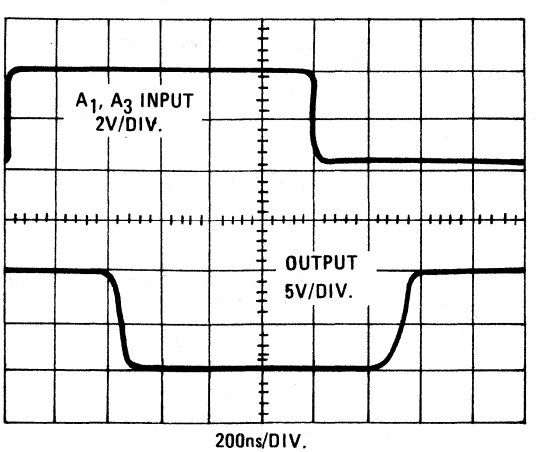


Test Circuit



ACCESS TIME

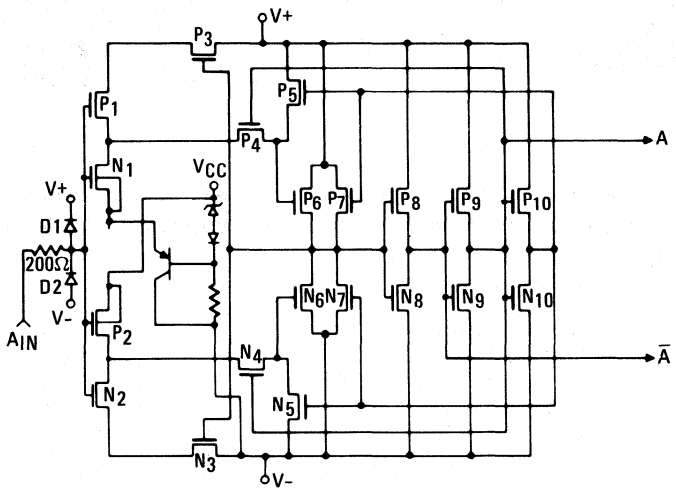




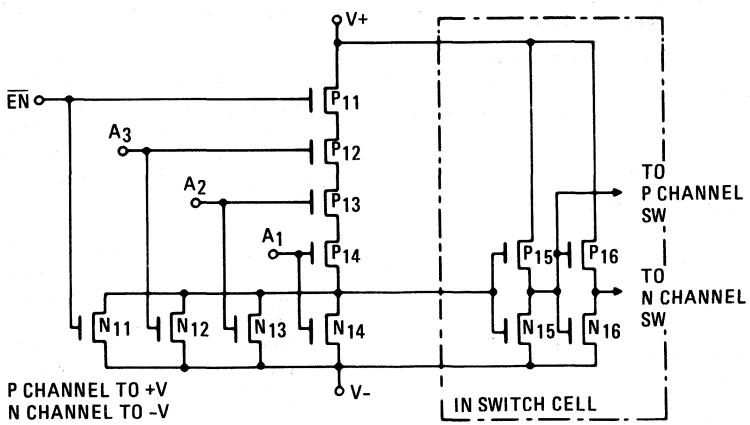
SCHEMATIC DIAGRAM

ADDRESS INPUT BUFFER

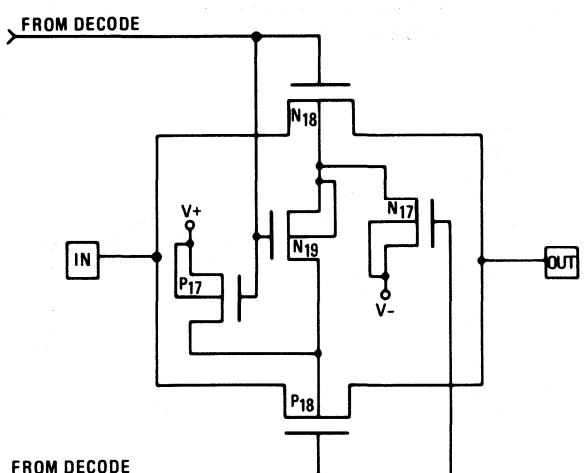
ALL N-CHANNEL BODIES TO V-
ALL P-CHANNEL BODIES TO V+
UNLESS OTHERWISE INDICATED



DECODER GATE



MULTIPLEX SWITCH



HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HI-5040 thru HI-5051
HI-5046A and HI-5047A

CMOS Analog Switches

3

FEATURES

- WIDE ANALOG SIGNAL RANGE ±15V
- LOW "ON" RESISTANCE (TYP) 25Ω
- HIGH CURRENT CAPABILITY (TYP) 80mA
- BREAK-BEFORE-MAKE SWITCHING
  - TURN-ON TIME (TYP) 370ns
  - TURN-OFF TIME (TYP) 280ns
- NO LATCH-UP
- INPUT MOS GATES ARE PROTECTED FROM ELECTROSTATIS DISCHARGE
- DTL, TTL, CMOS, PMOS COMPATIBLE

APPLICATIONS

- HIGH FREQUENCY SWITCHING
- SAMPLE AND HOLD
- DIGITAL FILTERS
- OP AMP GAIN SWITCHING

DESCRIPTION

This family of CMOS analog switches offers low-resistance switching performance for analog voltages up to the supply rails and for signal currents up to 80mA. "ON" resistance is low and stays reasonably constant over the full range of operating signal voltage and current. R_{ON} remains exceptionally constant for input voltages between +5V and -5V and currents up to 50mA. Switch impedance also changes very little over temperature, particularly between 0°C and +75°C. R_{ON} is nominally 25 ohms for HI-5048 through HI-5051 and HI-5046A/5047A and 50Ω for HI-5040 through HI-5047.

All devices provide break-before-make switching and are TTL and CMOS compatible for maximum application versatility. Performance is further enhanced by Dielectric Isolation processing which insures latch-free operation with very low input and output leakage currents (0.8nA at 25°C). This family of switches also features very low power operation (1.5mW at 25°C).

There are 14 devices in this switch series which are differentiated by type of switch action and value of R_{ON} (see Functional diagram). All devices are available in 16 pin D.I.P. packages. The HI-5040/5050 switches can directly replace IH-5040 series devices and are functionally compatible with the DG 180/190 family. Each switch type is available in the -55°C to +125°C and 0°C to +75°C performance grades.

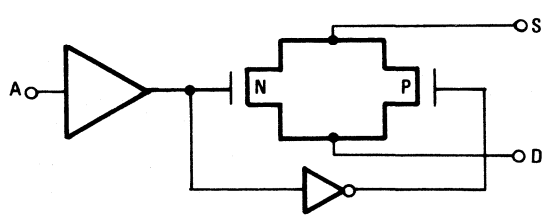
FUNCTIONAL DESCRIPTION

Package Code 4B

PART NUMBER	TYPE	R_{ON}
HI-5040	SPST	75Ω
HI-5041	DUAL SPST	75Ω
HI-5042	SPDT	75Ω
HI-5043	DUAL SPDT	75Ω
HI-5044	DPST	75Ω
HI-5045	DUAL DPST	75Ω
HI-5046	DPDT	75Ω
HI-5046A	DPDT	30Ω
HI-5047	4PST	75Ω
HI-5047A	4PST	30Ω
HI-5048	DUAL SPST	30Ω
HI-5049	DUAL DPST	30Ω
HI-5050	SPDT	30Ω
HI-5051	DUAL SPDT	30Ω

FUNCTIONAL DIAGRAM

TYPICAL DIAGRAM



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V^+ - V^-$)	36V
V_R to Ground	V^+, V^-
Digital and Analog Input Voltage	V^+ +4V V^- -4V
Analog Current (S to D)	80mA
Total Power Dissipation*	450mW
Operating Temperature	
HI-50XX-2	-55°C to +125°C
HI-50XX-5	0°C to +75°C
Storage Temperature	-65°C to +150°C

*Derate 6mW/°C above T_A = 75°C

ELECTRICAL CHARACTERISTICS

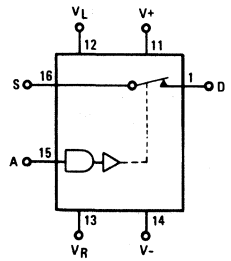
Unless Otherwise Specified
Supplies = +15V, -15V; V_R = 0V; V_{AH} (Logic Level High) = 3.0V; V_{AL} (Logic Level Low) = +0.8V, V_L = +5V
For Test Conditions, consult Performance Characteristics

PARAMETER	TEMP	-55°C to +125°C MIN	TYP	MAX	0°C to +75°C MIN	TYP	MAX	UNITS
ANALOG SWITCH CHARACTERISTICS								
* Analog Signal Range	Full	-15		+15	-15		+15	V
* Ron, "ON" Resistance (Note 1a)	+25°C		50			50		Ω
	Full			75			75	Ω
* Ron, "ON" Resistance (Note 1b)	+25°C		25			25		Ω
	Full			50			50	Ω
Ron, Channel-to-Channel Match (Note 1a)	+25°C		2	10		2	10	Ω
Ron, Channel-to-Channel Match (Note 1b)	+25°C		1	5		1	5	Ω
* $I_{S(OFF)}$ = $I_{D(OFF)}$, Off Input or Output	+25°C		0.8			0.8		nA
Leakage Current	Full		100	500		100	500	nA
* $I_{D(ON)}$, On Leakage Current	+25°C		0.01			0.01		nA
	Full		2	500		2	500	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold	Full			0.8			0.8	V
V_{AH}, Input High Threshold	Full	3.0			3.0			V
* I_A, Input Leakage Current (High or Low)	Full		.01	1.0		.01	1.0	μA
SWITCHING CHARACTERISTICS								
t_{on}, Switch "ON" Time	+25°C		370	1000		370		ns
t_{off}, Switch "OFF" Time	+25°C		280	500		280		ns
Charge Injection (Note 2)	+25°C		5	20		5		mV
"OFF Isolation" (Note 3)	+25°C	75	80			80		dB
"Crosstalk" (Note 3)	+25°C	80	88			88		dB
$C_{S(OFF)}$, Input Switch Capacitance	+25°C		11			11		pF
$C_{D(OFF)}$, Output Switch Capacitance	+25°C		11			11		pF
$C_{D(ON)}$, Output Switch Capacitance	+25°C		22			22		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
$C_{DS(OFF)}$, Drain-To-Source Capacitance	+25°C		0.5			0.5		pF
POWER REQUIREMENTS								
P_D, Quiescent Power Dissipation	+25°C		1.5			1.5		mW
* I^+, +15V Quiescent Current	Full			0.3			0.5	mA
* I^-, -15V Quiescent Current	Full			0.3			0.5	mA
* I_L, +5V Quiescent Current	Full			0.3			0.5	mA
* I_R, Gnd Quiescent Current	Full			0.3			0.5	mA

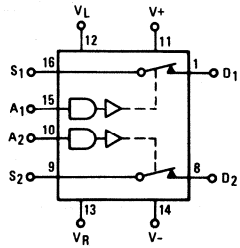
NOTES: 1. V_{OUT} = ±10V, I_{OUT} = 1mA
a) For HI-5040 thru HI-5047
b) For HI-5048 thru HI-5051, HI-5046A/5047A
2. V_{IN} = 0V, C_L = 10,000pF
3. R_L = 100Ω, f= 100 KHz, V_{IN} = 2 V_{PP}, C_L = 5pF

* 100% Tested for Dash 8 at +25°C and +125°C Only.

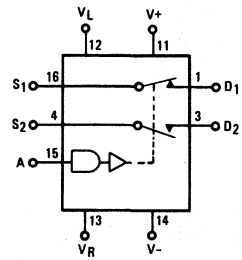
SPST
HI-5040 (75Ω)



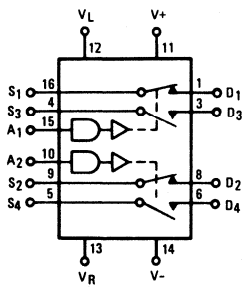
DUAL SPST
HI-5041 (75Ω)



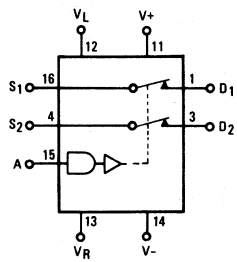
SPDT
HI-5042 (75Ω)



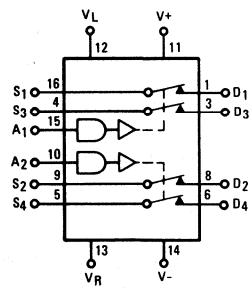
DUAL SPDT
HI-5043 (75Ω)



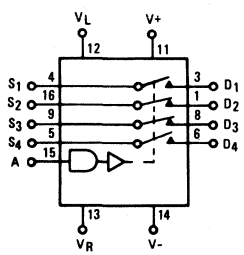
DPST
HI-5044 (75Ω)



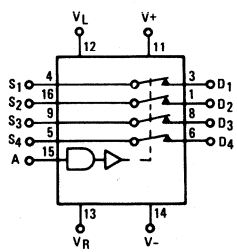
DUAL DPST
HI-5045 (75Ω)



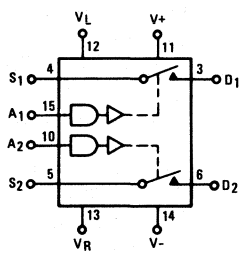
DPDT
HI-5046 (75Ω)
HI-5046A (30Ω)



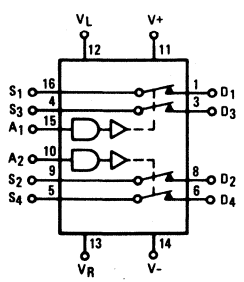
4PST
HI-5047 (75Ω)
HI-5047A (30Ω)



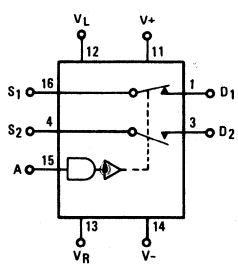
DUAL SPST
HI-5048 (30Ω)



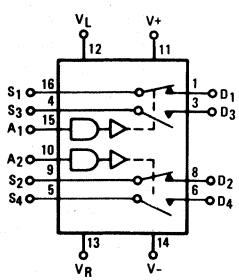
DUAL DPST
HI-5049 (30Ω)



SPDT
HI-5050 (30Ω)

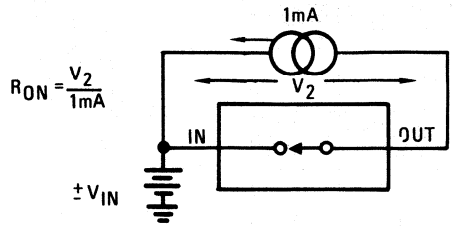


DUAL SPDT
HI-5051 (30Ω)

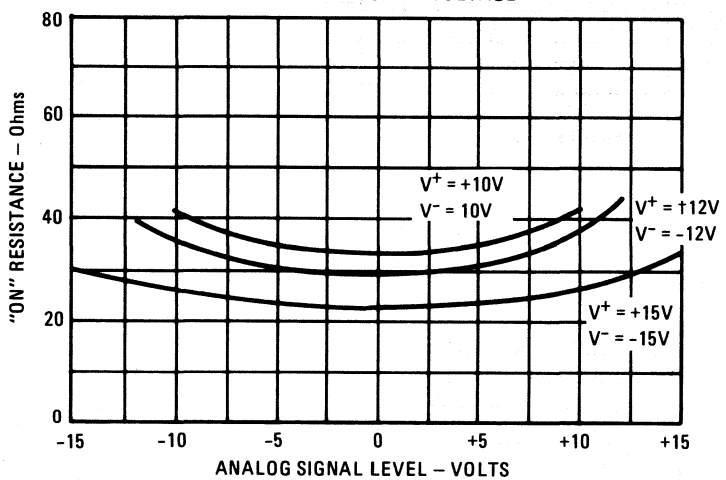


(UNLESS OTHERWISE SPECIFIED $T_A = 25^oC$, $V^+ = +15V$, $V^- = -15V$, $V_L = +5V$, $V_R = 0V$, $V_{AH} = 3.0V$ and $V_{AL} = 0.8V$

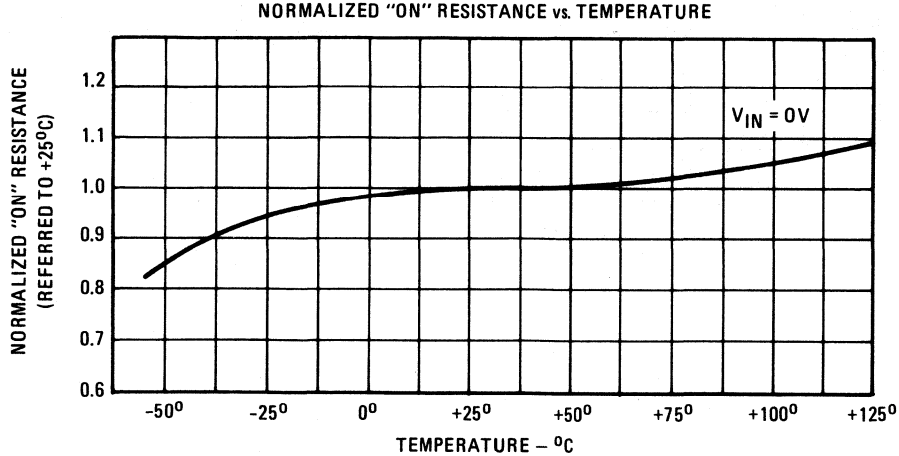
ON RESISTANCE vs. ANALOG SIGNAL LEVEL, SUPPLY VOLTAGE AND TEMPERATURE



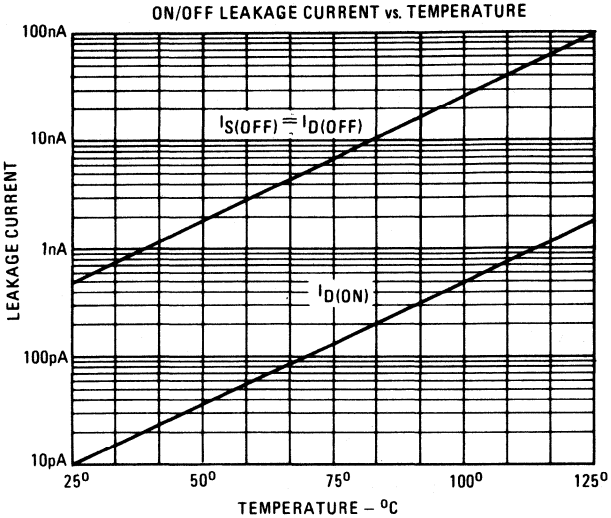
"ON"" RESISTANCE vs. ANALOG SIGNAL LEVEL AND POWER SUPPLY VOLTAGE



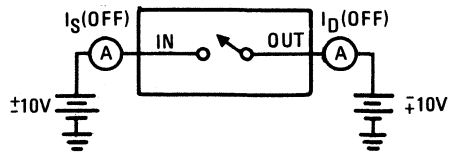
NORMALIZED "ON" RESISTANCE vs. TEMPERATURE



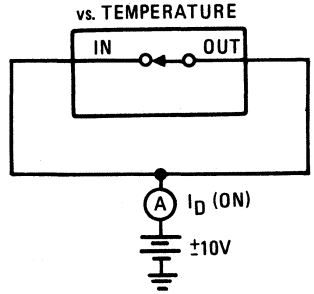
ON/OFF LEAKAGE CURRENT vs. TEMPERATURE



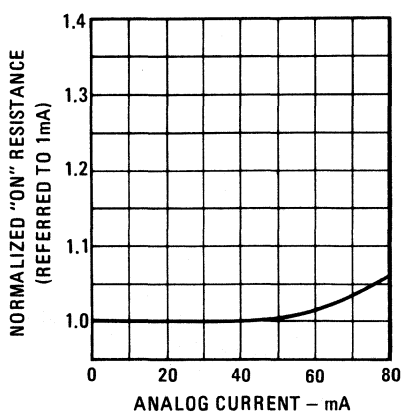
OFF LEAKAGE CURRENT vs. TEMPERATURE



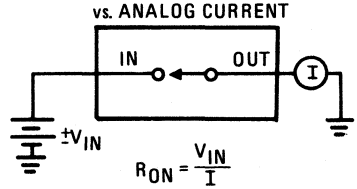
ON LEAKAGE CURRENT vs. TEMPERATURE



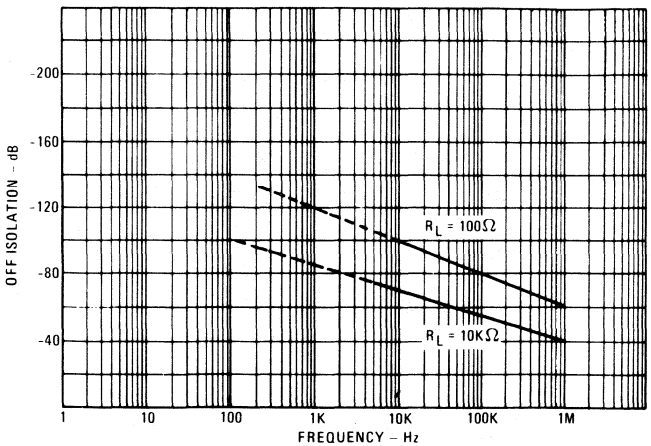
NORMALIZED "ON" RESISTANCE vs. ANALOG CURRENT

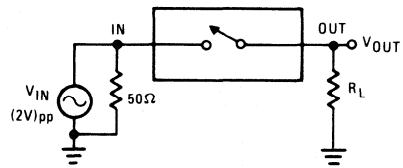


"ON" RESISTANCE vs. ANALOG CURRENT



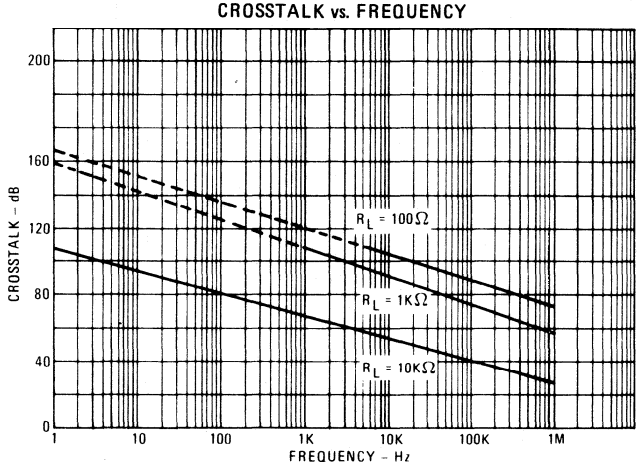
"OFF" ISOLATION vs. FREQUENCY

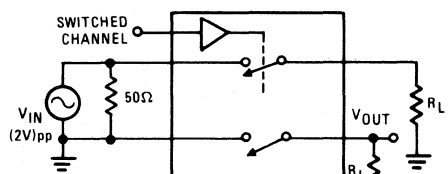




"OFF" ISOLATION = $20 \log\left(\frac{V_{IN}}{V_{OUT}}\right)$

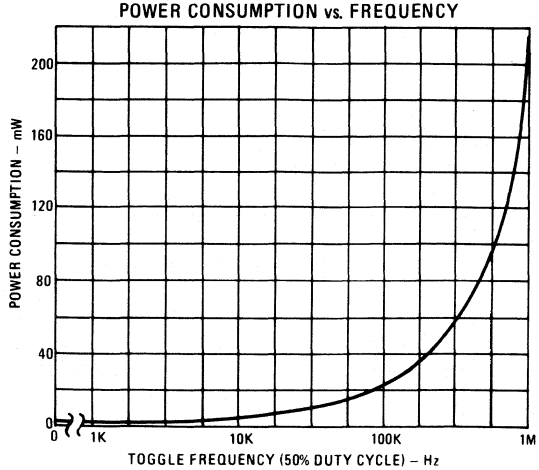
CROSSTALK vs. FREQUENCY

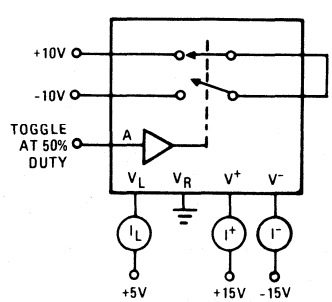




"CROSSTALK" = $20 \log\left(\frac{V_{IN}}{V_{OUT}}\right)$

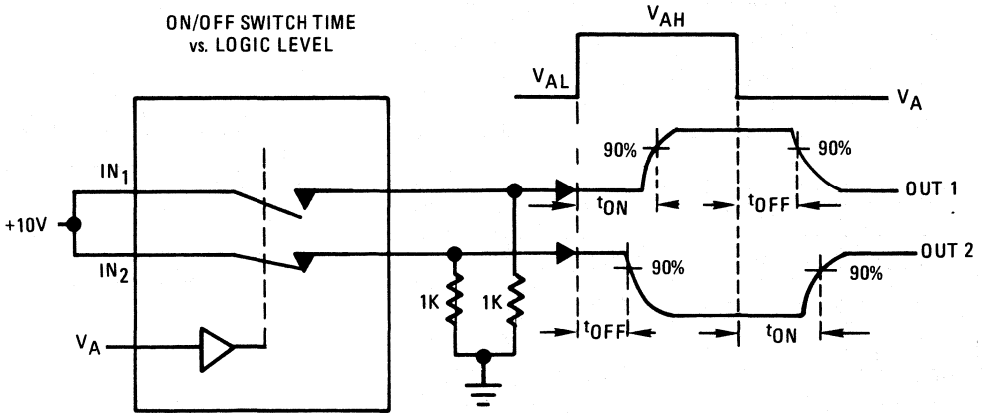
POWER CONSUMPTION vs. FREQUENCY

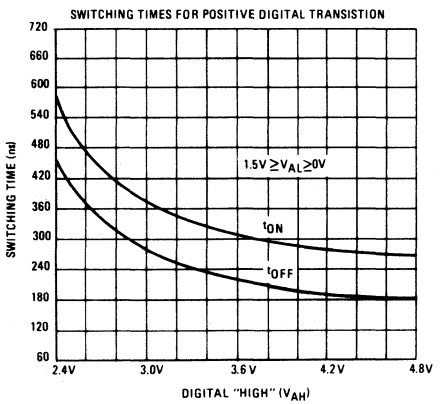


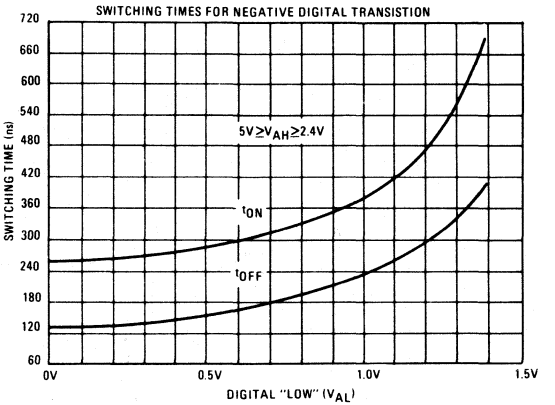


SWITCHING CHARACTERISTICS

ON/OFF SWITCH TIME
vs. LOGIC LEVEL

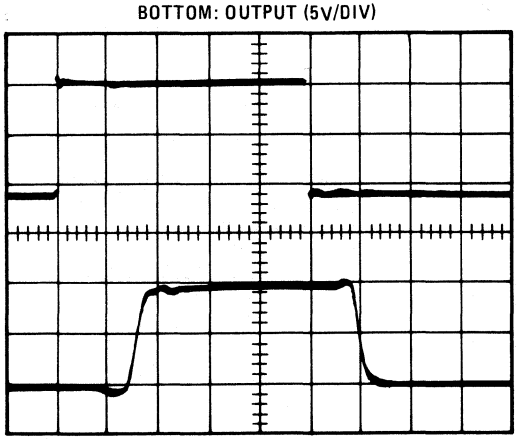






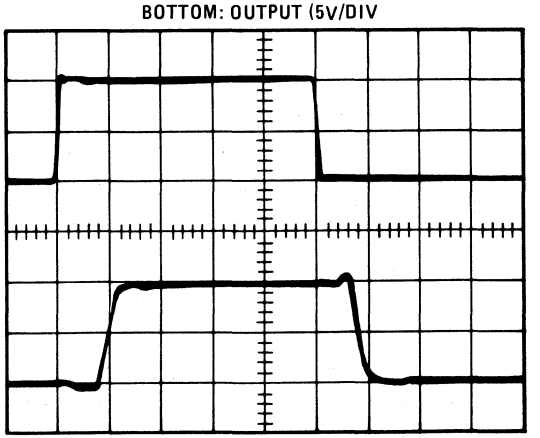
SWITCHING WAVEFORMS

TOP: TTL INPUT (1V/DIV)
V_{AH} = 3V, V_{AL} = 0.8V
BOTTOM: OUTPUT (5V/DIV)



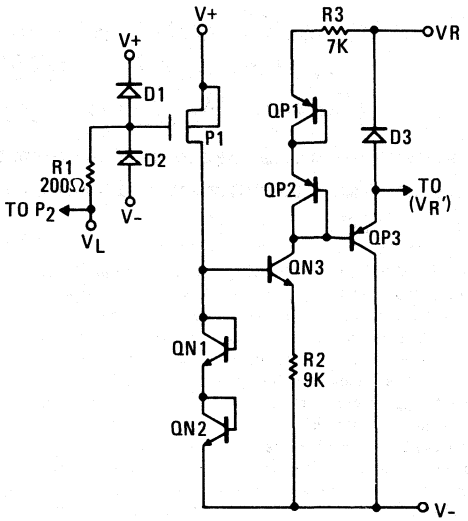
200ns/DIV

TOP: CMOS INPUT (5V/DIV)
V_{AH} = 10V, V_{AL} = 0V
BOTTOM: OUTPUT (5V/DIV



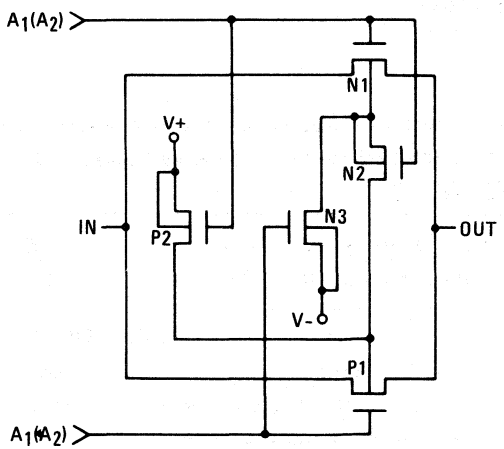
200ns/DIV

TTL/CMOS
REFERENCE CIRCUIT*

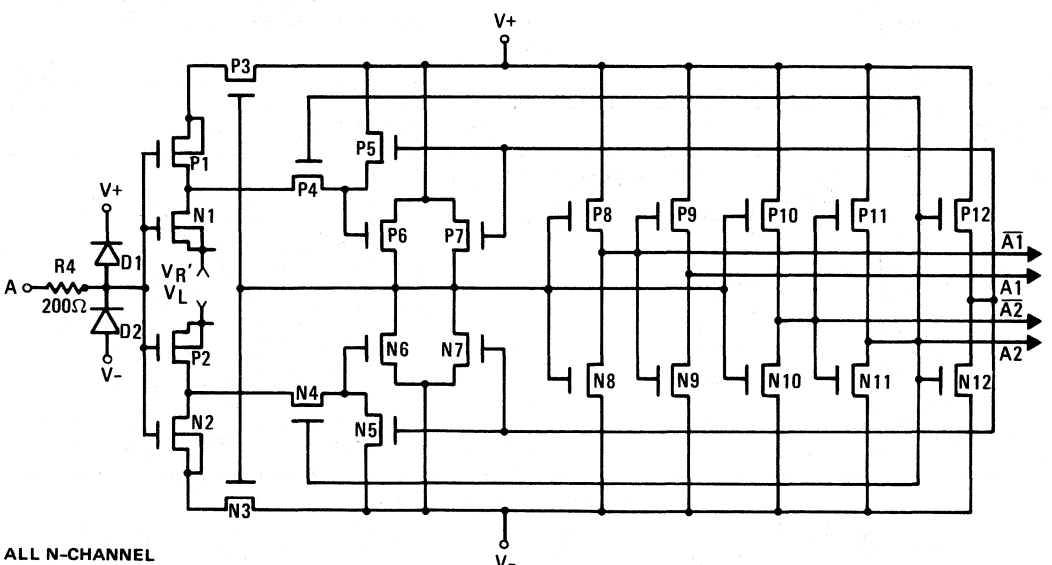


*Connect V^+ to V_L for minimizing power consumption when driving from CMOS circuits

SWITCH CELL



DIGITAL INPUT BUFFER
AND LEVEL SHIFTER



ALL N-CHANNEL
BODIES TO V-

ALL P-CHANNEL
BODIES TO V+

EXCEPT AS SHOWN

3

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HI-506/HI-507

Single 16/Differential 8 Channel CMOS Analog Multiplexers

3

FEATURES

- LOW ON RESISTANCE (TYP.) 170Ω
- WIDE ANALOG SIGNAL RANGE ±15V
- DIRECTLY TTL/CMOS COMPATIBLE 2.4V (LOGIC "1")
- ACCESS TIME (TYP.) 300ns
- HIGH CURRENT CAPABILITY (TYP.) 50mA
- BREAK-BEFORE-MAKE SWITCHING
- NO LATCH-UP

APPLICATIONS

- DATA ACQUISITION SYSTEMS
- PRECISION INSTRUMENTATION
- DEMULTIPLEXING
- SELECTOR SWITCH

DESCRIPTION

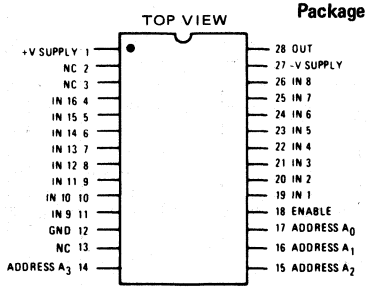
The HI-506/507 are monolithic high performance CMOS analog multiplexers offering built-in channel selection decoding plus an inhibit input for disabling all channels. Dielectric Isolation (DI) is used to fabricate these devices for enhanced reliability and performance over conventional Junction-Isolated (JI) devices. (See Application Note 521). Substrate leakages and parasitic capacitance are much lower in DI resulting in extremely low static errors and high throughput rates. Low output leakage (typically 0.3nA) and low channel ON resistance (170Ω) assure optimum performance in low level or current mode applications. Operation is specified with nominal ±15V supplies, however, supplies as low as ±7V can be used at somewhat lower performance. The HI-506/507 internally develops a +5V digital logic reference from the positive supply which eliminates an additional supply and provides direct TTL/CMOS compatibility without interface pull-up resistors.

The HI-506 is a single-ended 16 channel multiplexer while the HI-507 is a differential 8 channel version. Either device is ideally suited for medical instrumentation, telemetry systems and microprocessor based data acquisition systems.

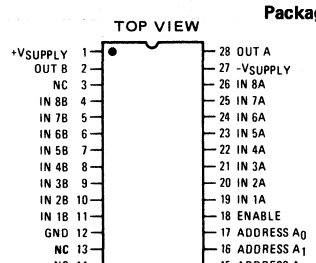
The HI-506-2 and HI-507-2 are specified over -55°C to +125°C, while the -5 versions are specified over 0°C to +75°C.

PINOUT

HI-506 TOP VIEW — Package Code 1M 3P LC

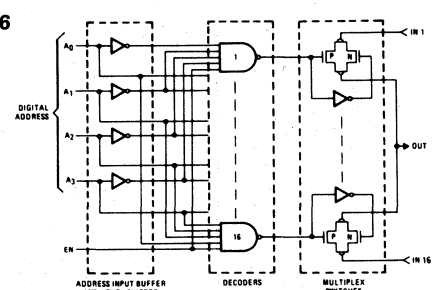


HI-507 TOP VIEW — Package Code 1M 3P LC

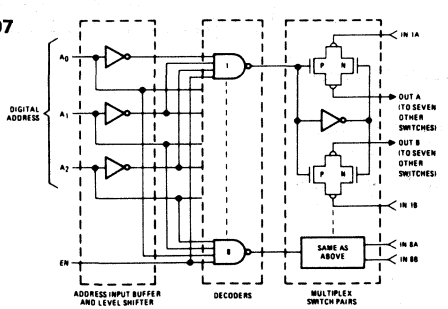


FUNCTIONAL DIAGRAM

HI-506



HI-507



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Between Pins 1 and 27 40V

V_{EN}, V_A, Digital Input Overvoltage:

V_A { V_{Supply} (+) +4V; V_{Supply} (-) -4V

Analog Input Overvoltage: (Note 6)

V_D or V_S { V_{Supply} (+) +2V; V_{Supply} (-) -2V

Total Power Dissipation* 1200 mW

Operating Temperature:

HI-506/HI-507-2 -55°C to +125°C

HI-506/HI-507-5 0°C to +75°C

Storage Temperature -65°C to +150°C

*Derate 8mW/°C above T_A = +25°C

ELECTRICAL CHARACTERISTICS

Unless Otherwise Specified: Supplies = +15V, -15V; V_{AH}(Logic Level High) = +2.4V, V_{AL}(Logic Level Low) = +0.8V. For Test Conditions, consult Performance Characteristics section.

		HI-506/HI-507-2 -55°C to +125°C			HI-506/HI-507-5 0°C to +75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
ANALOG CHANNEL CHARACTERISTICS								
* V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
* R_{ON}, On Resistance (Note 1)	+25°C		170	300		270	400	Ω
	Full			400			500	Ω
* ΔR_{ON}, (Between Channels)	+25°C		6			6		%
* $I_{S(OFF)}$, Off Input Leakage Current	+25°C		0.03			0.03		nA
	Full			±50			±50	nA
* $I_{D(OFF)}$, Off Output Leakage Current	+25°C		0.3			1.0		nA
HI-506	Full			±500			±500	nA
HI-507	Full			±250			±250	nA
* $I_{D(ON)}$, On Channel Leakage Current	+25°C		0.3			1.0		nA
HI-506	Full			±500			±500	nA
HI-507	Full			±250			±250	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold	Full			+0.8			+0.8	V
V_{AH}, Input High Threshold	Full	+2.4			+2.4			V
* I_A, Input Leakage Current (High or Low)(Note 2)	Full			1.0			5.0	μA
SWITCHING CHARACTERISTICS								
t_A, Access Time	+25°C		300	1000		300		ns
t_{OPEN}, Break-Before Make Delay	+25°C		80			80		ns
$t_{ON(EN)}$, Enable Delay (ON)	+25°C		300	1000		300		ns
$t_{OFF(EN)}$, Enable Delay (OFF)	+25°C		300	1000		300		ns
Settling Time (0.1%)	+25°C		1.2			1.2		μs
(0.025%)	+25°C		2.4			2.4		μs
"Off Isolation" (Note 3)	+25°C		75			75		dB
$C_{S(OFF)}$, Channel Input Capacitance	+25°C		4			4		pF
$C_{D(OFF)}$, Channel Output Capacitance								
HI-506	+25°C		44			44		pF
HI-507	+25°C		22			22		pF
C_A, Digital Input Capacitance	+25°C		2.2			2.2		pF
$C_{DS(OFF)}$, Input to Output Capacitance	+25°C		0.08			0.08		pF
POWER REQUIREMENTS								
* I+, Current Pin 1 (Note 4)	Full		1.7	3.0		3.4	5.0	mA
* I-, Current Pin 27 (Note 4)	Full		0.4	1.0		0.8	2.0	mA
* I+, Standby (Note 5)	Full		1.7	3.0		3.4	5.0	mA
* I-, Standby (Note 5)	Full		0.4	1.0		0.8	2.0	mA

NOTES:
1. V_{OUT} = ±10V, I_{OUT} = -1mA
2. Digital Inputs are Mos Gates. Typical Leakage Less Than 1nA.
3. V_{EN} = 0.8V, R_L = 1K, C_L = 28pF, V_S = 7VRMS, f = 500kHz.
4. V_{EN} = 4.0V, All V_A = 4.0V
5. V_{EN} = 0V, All V_A = 0V
6. If Analog Input Overvoltage Conditions are Anticipated, Use of HI-506A/507A Protected Multiplexers is Recommended. See HI-506A/507A Data Sheet.

* 100% Tested for Dash 8 at +25°C and +125°C Only.

TRUTH TABLES

HI-506

A_3	A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	X	L	NONE
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

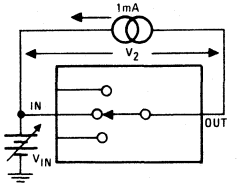
HI-507

A_2	A_1	A_0	EN	ON SWITCH PAIR
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

Unless Otherwise Specified; $T_A = 25^oC$, $V_{Supply} = \pm 15V$, $V_{AH} = 2.4V$, $V_{AL} = 0.8V$.

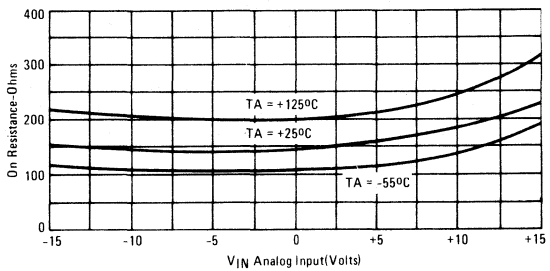
TEST CIRCUIT NO. 1

ON RESISTANCE vs. INPUT SIGNAL LEVEL, SUPPLY VOLTAGE

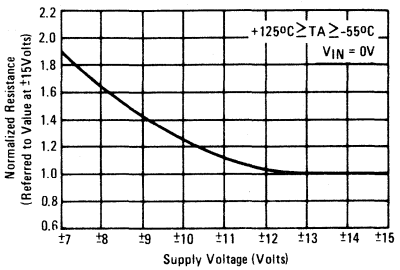


$R_{ON} = \frac{V_2}{1mA}$

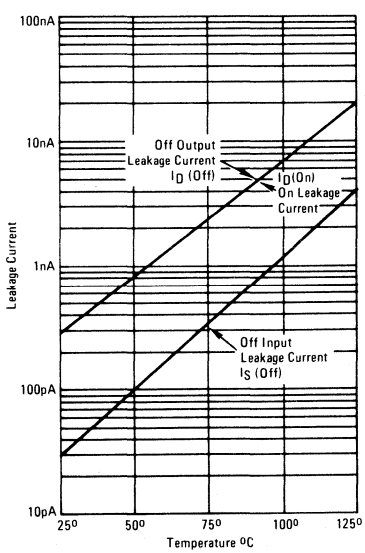
ON RESISTANCE vs. ANALOG INPUT VOLTAGE, TEMPERATURE



NORMALIZED ON RESISTANCE vs. SUPPLY VOLTAGE

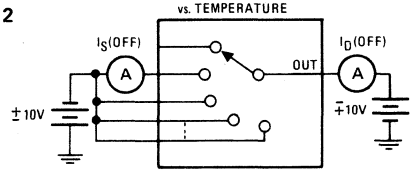


LEAKAGE CURRENT vs. TEMPERATURE



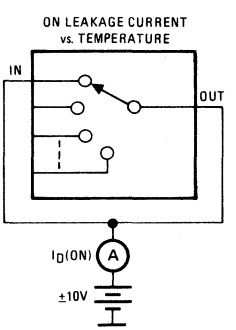
TEST CIRCUIT NO. 2

OFF LEAKAGE CURRENT vs. TEMPERATURE

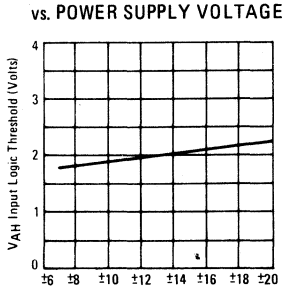


TEST CIRCUIT NO. 3

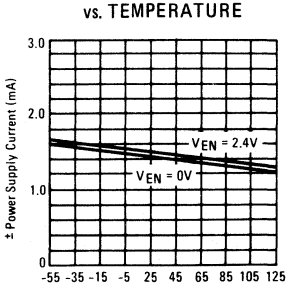
ON LEAKAGE CURRENT vs. TEMPERATURE



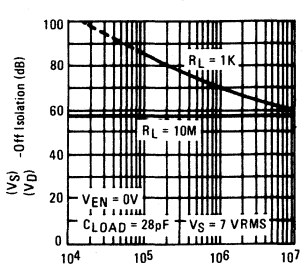
LOGIC THRESHOLD vs. POWER SUPPLY VOLTAGE



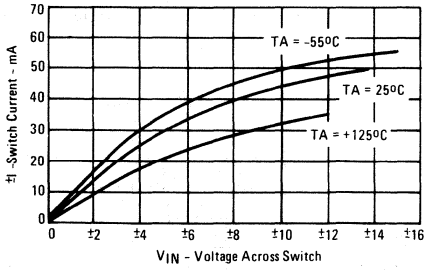
POWER SUPPLY CURRENT vs. TEMPERATURE



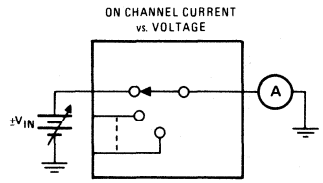
OFF ISOLATION vs. FREQUENCY



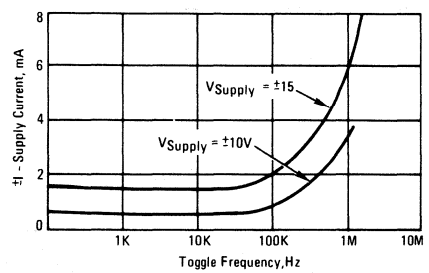
ON CHANNEL CURRENT vs. VOLTAGE



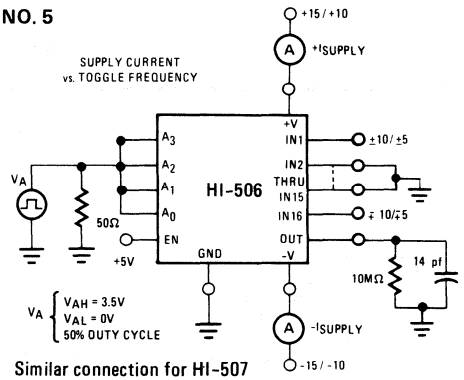
TEST CIRCUIT NO. 4



SUPPLY CURRENT vs. TOGGLE FREQUENCY

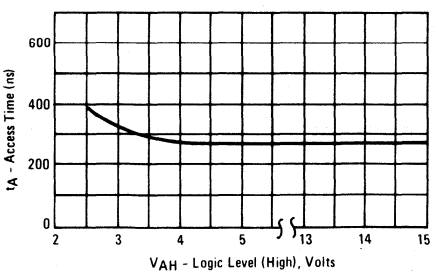


TEST CIRCUIT NO. 5

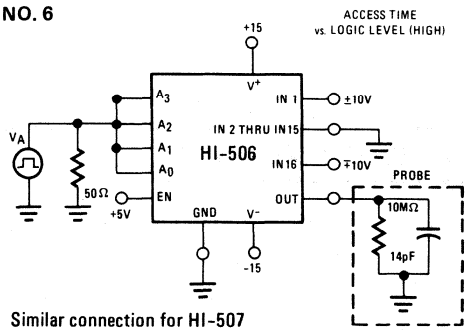


Similar connection for HI-507

ACCESS TIME vs. LOGIC LEVEL (HIGH)

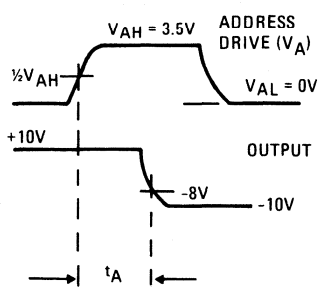


TEST CIRCUIT NO. 6

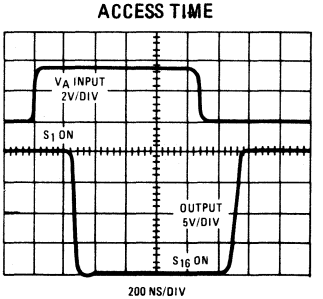


Similar connection for HI-507

SWITCHING WAVEFORMS



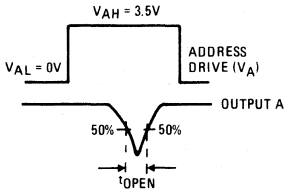
ACCESS TIME

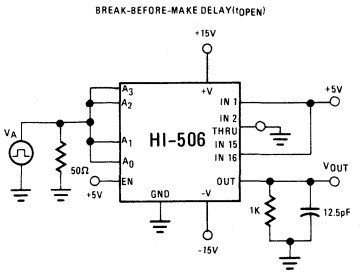


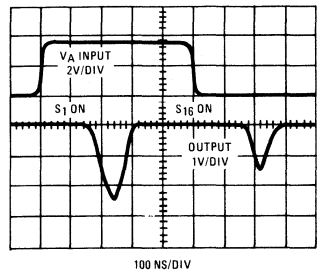
SWITCHING WAVEFORMS (continued)

TEST CIRCUIT NO. 7

BREAK-BEFORE-MAKE DELAY (t_{OPEN})



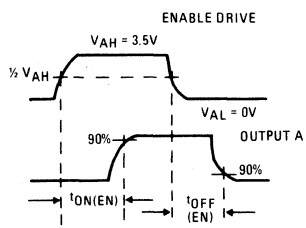


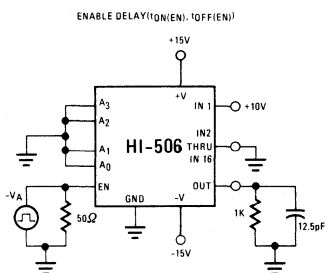


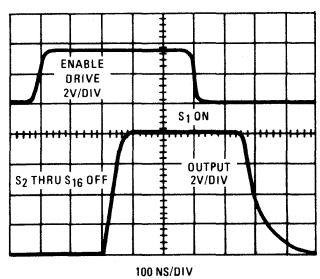
Similar connection for HI-507

TEST CIRCUIT NO. 8

ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)



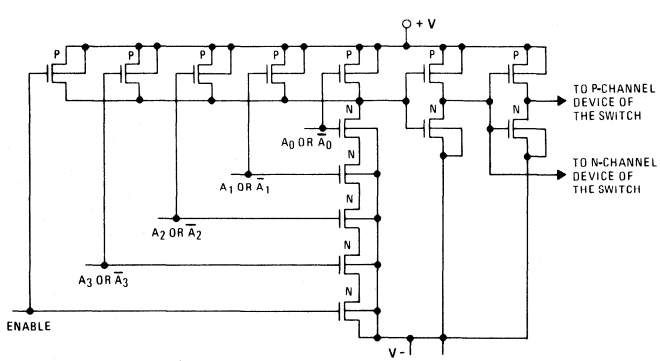




Similar connection for HI-507

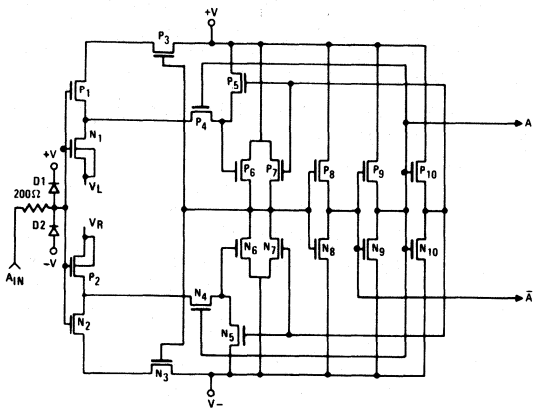
SCHEMATIC DIAGRAMS

ADDRESS DECODER



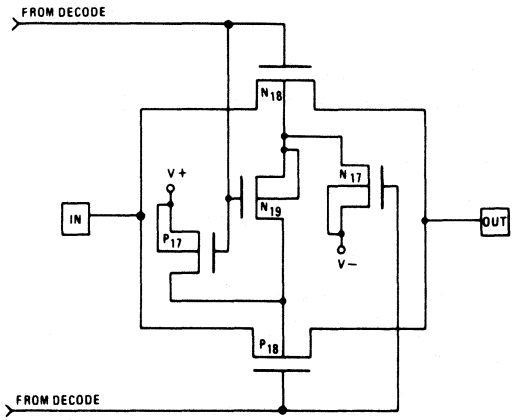
Delete A_3 or $\overline{A_3}$ Input for HI-507

ADDRESS INPUT BUFFER
LEVER SHIFTER

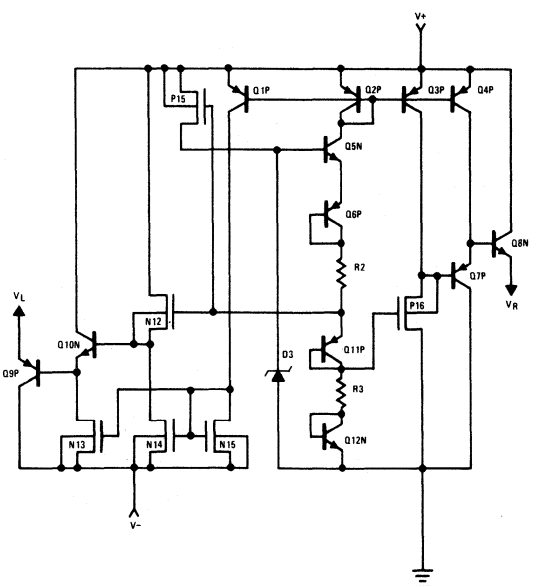


All N-Channel Bodies to V-
All P-Channel Bodies to V+ Unless Otherwise Indicated.

MULTIPLEX SWITCH



TTL REFERENCE CIRCUIT



HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HI-506A/HI-507A

16 Channel CMOS Analog Multiplexer with Overvoltage Protection

3

FEATURES

- ANALOG/DIGITAL OVERVOLTAGE PROTECTION
- FAIL SAFE WITH POWER LOSS (NO LATCHUP)
- BREAK-BEFORE-MAKE SWITCHING
- DTL/TTL AND CMOS COMPATIBLE
- ANALOG SIGNAL RANGE ±15V
- ACCESS TIME (TYP.) 500ns
- SUPPLY CURRENT AT 1MHz ADDRESS TOGGLE (TYP.) 4mA
- STANDBY POWER (TYP.) 7.5mW

APPLICATIONS

- DATA ACQUISITION
- INDUSTRIAL CONTROLS
- TELEMETRY

DESCRIPTION

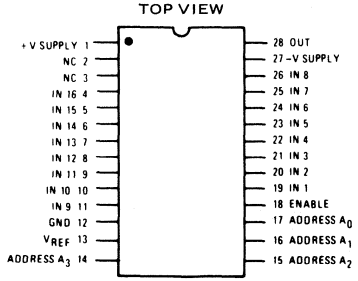
The HI-506A and HI-507A are dielectrically isolated CMOS analog multiplexers incorporating an important feature; they withstand analog input voltages much greater than the supplies. This is essential in any system where the analog inputs originate outside the equipment. They can withstand a continuous input up to 10 volts greater than either supply, which eliminates the possibility of damage when supplies are off, but input signals are present. Equally important, they can withstand brief input transient spikes of several hundred volts; which otherwise would require complex external protection networks. Necessarily, ON resistance is somewhat higher than similar unprotected devices, but very low leakage currents combine to produce low errors. Application Notes 520 and 521 further explain these features.

The HI-506A-2 and HI-507A-2 are specified over -55°C to +125°C while the -5 versions are specified over 0°C to +75°C.

PINOUT

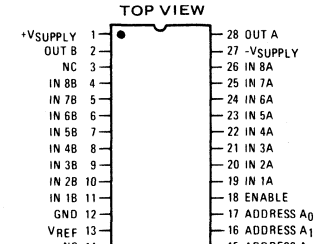
HI-506A — **Package Code 1M, 3P, LC**

TOP VIEW



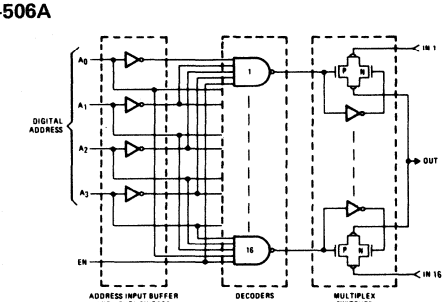
HI-507A — **Package Code 1M, 3P, LC**

TOP VIEW

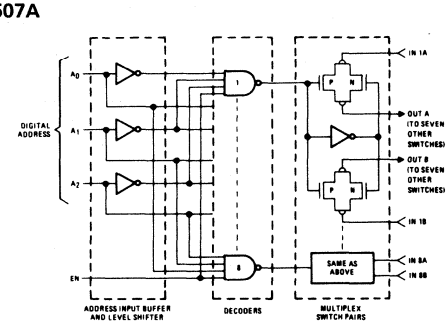


FUNCTIONAL DIAGRAM

HI-506A



HI-507A



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Between Pins 1 and 27	40V	Total Power Dissipation*	1200mW
V_{REF} to Ground V+ to Ground	+20V	Operating Temperature	
V_{EN}, V_A, Digital Input Overvoltage:		HI-506A/507A-2	-55°C to +125°C
V_A (V_{Supply} (+))	+4V	HI-506A/507A-5	0°C to +75°C
V_A (V_{Supply} (−))	-4V	Storage Temperature	-65°C to +150°C
Analog Overvoltage:			
V_S (V_{Supply} (+))	+20V		
V_S (V_{Supply} (−))	-20V	*Derate 8mW/°C above T_A = +25°C	

ELECTRICAL CHARACTERISTICS (Unless otherwise specified)

Supplies = +15V, -15V; V_{REF} (Pin 13) = Open; V_{AH} (Logic Level High) = +4.0V; V_{AL} (Logic Level Low) = +0.8V
For Test Conditions, consult Performance Characteristics section.

PARAMETER		TEMP.	HI-506A/507A-2 -55°C to +125°C MIN.	TYP.	MAX.	HI-506A/507A-5 0°C to +75°C MIN.	TYP.	MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS									
*V_S, Analog Signal Range		Full	-15		+15	-15		+15	V
*R_{ON}, On Resistance (Note 1)		+25°C		1.2	1.5		1.5	1.8	KΩ
		Full		1.5	2.0		1.8	2.0	KΩ
*I_S (OFF), Off Input Leakage Current		+25°C		0.03			0.03		nA
		Full			±50			±50	nA
*I_D (OFF), Off Output Leakage Current		+25°C		1.0			1.0		nA
	HI-506A	Full			±500			±500	nA
	HI-507A	Full			±250			±250	nA
*I_D (OFF) with Input Overvoltage Applied (Note 2)		+25°C		4.0			4.0		nA
		Full			2.0				μA
*I_D (ON), On Channel Leakage Current		+25°C		0.1			0.1		nA
	HI-506A	Full			±500			±500	nA
	HI-507A	Full			±250			±250	nA
DIGITAL INPUT CHARACTERISTICS									
V_{AL}, Input Low Threshold | TTL Drive		Full			0.8			0.8	V
V_{AH}, Input High Threshold | (Note 7)		Full	4.0			4.0			V
V_{AL} | MOS Drive (Note 3)		+25°C			0.8			0.8	V
V_{AH} |		+25°C	6.0			6.0			V
*I_A, Input Leakage Current (High or Low)		Full			1.0			5.0	μA
SWITCHING CHARACTERISTICS									
t_A, Access Time		+25°C		0.5	1.0		0.5		μs
t_{OPEN}, Break-Before Make Delay		+25°C		80			80		ns
t_{ON} (EN), Enable Delay (ON)		+25°C		300			300		ns
t_{OFF} (EN), Enable Delay (OFF)		+25°C		300			300		ns
Settling Time (0.1%)		+25°C		1.3			1.3		μs
(0.025%)		+25°C		4.4			4.4		μs
"Off Isolation" (Note 4)		+25°C		65			65		dB
C_S (OFF), Channel Input Capacitance		+25°C		5			5		pF
C_D (OFF), Channel Output Capacitance	HI-506A	+25°C		50			50		pF
	HI-507A	+25°C		25			25		pF
C_A, Digital Input Capacitance		+25°C		5			5		pF
C_{DS} (OFF), Input to Output Capacitance		+25°C		0.1			0.1		pF
POWER REQUIREMENTS									
P_D, Power Dissipation		Full		7.5			7.5		mW
*I+, Current Pin 1 (Note 5)		Full		0.5	2.0		0.5	5.0	mA
*I−, Current Pin 27 (Note 5)		Full		0.02	1.0		0.02	2.0	mA
*I+, Standby (Note 6)		Full		0.5	2.0		0.5	5.0	mA
*I−, Standby (Note 6)		Full		0.02	1.0		0.02	2.0	mA

NOTES:
1. V_{OUT} = ±10V, I_{OUT} = - 100 μA.
2. Analog Overvoltage = ±33V.
3. V_{REF} = +10V.
4. V_{EN} = 0.8V, R_L = 1K, C_L = 7pF, V_S = 3VRMS, f = 500KHz.
5. V_{EN} = +4.0V.
6. V_{EN} = 0.8V.
7. To drive from DTL/TTL circuits, 1KΩ pull-up resistors to +5.0V supply are recommended.

* 100% Tested for Dash 8 at +25°C and +125°C Only.

TRUTH TABLES

HI-506A

A_3	A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	X	L	NONE
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

HI-507A

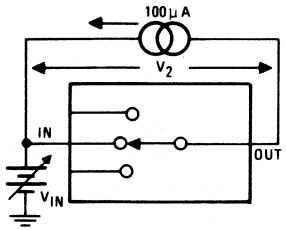
A_2	A_1	A_0	EN	ON SWITCH PAIR
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

(UNLESS OTHERWISE SPECIFIED $T_A = 25^oC$, $V_{SUPPLY} = \pm 15V$, $V_{AH} = +4V$, $V_{AL} = 0.8V$ AND V_{REF} = OPEN.)

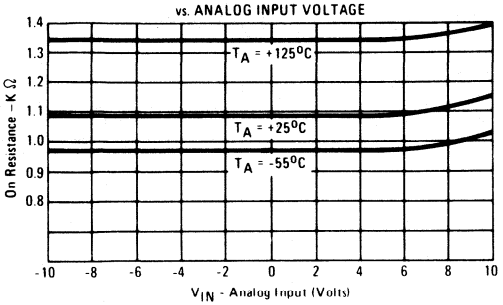
TEST CIRCUIT NO.1

ON RESISTANCE vs. INPUT SIGNAL LEVEL, SUPPLY VOLTAGE

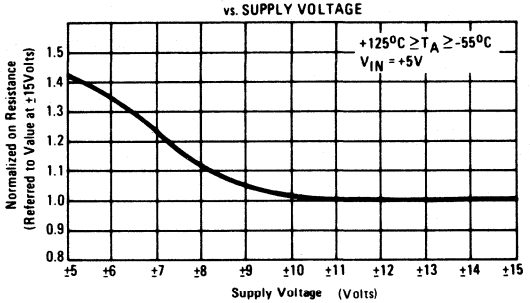
$R_{ON} = \frac{V_2}{100\mu A}$



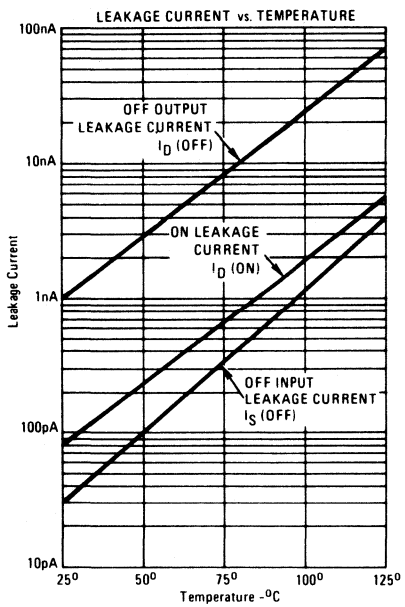
ON RESISTANCE vs. ANALOG INPUT VOLTAGE



NORMALIZED ON RESISTANCE vs. SUPPLY VOLTAGE

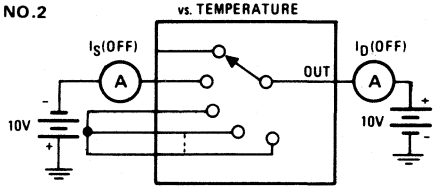


LEAKAGE CURRENT vs. TEMPERATURE



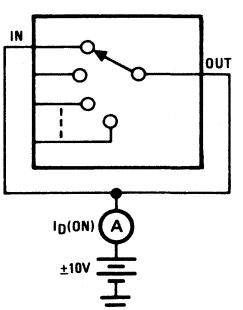
TEST CIRCUIT NO.2

OFF LEAKAGE CURRENT vs. TEMPERATURE

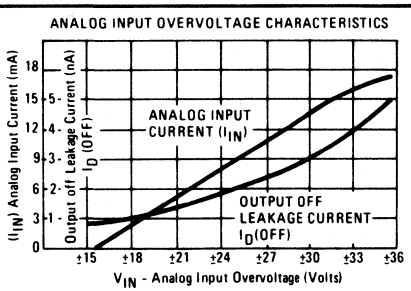


TEST CIRCUIT NO.3

ON LEAKAGE CURRENT vs. TEMPERATURE

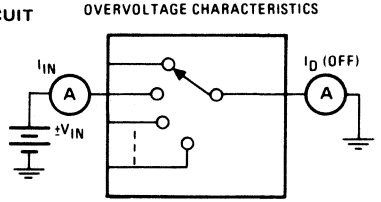


ANALOG INPUT OVERVOLTAGE CHARACTERISTICS

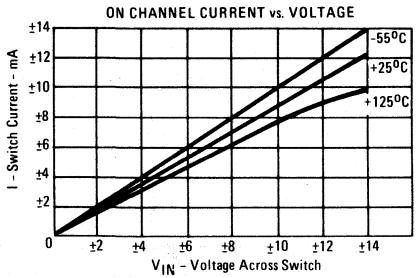


TEST CIRCUIT NO.4

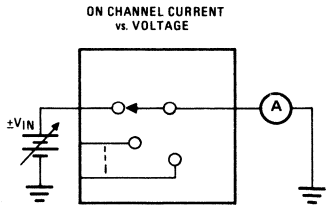
ANALOG INPUT OVERVOLTAGE CHARACTERISTICS

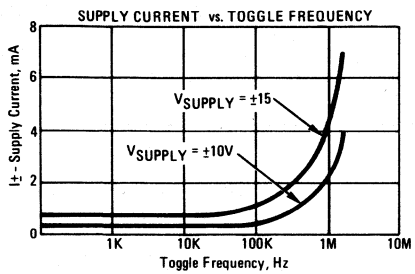


PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS (continued)

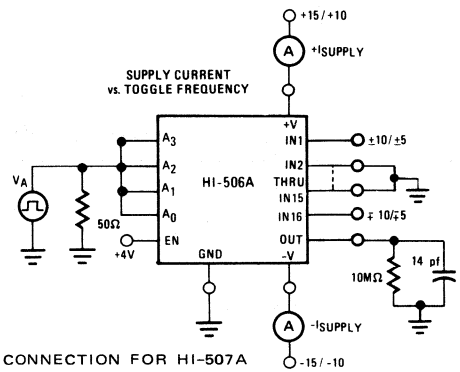


TEST CIRCUIT NO.5

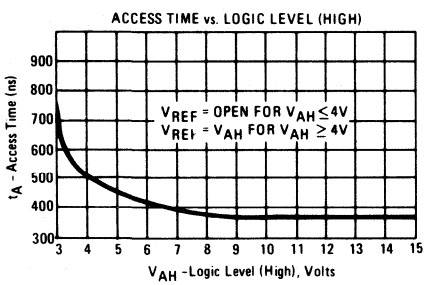




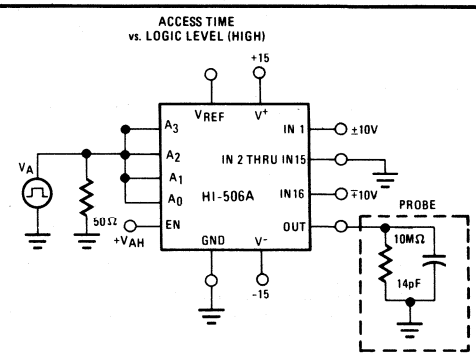
TEST CIRCUIT NO.6



SIMILAR CONNECTION FOR HI-507A

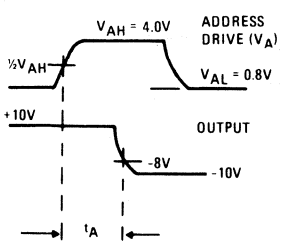


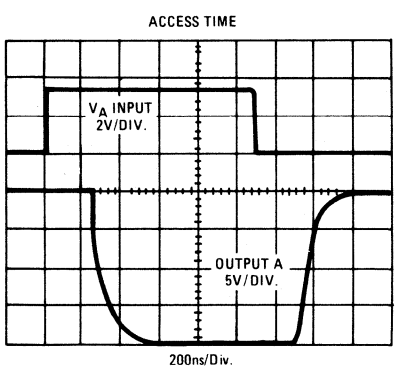
TEST CIRCUIT NO.7



SIMILAR CONNECTION FOR HI-507A

SWITCHING WAVEFORMS

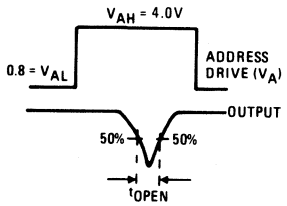


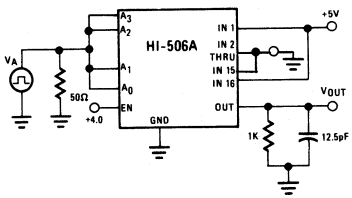


SWITCHING WAVEFORMS (continued)

TEST CIRCUIT
NO.8

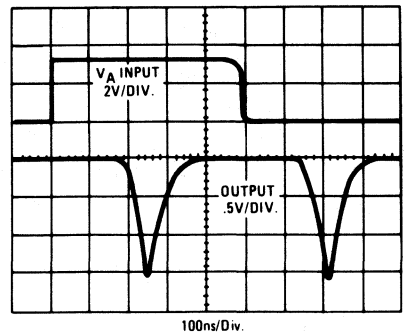
BREAK BEFORE MAKE DELAY (t_{OPEN})





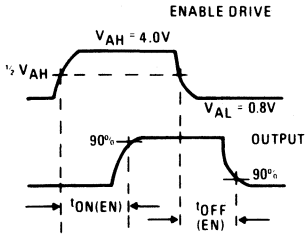
SIMILAR CONNECTION FOR HI-507A

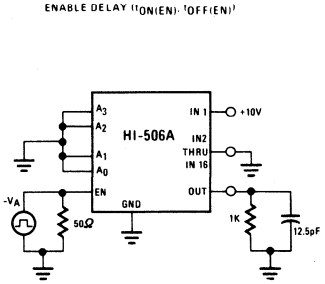
BREAK BEFORE MAKE DELAY (t_{OPEN})



TEST CIRCUIT
NO.9

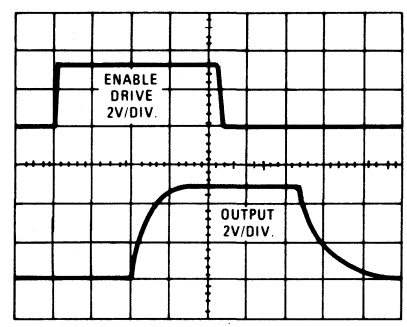
ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)





SIMILAR CONNECTION FOR HI-507A

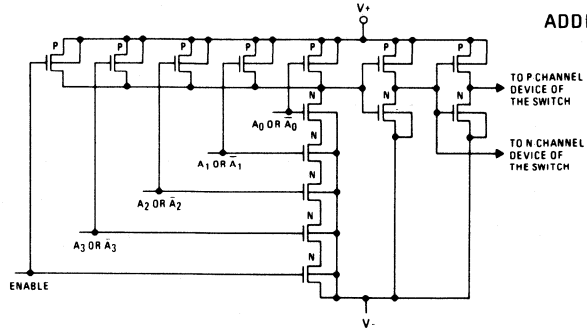
ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)



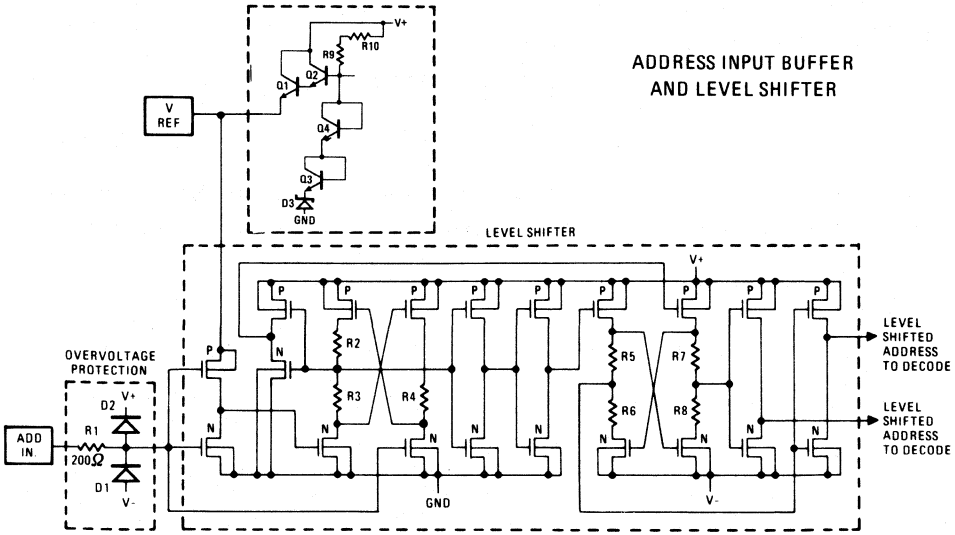
SCHEMATIC DIAGRAMS

DELETE A_3 or $\overline{A}_3$
INPUT FOR HI-507A

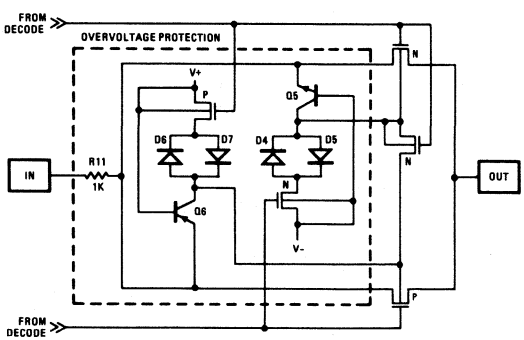
ADDRESS DECODER



ADDRESS INPUT BUFFER
AND LEVEL SHIFTER



MULTIPLEX SWITCH



3

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HI-508A/509A

8 Channel CMOS Analog Multiplexers with Overvoltage Protection

3

FEATURES

- ANALOG/DIGITAL OVERVOLTAGE PROTECTION
- FAIL SAFE WITH POWER LOSS (NO LATCHUP)
- BREAK-BEFORE-MAKE SWITCHING
- DTL/TTL AND CMOS COMPATIBLE
- ANALOG SIGNAL RANGE ±15V
- ACCESS TIME (TYP.) 500ns
- SUPPLY CURRENT AT 1MHz ADDRESS TOGGLE (TYP.) 4mA
- STANDBY POWER (TYP.) 7.5mW

APPLICATIONS

- DATA ACQUISITION
- INDUSTRIAL CONTROLS
- TELEMETRY

DESCRIPTION

The HI-508A and HI-509A are dielectrically isolated CMOS analog multiplexers incorporating an important feature; they withstand analog input voltages much greater than the supplies. This is essential in any system where the analog inputs originate outside the equipment. They can withstand a continuous input up to 10 volts greater than either supply, which eliminates the possibility of damage when supplies are off, but input signals are present. Equally important, they can withstand brief input transient spikes of several hundred volts; which otherwise would require complex external protection networks. Necessarily, ON resistance is somewhat higher than similar unprotected devices, but very low leakage currents combine to produce low errors. Application Notes 520 and 521 further explain these features.

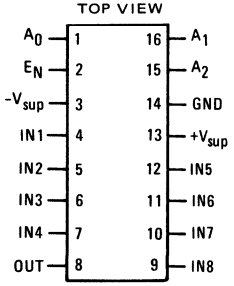
The HI-508A-2 and HI-509A-2 are specified over -55°C to +125°C while the -5 versions are specified over 0°C to +75°C.

PINOUT

HI-508A

Package Code 4B
3L
LA

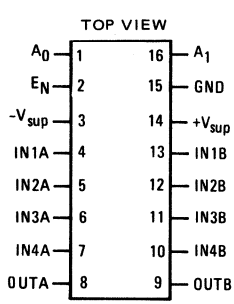
TOP VIEW



HI-509A

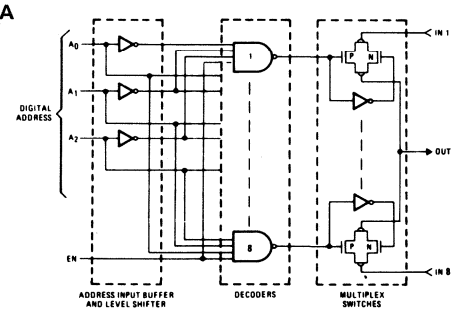
Package Code 4B
3L
LA

TOP VIEW

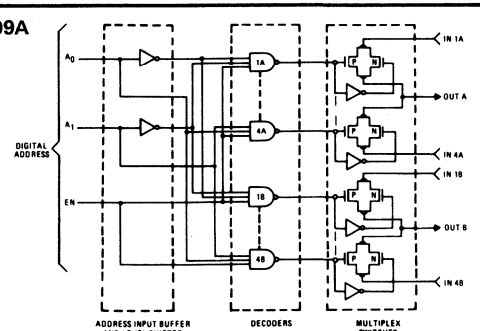


FUNCTIONAL DIAGRAM

HI-508A



HI-509A



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage between Supply Pins 40V

V+ to Ground 20V

V_{EN}, V_A, Digital Input Overvoltage:

V_A { V_{Supply} (+) +4V; V_{Supply} (-) -4V

Analog Input Overvoltage:

V_S { V_{Supply} (+) +20V; V_{Supply} (-) -20V

Total Power Dissipation* 725 mW

Operating Temperature:

HI-508A/HI-509A-2 -55°C to +125°C

HI-508A/HI-509A-5 0°C to +75°C

Storage Temperature -65°C to +150°C

*Derate 8mW/°C above t_A = 75°C

ELECTRICAL CHARACTERISTICS (Unless Otherwise Specified)

Supplies = +15V, -15V; V_{AH} (Logic Level High) = +4.0V; V_{AL} (Logic Level Low) = +0.8V
For Test Conditions, consult Performance Characterisitcs section.

		HI-508A/509A-2 -55°C to +125°C			HI-508A/509A-5 0°C to +75°C			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP	MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS								
*V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
* R_{ON}, On Resistance (Note 1)	+25°C		1.2	1.5		1.5	1.8	KΩ
	Full		1.5	1.8		1.8	2.0	KΩ
*$I_{S(OFF)}$, Off Input Leakage Current	+25°C		0.03			0.03		nA
	Full			±50			±50	nA
*$I_{D(OFF)}$, Off Output Leakage Current	+25°C		1.0			1.0		nA
HI-508A	Full			±250			±250	nA
HI-509A	Full			±125			±125	nA
*$I_{D(OFF)}$ with Input Overvoltage Applied (Note 2)	+25°C		4.0			4.0		nA
	Full			2.0				μA
*$I_{D(ON)}$, On Channel Leakage Current	+25°C		0.1			0.1		nA
HI-508A	Full			±250			±250	nA
HI-509A				±125			±125	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold (Note 6)	Full			0.8			0.8	V
V_{AH}, Input High Threshold (Note 6)	Full	4.0			4.0			V
*I_A, Input Leakage Current (High or Low)	Full			1.0			1.0	μA
SWITCHING CHARACTERISTICS								
t_A, Access Time	+25°C		0.5	1.0		0.5		μs
t_{OPEN}, Break - Before Make Delay	+25°C		80			80		ns
$t_{ON(EN)}$, Enable Delay (ON)	+25°C		300			300		ns
$t_{OFF(EN)}$, Enable Delay (OFF)	+25°C		300			300		ns
Settling Time (0.1%)	+25°C		1.2			1.2		μs
(0.025%)	+25°C		3.5			3.5		μs
"OFF Isolation" (Note 3)	+25°C		65			65		dB
$C_{S(OFF)}$, Channel Input Capacitance	+25°C		5			5		pF
$C_{D(OFF)}$, Channel Output Capacitance								
HI-508A	+25°C		25			25		pF
HI-509A	+25°C		12			12		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
$C_{DS(OFF)}$, Input to Output Capacitance	+25°C		0.1			0.1		pF
POWER REQUIREMENTS								
P_D, Power Dissipation	Full		7.5			7.5		mW
*I+, Current (Note 4)	Full		0.5	2.0		0.5	5.0	mA
*I-, Current (Note 4)	Full		0.02	1.0		0.02	2.0	mA
*I+, Standby (Note 5)	Full		0.5	2.0		0.5	5.0	mA
*I-, Standby (Note 5)	Full		0.02	1.0		0.02	2.0	mA

NOTES:
1. V_{OUT} = ±10V, I_{OUT} = -100μA
2. Analog Overvoltage = ±33V
3. V_{EN} = 0.8V, R_L = 1K, C_L = 7pF, V_S = 3V RMS, f = 500KHz
4. V_{EN} = +4.0V
5. V_{EN} = 0.8V
6. To drive from DTL/TTL Circuits, 1KΩ pull-up resistors to +5.0V supply are recommended

* 100% Tested for Dash 8 at +25°C and +125°C Only.

TRUTH TABLES

HI-508A

A_2	A_1	A_0	E_N	"ON" CHANNEL
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

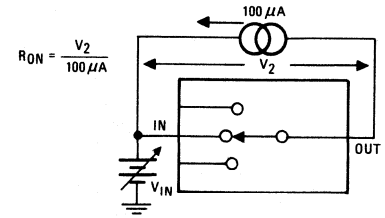
HI-509A

A_1	A_0	EN	ON SWITCH PAIR
X	X	L	NONE
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

3

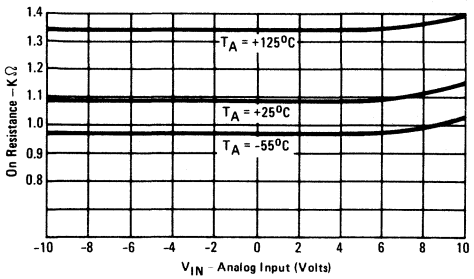
UNLESS OTHERWISE SPECIFIED: $T_A = 25^oC$, $V_{SUPPLY} = +15V$, $V_{AH} = +4V$, $V_{AL} = 0.8V$

TEST CIRCUIT NO. 1

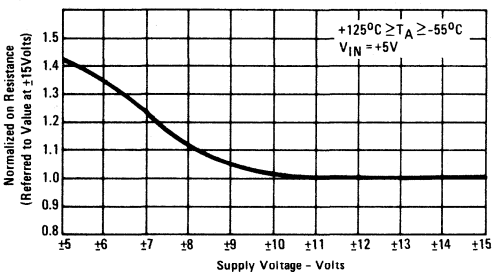


ON RESISTANCE vs. INPUT SIGNAL LEVEL, SUPPLY VOLTAGE

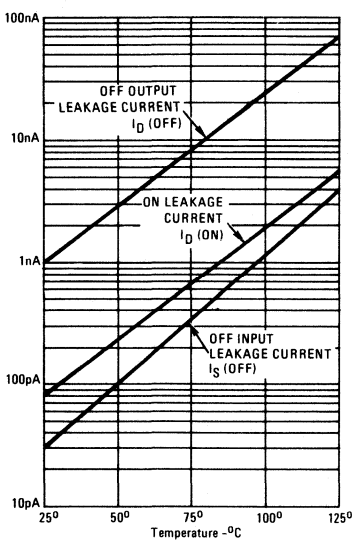
ON RESISTANCE vs. ANALOG INPUT VOLTAGE



NORMALIZED ON RESISTANCE vs. SUPPLY VOLTAGE

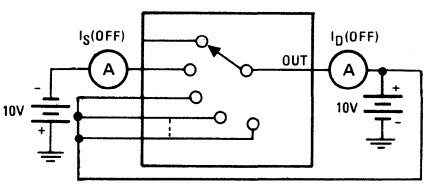


LEAKAGE CURRENT vs. TEMPERATURE



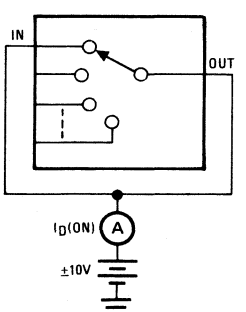
TEST CIRCUIT NO. 2

OFF LEAKAGE CURRENT vs. TEMPERATURE

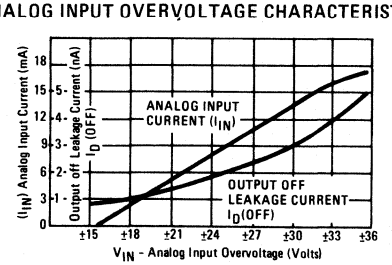


ON LEAKAGE CURRENT vs. TEMPERATURE

TEST CIRCUIT NO. 3

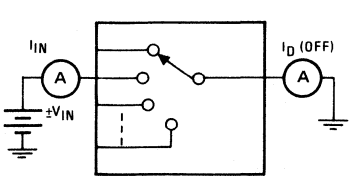


ANALOG INPUT OVERVOLTAGE CHARACTERISTICS

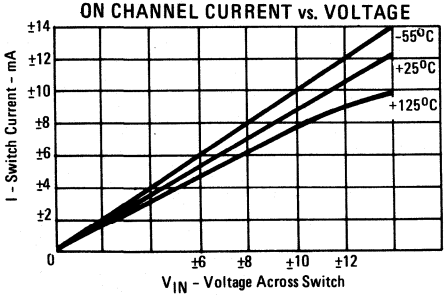


TEST CIRCUIT NO. 4

ANALOG INPUT OVERVOLTAGE CHARACTERISTICS

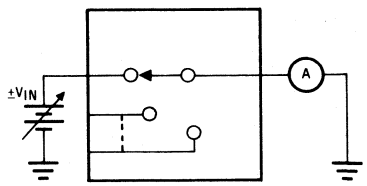


ON CHANNEL CURRENT vs. VOLTAGE

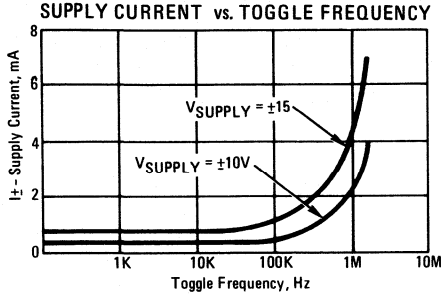


TEST CIRCUIT NO. 5

ON CHANNEL CURRENT vs. VOLTAGE

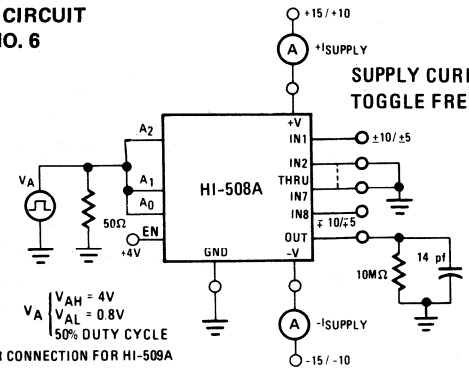


SUPPLY CURRENT vs. TOGGLE FREQUENCY



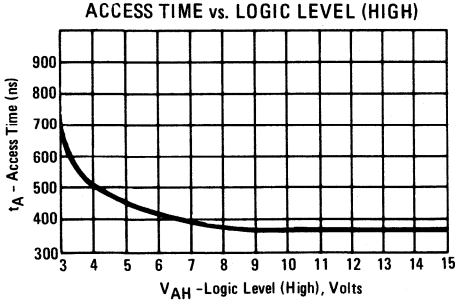
TEST CIRCUIT NO. 6

SUPPLY CURRENT vs. TOGGLE FREQUENCY



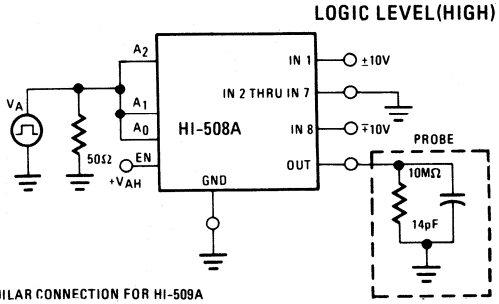
*SIMILAR CONNECTION FOR HI-509A

ACCESS TIME vs. LOGIC LEVEL (HIGH)



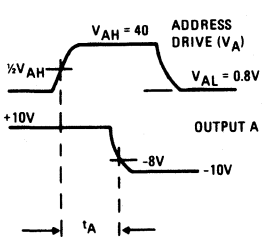
TEST CIRCUIT NO. 7

ACCESS TIME vs. LOGIC LEVEL(HIGH)

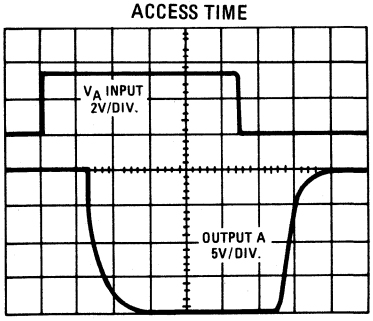


* SIMILAR CONNECTION FOR HI-509A

SWITCHING WAVEFORMS

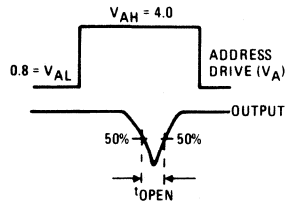


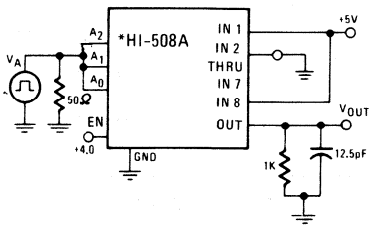
ACCESS TIME



SWITCHING WAVEFORMS (continued)

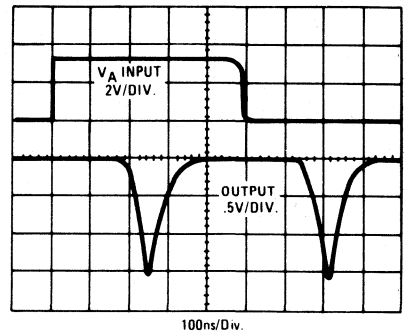
TEST CIRCUIT
NO. 8
BREAK BEFORE MAKE DELAY (t_{OPEN})



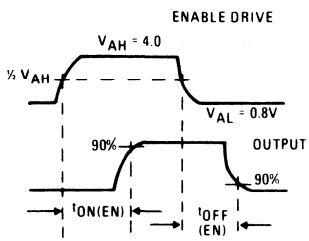


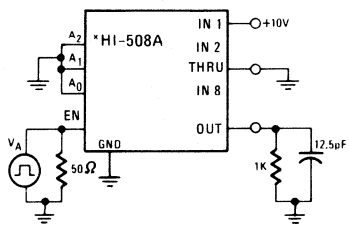
*SIMILAR CONNECTION FOR HI-509A

BREAK BEFORE MAKE DELAY (t_{OPEN})



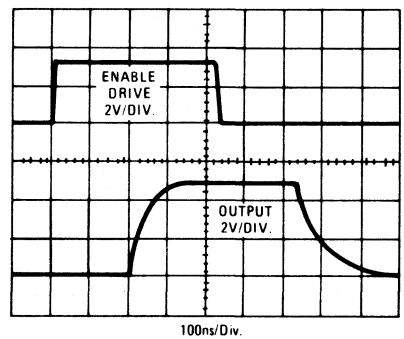
TEST CIRCUIT
NO. 9
ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)





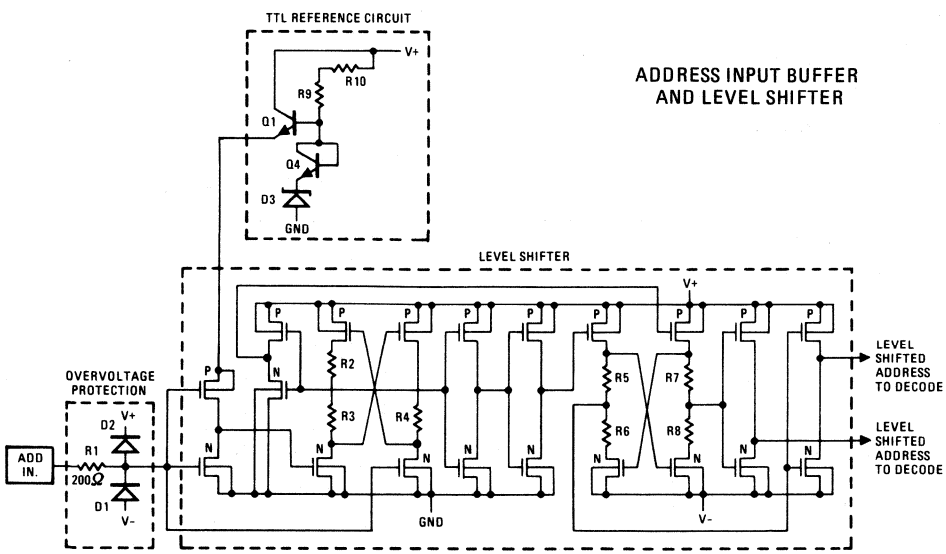
* SIMILAR CONNECTION FOR HI-509A

ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)

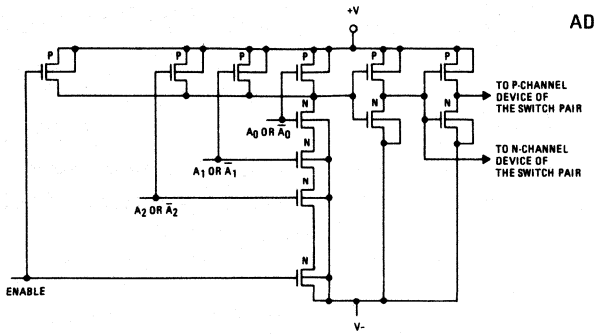


SCHEMATIC DIAGRAMS

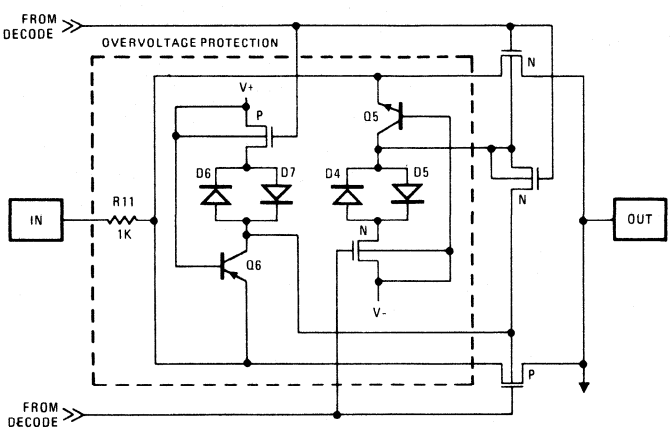
ADDRESS INPUT BUFFER
AND LEVEL SHIFTER



ADDRESS DECODER



MULTIPLEX SWITCH



3

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HI-516

16 Channel/Differential 8 Channel CMOS High Speed Analog Multiplexer

Preliminary

3

FEATURES

- ACCESS TIME (TYP) 100ns
- SETTLING TIME (TYP TO 0.01%) 800ns
- LOW LEAKAGE I_S OFF 10pA
  I_D OFF 35pA
- LOW CAPACITANCE C_S OFF 2.5pF
  C_D OFF 18pF
- HIGH OFF ISOLATION AT 1MHz 80dB
- LOW CHARGE INJECTION 0.3pC
- SINGLE ENDED TO DIFFERENTIAL SELECTABLE (SDS)
- LOGIC LEVEL SELECTABLE (LLS)

APPLICATIONS

- DATA ACQUISITION SYSTEMS
- PRECISION INSTRUMENTATION
- INDUSTRIAL CONTROL

DESCRIPTION

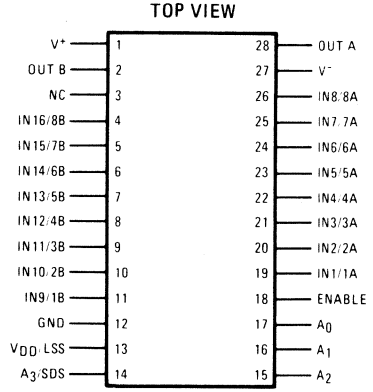
The HI-516 is a monolithic dielectrically isolated, high speed, high performance CMOS analog multiplexer. It offers unique built-in channel selection decoding plus an inhibit input for disabling all channels. The dual function of address input A_3 enables the HI-516 to be user programmed either as a single ended 16-channel multiplexer by connecting 'out A' to 'out B' and using A_3 as a digital address input, or as an 8-channel differential multiplexer by connecting A_3 to the V^- supply. The substrate leakages and parasitic capacitances are reduced substantially using the Harris dielectric isolation process to achieve ,optimum performances in both high and low level signal applications. The low output leakage current (I_D Off < 100pA @ 25°C) and fast settling (t_{SETTLE} = 800ns to 0.01%) characteristics of the device make it an ideal choice for high speed data acquisition systems, precision instrumentation, and industrial process controls.

The HI-516 is available in a 28 lead dual-in-line package. HI-516-5 is specified for operation over 0°C to +75°C, and the HI-516-2 over -55°C to +125°C. Processing to MIL-STD-883A, Class B screening is available by selecting the HI-516-8.

PINOUT

Package Code 1M

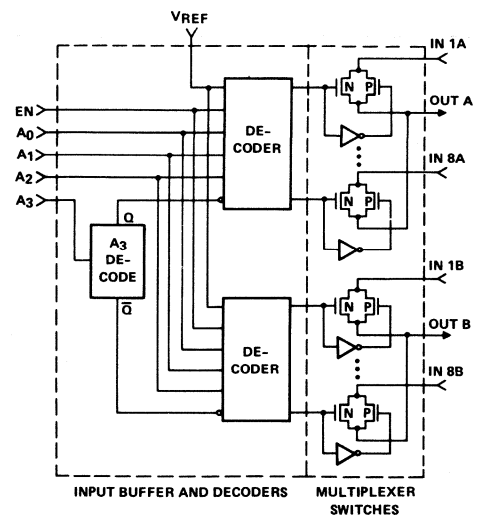
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on page 1-4.

FUNCTIONAL DIAGRAM

A_3 Decode		
A_3	Q	$\overline{Q}$
H	H	L
L	L	H
V^-	L	L



ABSOLUTE MAXIMUM RATINGS

Digital Input Overvoltage:

- TTL: $-6V < V_{AH} < +6V$
- TTL: A2 V_{SUPPLY} (-) -2V
- CMOS: V_{SUPPLY}(+) +2V
- CMOS: GND -2V

Analog Input Voltage:

- V_S: V_{SUPPLY}(+) +2V
- V_S: V_{SUPPLY}(-) -2V

Voltage Between Supply Pins	33V
Total Power Dissipation*	1200mW
Operating Temperature Ranges:	
HI-516-2	-55°C to +125°C
HI-516-5	0°C to 75°C
Storage Temperature Range	-65°C to 150°C
*Derate 8mW/°C above t_A	75°C

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified) Supplies = +15V, -15V; V_{AH} (Logic Level High) = +2.4V, V_{AL} (Logic Level Low) = +0.8V; V_{DD}/LLS = Open (Note 6)

PARAMETER	TEMP	-55°C to +125°C MIN	TYP	MAX	0°C to +75°C MIN	TYP	MAX	UNITS
ANALOG CHANNEL CHARACTERISTICS								
V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
R_{ON}, On Resistance (Note 1)	+25°C		620	750		620	750	Ω
	Full		770	1,000		700	1,000	Ω
I_S (OFF), Off Input Leakage Current	+25°C		0.01			0.01		nA
	Full		0.38	50		0.38	50	nA
I_D(OFF), Off Output Leakage Current	+25°C		0.035			0.035		nA
	Full		0.48	100		0.48	100	nA
I_D(ON), On Channel Leakage Current	+25°C		0.04			0.04		nA
	Full		0.56	100		0.56	100	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL} Input Low Threshold (TTL)	Full			0.8			0.8	V
V_{AH} Input High Threshold (TTL)	Full	2.4			2.4			V
V_{AH} Input Low Threshold (CMOS)	Full			$0.3V_{DD}$			$0.3V_{DD}$	V
V_{AH} Input High Threshold (CMOS)	Full	$0.7V_{DD}$			$0.7V_{DD}$			V
I_{AH} Input Leakage Current (High)	Full		0.05	1		0.05	1	μA
I_{AL} Current (Low)	Full		4	25		4	25	μA
SWITCHING CHARACTERISTICS								
t_A, Access Time	+25°C		100	150		100	150	ns
	Full		120	200		120	200	ns
t_{OPEN}, Break before make delay	+25°C		20			20		ns
t_{ON}(EN), Enable Delay (IN)	+25°C		100	150		100		ns
t_{OFF}(EN), Enable Delay (OFF)	+25°C		80	125		80		ns
Settling Time (0.1%)	+25°C		250			250		ns
(0.01%)	+25°C		800			800		ns
Charge Injection (Note 2)	+25°C		0.33			0.33		pC
Off Isolation (Note 3)	+25°C		90			90		dB
C_S(OFF), Channel Input Capacitance	+25°C		2.5			2.5		pF
C_D(OFF), Channel Output Capacitance	+25°C		18			18		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
C_{DS}(OFF), Input to Output Capacitance	+25°C		0.02			0.02		pF
POWER REQUIREMENTS								
PD, Power Dissipation	Full		525			525		mW
I^+, Current (Note 4)	Full		17.5	25		17.5	30	mA
I^-, Current (Note 4)	Full		17.5	25		17.5	30	mA
I^+, Standby (Note 5)	Full		17.0	25		17.0	30	mA
I^-, Standby (Note 5)	Full		17.0	25		17.0	30	mA

NOTES:

1. $V_{IN} = \pm 10V$, $I_{OUT} = -100$ A
2. $V_{IN} = 0V$, $C_L = 100pF$, Enable input pulse = 3V, f = 500kHz
3. $V_{EN} = 0.8V$, $V_S = 3V_{RMS}$, f = 500kHz, $C_L = 40pF$, $R_L = 1k$, Pin 3 grounded
4. $V_{EN} = +2.4V$
5. $V_{EN} = 0.8V$
6. V_{DD}/LLS Pin = Open or Grounded for TTL Compatibility
   V_{DD}/LLS Pin = V_{DD} for CMOS Compatibility

HI-516 USED AS A 16-CHANNEL MULTIPLEXER OR 8 CHANNEL DIFFERENTIAL MULTIPLEXER *

USE A_3 AS DIGITAL ADDRESS INPUT					ON CHANNEL TO	
ENABLE	A_3	A_2	A_1	A_0	OUT A	OUT B
L	X	X	X	X	NONE	NONE
H	L	L	L	L	1A	NONE
H	L	L	L	H	2A	NONE
H	L	L	H	L	3A	NONE
H	L	L	H	H	4A	NONE
H	L	H	L	L	5A	NONE
H	L	H	L	H	6A	NONE
H	L	H	H	L	7A	NONE
H	L	H	H	H	8A	NONE
H	H	L	L	L	NONE	1B
H	H	L	L	H	NONE	2B
H	H	L	H	L	NONE	3B
H	H	L	H	H	NONE	4B
H	H	H	L	L	NONE	5B
H	H	H	L	H	NONE	6B
H	H	H	H	L	NONE	7B
H	H	H	H	H	NONE	8B

* For 16-Channel single-ended function, tie 'out A' to 'out B', for dual 8-channel function use the A_3 address pin to select between MUX A and MUX B, where MUX A is selected with A_3 low.

HI-516 USED AS A DIFFERENTIAL 8-CHANNEL MULTIPLEXER

A_3 CONNECT TO V^- SUPPLY				ON CHANNEL TO	
ENABLE	A_2	A_1	A_0	OUT A	OUT B
L	X	X	X	NONE	NONE
H	L	L	L	1A	1B
H	L	L	H	2A	2B
H	L	H	L	3A	3B
H	L	H	H	4A	4B
H	H	L	L	5A	5B
H	H	L	H	6A	6B
H	H	H	L	7A	7B
H	H	H	H	8A	8B

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HI-518

8 Channel/Differential 4 Channel CMOS High Speed Analog Multiplexer

Preliminary

FEATURES

- ACCESS TIME (TYP) 80ns
- SETTLING TIME (0.1%) 250ns
- LOW LEAKAGE I_S (OFF) 50pA
  I_D (OFF) 100pA
- LOW CAPACITANCE (TYP) C_S (OFF) 2pF
  C_D (OFF) 10pF
- HIGH OFF ISOLATION @ (1MHz) 75dB
- SINGLE ENDED TO DIFFERENTIAL MODE SELECTABLE (SDS)
- LOGIC LEVEL SELECTABLE (LLS)
- LOW CHARGE INJECTION 0.3pC

APPLICATIONS

- DATA ACQUISITIONS SYSTEMS
- INDUSTRIAL CONTROLS
- TELEMETRY

DESCRIPTION

The HI-518 is a monolithic, high performance, high speed Analog Multiplexer, constructed utilizing the Harris Dielectrically isolated CMOS process.

This device has the added feature that it can be user programmed either as a single ended 8-channel multiplexer by connecting 'out A' to 'out B' and using A2 as a digital address input, or as a 4-channel differential multiplexer by connecting A2 to the V^- supply.

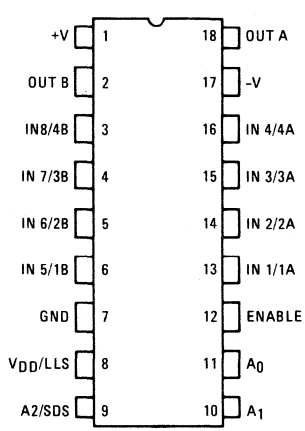
TTL or CMOS compatibility is also selectable. Low leakage current, I_D off < 100pA @ 25°C, and fast settling, 250ns to 0.1%, charateristics of this device make it an ideal choice for high speed data acquisition systems, precision instrumentation and industrial process controls.

The HI-518 is available in an 18 lead Dual-in-Line Package. The HI-518-5 is specified for operation over 0°C to +75°C, and the HI-518-2 over -55°C to +125°C. Processing to MIL-STD-883A Class B screening is available by selecting the HI-518-8.

PINOUT

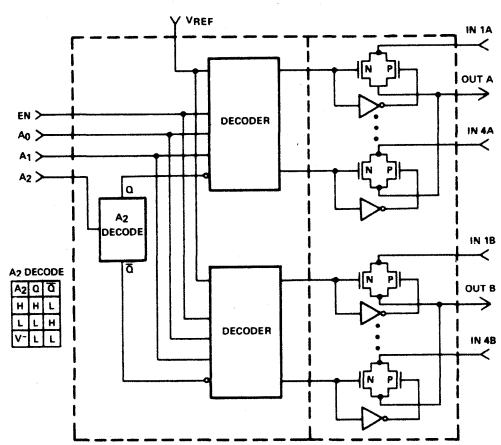
Package Code 4N

TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on page 1-4.

FUNCTIONAL DIAGRAM



3

ABSOLUTE MAXIMUM RATINGS

Digital Input Overvoltage:

TTL	$-6V < V_{AH} < +6V$	
	A2 V_{SUPPLY} (-)	-2V
CMOS	V_{SUPPLY}(+)	+2V
	GND	-2V

Analog Input Voltage:

V_S	V_{SUPPLY}(+)	+2V
	V_{SUPPLY}(-)	-2V

Voltage Between Supply Pins	33V
Total Power Dissipation*	725mW
Operating Temperature Ranges:	
HI-518-2	-55°C to +125°C
HI-518-5	0°C to 75°C
Storage Temperature Range	-65°C to 150°C
*Derate 8mW/°C above t_A	75°C

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified) Supplies = +15V, -15V; V_{AH} (Logic Level High) = +2.4V, V_{AL} (Logic Level Low) = +0.8V; V_{DD}/LLS = Open (Note 6).

PARAMETER	TEMP	-55°C to +125°C			0°C to +75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG CHANNEL CHARACTERISTICS								
V_S Analog Signal Range	Full	-15		+15	-15		+15	V
R_{ON} On Resistance (Note 1)	+25°C		480	750		480	750	Ω
	Full		700	1000		700	1000	Ω
I_S (OFF) Off Input	+25°C		0.05			0.05		nA
Leakage Current	Full		0.60	50		0.60	50	nA
I_D (OFF) Off Output	+25°C		0.10			0.10		nA
Leakage Current	Full		0.30	50		0.30	50	nA
I_D (ON) On Channel	+25°C		0.10			0.10		nA
Leakage Current	Full		0.30	50		0.30	50	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL} Input Low Threshold (TTL)	Full			0.8			0.8	V
V_{AH} Input High Threshold (TTL)	Full	2.4			2.4			V
V_{AL} Input Low Threshold (CMOS)	Full			$0.3V_{DD}$			$0.3V_{DD}$	V
V_{AH} Input High Threshold (CMOS)	Full	$0.7V_{DD}$			$0.7V_{DD}$			V
I_{AH} Input Leakage Current (High)	Full		0.05	1		0.05	1	μA
I_{AH} Input Leakage Current (Low)	Full		4	20		4	20	μA
SWITCHING CHARACTERISTICS								
t_A, Access Time	+25°C		80	125		80	125	
	Full		110	150		110	150	ns
t_{OPEN}, Break before make Delay	+25°C		20			20		ns
t_{ON} (EN), Enable Delay (ON)	+25°C		80	150		80	150	ns
t_{OFF} (EN), Enable Delay (OFF)	+25°C		60	125		60	125	ns
Settling Time (0.1%)	+25°C		250			250		ns
(0.01%)	+25°C		800			800		
Charge Injection (Note 2)	+25°C		0.3			0.3		pC
Off Isolation (Note 3)	+25°C		86			86		dB
C_S (OFF) Channel Input Capacitance	+25°C		1.9			1.9		pF
C_D (OFF) Channel Output Capacitance	+25°C		10			10		pF
C_A, Digital Input Capacitance	+25°C		3			3		pF
CDS (OFF) Input to Output Capacitance	+25°C		0.02			0.02		pF
POWER REQUIREMENTS								
P_D, Power Dissipation	Full		360	450		360	540	mW
I+, Current (Note 4)	Full		12	15		12	18	mA
I⁻, Current (Note 4)	Full		12	15		12	18	mA
I+, Standby (Note 5)	Full		11.5	15		11.5	18	mA
I⁻, Standby (Note 5)	Full		11.5	15		11.5	18	mA

NOTES:

1. $V_{IN} = \pm 10V$, $I_{OUT} = -100\mu A$
2. $V_{IN} = 0V$, $C_L = 100pF$, Enable Input pulse = 3V, f = 500kHz.
3. $V_{EN} = 0.8V$, $V_S = 3VMS$, f = 500kHz, $C_L = 40pF$, $R_L = 1k$. Due to the pin to pin capacitance between IN 8/4B (Pin 3) and Out B (Pin 2) channel 8/4B exhibits 60dB of Off Isolation under the above test conditions.
4. $V_{EN} = +2.4V$.
5. $V_{EN} = 0.8V$.
6. V_{DD}/LLS Pin = Open or grounded for TTL compatibility. V_{DD}/LLS Pin = V_{DD} for CMOS compatibility.

HI-518 USED AS 8 CHANNEL MULTIPLEXER OR
4 CHANNEL DIFFERENTIAL MULTIPLEXER

USE A_2 AS DIGITAL ADDRESS INPUT				ON CHANNEL TO	
ENABLE	A_2	A_1	A_0	OUT A	OUT B
L	X	X	X	NONE	NONE
H	L	L	L	1A	NONE
H	L	L	H	2A	NONE
H	L	H	L	3A	NONE
H	L	H	H	4A	NONE
H	H	L	L	NONE	1B
H	H	L	H	NONE	2B
H	H	H	L	NONE	3B
H	H	H	H	NONE	4B

HI-518 USED AS DIFFERENTIAL
4 CHANNEL MULTIPLEXER

A_2 CONNECT TO V^- SUPPLY			ON CHANNEL TO	
ENABLE	A_1	A_0	OUT A	OUT B
L	X	X	NONE	NONE
H	L	L	1A	1B
H	L	H	2A	2B
H	H	L	3A	3B
H	H	H	4A	4B

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
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HI-1818A/1828A

Low Resistance 8 Channel CMOS Analog Multiplexers

3

FEATURES

- SIGNAL RANGE ±15V
- "ON" RESISTANCE (TYP.) 250Ω
- INPUT LEAKAGE AT +125°C (TYP.) 20nA
- ACCESS TIME (TYP.) 350ns
- POWER CONSUMPTION (TYP.) 5mW
- DTL/TTL COMPATIBLE ADDRESS
- -55°C to +125°C OPERATION

APPLICATIONS

- DATA ACQUISITION SYSTEMS
- PRECISION INSTRUMENTATION
- DEMULTIPLEXING
- SELECTOR SWITCH

DESCRIPTION

The HI-1818A/1828A are monolithic high performance CMOS analog multiplexers offering built-in channel selection decoding plus an inhibit (enable) input for disabling all channels. Dielectric Isolation (DI) processing is used for enhanced reliability and performance (see Application Note 521). Substrate leakage and parasitic capacitance are much lower, resulting in extremely low static errors and high throughput rates. Low output leakage (typically 0.1nA) and low channel ON resistance (250 Ω) assure optimum performance in low level or current mode applications.

The 1818A is a single-ended 8 channel multiplexer, while the HI-1828A is a differential 4 channel version. Either device is ideally suited for medical instrumentation, telemetry systems, and microprocessor based data acquisition systems.

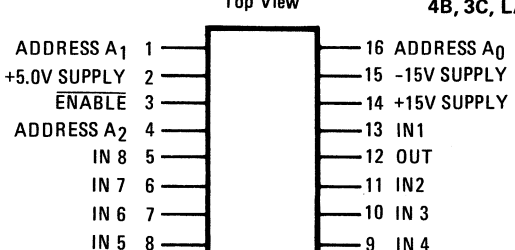
The HI-1818A-2 and HI-1828A are specified over -55°C to +125°C, while the -5 versions are specified over 0°C to +75°C.

PINOUT

HI-1818A

Top View

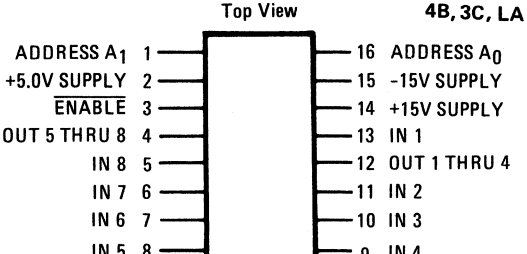
Package Code 4B, 3C, LA



HI-1828A

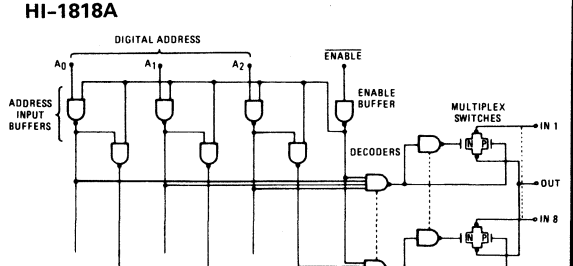
Top View

Package Code 4B, 3C, LA

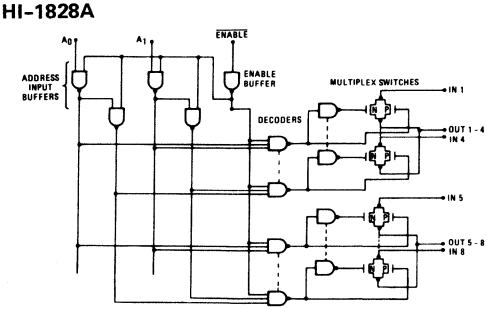


FUNCTIONAL DIAGRAM

HI-1818A



HI-1828A



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

ABSOLUTE MAXIMUM RATINGS (NOTE 1)

Supply Voltage Between Pins 14 and 15	40.0V	Digital Input Voltage	V-Supply to V+ Supply
Logic Supply Voltage, Pin 2	30.0V	Total Power Dissipation (Note 2)	780mW
Analog Input Voltage: V^+_{Supply} +2V		Storage Temperature Range	-65°C to +150°C
V^-_{Supply} -2V			

ELECTRICAL CHARACTERISTICS

Supplies = +15V, -15V, +5V

PARAMETER	TEMP.	HI-1818A-2/1828A-2 -55°C to +125°C MIN.	TYP.	MAX.	HI-1818A-5/1828A-5 0°C to +75°C MIN.	TYP.	MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS								
*V_{IN}, Analog Signal Range	Full	-15		+15	-15		+15	V
*R_{ON}, ON Resistance (Note 3)	+25°C		250	400		250	400	Ω
	Full		300	500		300	500	Ω
*I_S(OFF), Input Leakage Current	Full		20	50		20	50	nA
*I_D(ON), On Channel Leakage Current								
(HI-1818A)	Full		100	250		100	250	nA
(HI-1828A)	Full		50	125		50	125	nA
*I_D(OFF) Output Leakage Current								
(HI-1818A)	Full		100	250		100	250	nA
(HI-1828A)	Full		50	125		50	125	nA
DIGITAL INPUT CHARACTERISTICS								
V_{IL}, Input Low Threshold	Full			0.4			0.4	V
V_{IH}, Input High Threshold (Note 4)	Full	4.0			4.0			V
*I_{IN}, Input Leakage Current	Full		.01	1		.01	1	μA
SWITCHING CHARACTERISTICS								
T_S, Access Time (Note 5)	+25°C		350			350		ns
Break-Before-Make Delay	+25°C		100			100		ns
Settling Time (0.1%)	+25°C		1.08			1.08		μs
(0.025%)	+25°C		2.8			2.8		μs
C_{IN}, Channel Input Capacitance	+25°C		4			4		pF
C_{OUT}, Channel Output Capacitance								
(HI-1818A)	+25°C		20			20		pF
(HI-1828A)	+25°C		10			10		pF
C_{DS}(OFF), Drain-To-Source Capacitance	+25°C		0.6			0.6		pF
C_D, Digital Input Capacitance	+25°C		5			5		pF
POWER REQUIREMENTS								
P_D, Power Dissipation	Full		5			5		mW
P_{DS}, Standby Power (Note 6)	Full		5			5		mW
*I_+, Current Pin 14	Full		0.1	0.5		0.1	1	mA
*I_-, Current Pin 15	Full		0.3	1		0.3	2	mA
*I_L, Current Pin 2	Full		0.3	1		0.3	2	mA

NOTES:
1. Voltage ratings apply when voltages at all other pins are within their normal operating ranges.
2. Derate 9.25 mW/°C above 75°C.
3. V_{OUT} = ± 10V I_{OUT} = - 1mA.
4. To drive from DTL/TTL circuits, 1K pull-up resistors to + 5.0V supply are recommended.
5. Time measured to 90% of final output level; V_{OUT} = - 5.0V to +5.0V, Digital Inputs = 0V to + 4.0V.
6. Voltage at Pin 3, $\overline{ENABLE}$ = + 4.0V.

* 100% Tested for Dash 8 at +25°C and +125°C Only.

TRUTH TABLES

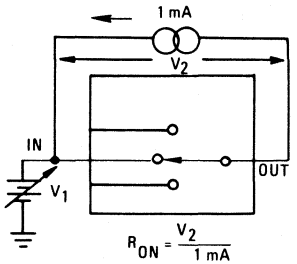
HI-1818A

ADDRESS A_2	A_1	A_0	$\overline{EN}$	"ON" CHANNEL
L	L	L	L	1
L	L	H	L	2
L	H	L	L	3
L	H	H	L	4
H	L	L	L	5
H	L	H	L	6
H	H	L	L	7
H	H	H	L	8
X	X	X	H	NONE

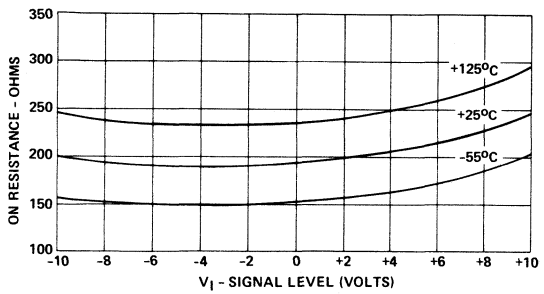
HI-1828A

ADDRESS A_1	A_0	$\overline{EN}$	"ON" CHANNELS
L	L	L	1 and 5
L	H	L	2 and 6
H	L	L	3 and 7
H	H	L	4 and 8
X	X	H	NONE

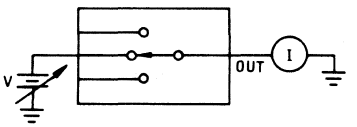
ON RESISTANCE vs ANALOG SIGNAL LEVEL



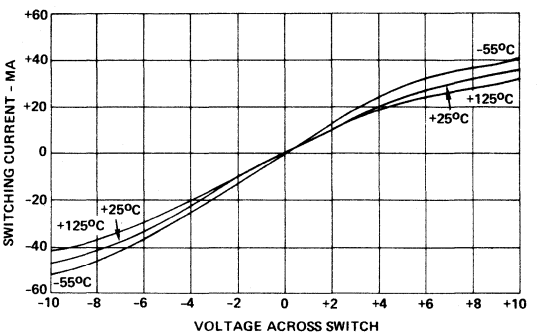
Test Circuit



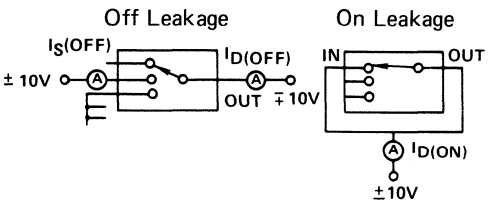
ON CHANNEL CURRENT vs VOLTAGE

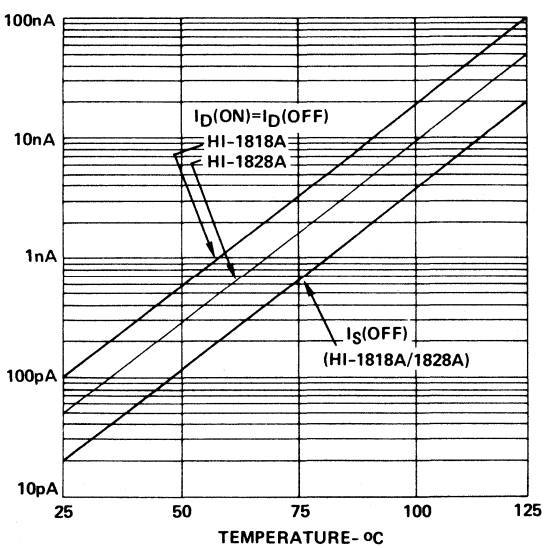


Test Circuit

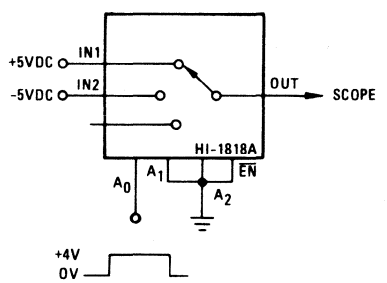


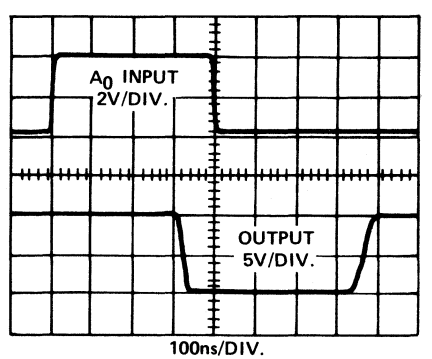
ON/OFF LEAKAGE CURRENTS vs TEMPERATURE



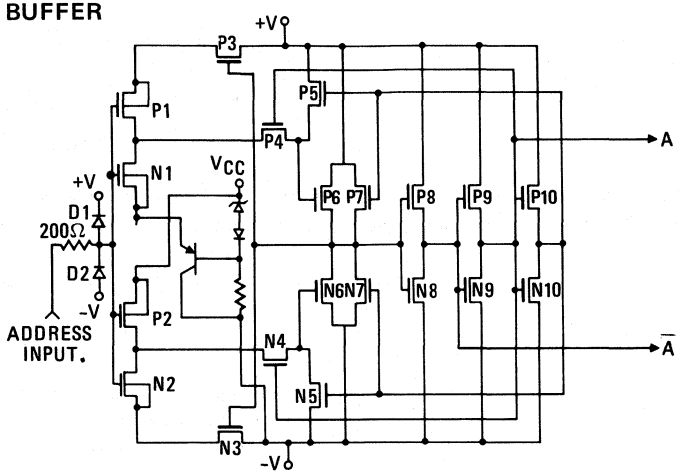


ACCESS TIME





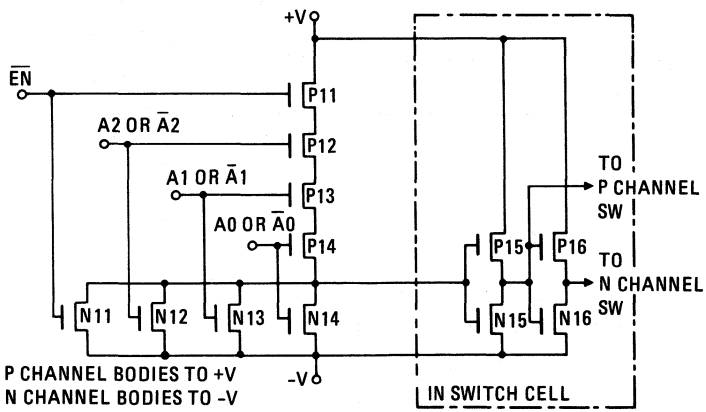
ADDRESS INPUT BUFFER



ALL N-CHANNEL BODIES TO V-

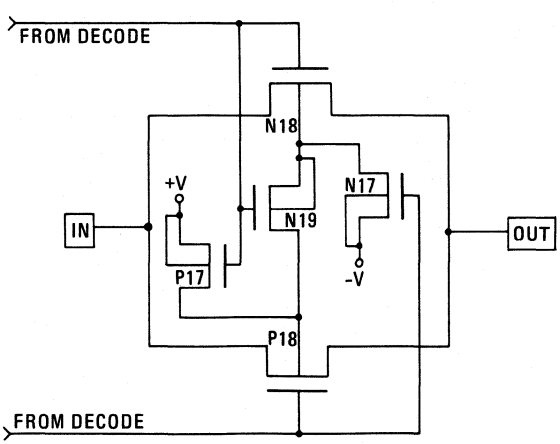
ALL P-CHANNEL BODIES TO V+ UNLESS OTHERWISE INDICATED.

DECODER GATE



A2 OR Ā2 NOT USED FOR HI-1828A

MULTIPLEX SWITCH



3

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HI-1840

16 Channel CMOS Analog Multiplexer with High-Z Analog Input Protection

3

FEATURES

- HIGH ANALOG INPUT IMPEDANCE DURING POWER LOSS (OPEN) 500MΩ
- LOW POWER CONSUMPTION (STANDBY) 600μW
- ACCESS TIME 500ns
- EXCELLENT IN HI-REL REDUNDANT SYSTEMS
- BREAK-BEFORE-MAKE SWITCHING
- NO LATCH-UP

APPLICATIONS

- FAIL-SAFE DATA ACQUISITION SYSTEMS
- FAIL-SAFE TELEMETRY SYSTEMS
- AIRCRAFT INSTRUMENTATION AND CONTROL

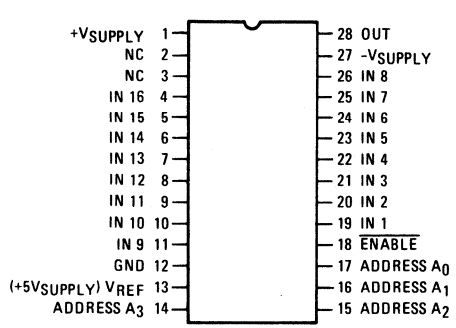
DESCRIPTION

The HI-1840 is a monolithic 16 channel multiplexer constructed with the Harris Linear Dielectric Isolation CMOS process. It is designed to provide a high input impedance to the analog source if device power fails (open) or the analog signal voltage inadvertently exceeds the supply rails during powered operation. Excellent for use in redundant applications, since the secondary device can be operated in a standby unpowered mode affording no additional power drain. But more significantly, a very high impedance exists between the active and inactive devices preventing any interaction. One of sixteen channel selection is controlled by a 4-bit binary address plus an Enable-Inhibit input which conveniently controls the ON/OFF operation of several multiplexers in a system. All digital inputs have electrostatic discharge protection. The HI-1840 is tested and guaranteed within the military temperature range and is available in a 28 pin dual-in-line package.

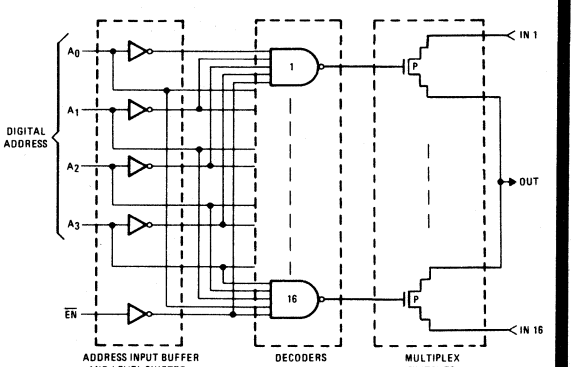
PINOUT

Package Code 1M

TOP VIEW



FUNCTIONAL DIAGRAM



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Between Pins 1 and 27 +40V
V_{REF} to Ground +20V
V_{EN}, V_A, Digital Input Overvoltage:
V_A V_{Supply} (+) +4V
V_{Supply} (-) -4V
Analog Input Overvoltage:
V_S V_{Supply} (+) +10V
V_{Supply} (-) -10V

Total Power Dissipation* 1200mW
Operating Temperature:
HI-1840-2 -55°C to +125°C
Storage Temperature -65°C to +150°C

*Derate 8mW/°C above T_A = +25°C

ELECTRICAL CHARACTERISTICS

Unless Otherwise Specified:
Supplies = +15V, -15V: V_{REF}(Pin 13) = +5V; V_{AH}(Logic Level High) = 4.0V; V_{AL}(Logic Level Low) = +0.8V
For Test Conditions, consult Performance Characteristics section.

PARAMETER	TEMP.	-55°C to +125°C MIN.	TYP.	MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS					
*V_S, Analog Signal Range	Full	-5		+15	V
*R_{ON}, On Resistance (Note 1) V_{IN} = +15V	Full		0.5	1.0	KΩ
V_{IN} = -5V	Full		2.5	5.0	KΩ
*I_S(OFF), Off Input Leakage Current	+25°C		0.03		nA
	Full			±100	nA
*I_S(OFF), with Power Off (Note 8)	Full			±100	nA
*I_D(OFF), Off Output Leakage Current	+25°C		1.0		nA
	Full			±1000	nA
* I_D(OFF), or I_S(OFF) with Input Overvoltage Applied (Note 2)	+25°C		50		nA
	Full			±1000	nA
*I_D(ON), On Channel Leakage Current	+25°C		1.0		nA
	Full			±1000	nA
DIGITAL INPUT CHARACTERISTICS					
V_{AL}, Input Low Threshold | TTL Drive	Full			0.8	V
V_{AH}, Input High Threshold | (Note 7)	Full	4.0			V
V_{AL} | MOS Drive (Note 3)	+25°C			0.8	V
V_{AH} |	+25°C	6.0			V
*I_A, Input Leakage Current (High or Low)	Full			1.0	µA
SWITCHING CHARACTERISTICS					
t_A, Access Time	+25°C		500	1000	ns
t_{OPEN}, Break-Before-Make Delay	+25°C	20	80		ns
t_{ON}(EN), Enable Delay (ON)	+25°C		300	1000	ns
t_{OFF}(EN), Enable Delay (OFF)	+25°C		300	1000	ns
Settling Time (0.1%)	+25°C		1.2		µs
(0.025%)	+25°C		4.1		µs
"Off Isolation" (Note 4)	+25°C		65		dB
C_S(OFF), Channel Input Capacitance	+25°C		5		pF
C_D(OFF), Channel Output Capacitance :	+25°C		50		pF
C_A, Digital Input Capacitance	+25°C		5		pF
C_{DS}(OFF), Input ot Output Capacitance	+25°C		0.15		pF
POWER REQUIREMENTS					
P_D, Power Dissipation (Note 5)	+25°C		0.6	15.0	mW
(Note 6)	+25°C		0.6	15.0	mW
*I+, Current Pin 1 (Note 5)	Full		0.02	0.5	mA
*I-, Current Pin 27 (Note 5)	Full		0.02	0.5	mA
*I+, Standby (Note 6)	Full		0.02	0.5	mA
*I-, Standby (Note 6)	Full		0.02	0.5	mA

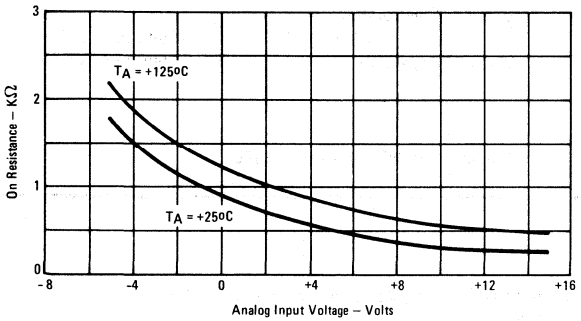
TRUTH TABLE

A_3	A_2	A_1	A_0	$\overline{EN}$	"ON" CHANNEL
X	X	X	X	H	NONE
L	L	L	L	L	1
L	L	L	H	L	2
L	L	H	L	L	3
L	L	H	H	L	4
L	H	L	L	L	5
L	H	L	H	L	6
L	H	H	L	L	7
L	H	H	H	L	8
H	L	L	L	L	9
H	L	L	H	L	10
H	L	H	L	L	11
H	L	H	H	L	12
H	H	L	L	L	13
H	H	L	H	L	14
H	H	H	L	L	15
H	H	H	H	L	16

NOTES:
1. I_{OUT} = 1mA
2. Analog Overvoltage = ±20V
3. V_{REF} = +10V
4. V_{EN} = 4.0V, R_L = 1K, C_L = 7pF, V_S = 3VRMS, f = 500kHz
5. V_{EN} = 0.8V
6. V_{EN} = 4.0V
7. To drive from DTL/TTL circuits 1K pull-up resistors to +5.0V supply are recommended
8. All supplies (V+, V-, +5V) and digital inputs (A_0, A_1, A_2, A_3, EN) opened. Analog input ±10V.

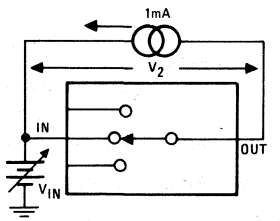
Unless Otherwise Specified: T_A = 25°C, V_{SUPPLY} = ±15V, V_{AH} = +4V, V_{AL} = 0.8V and V_{REF} = 5V.

ON RESISTANCE VS. ANALOG INPUT VOLTAGE

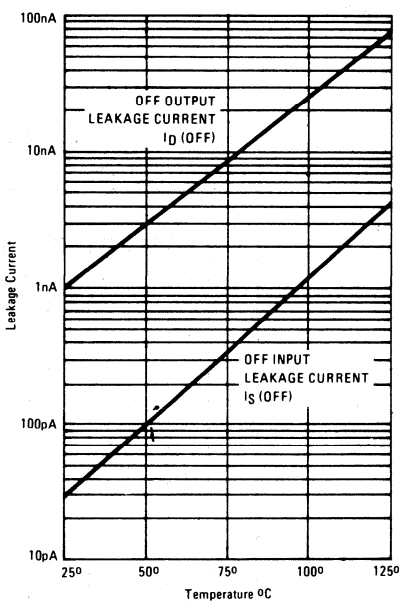


ON RESISTANCE vs. INPUT SIGNAL LEVEL

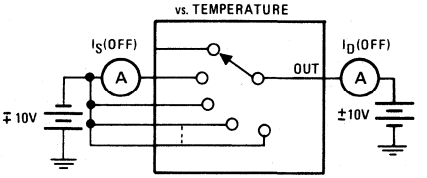
$R_{ON} = \frac{V_2}{1mA}$



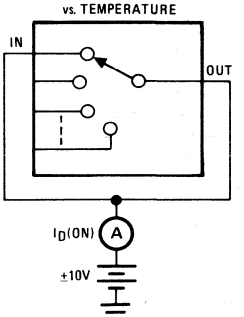
LEAKAGE CURRENT VS. TEMPERATURE



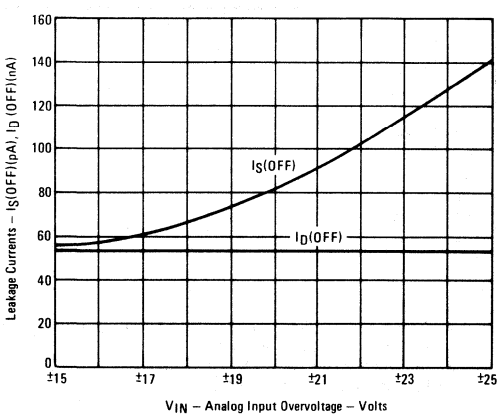
OFF LEAKAGE CURRENT vs. TEMPERATURE



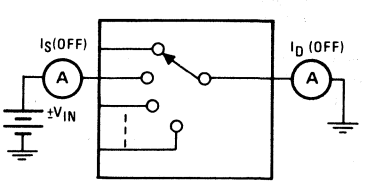
ON LEAKAGE CURRENT vs. TEMPERATURE



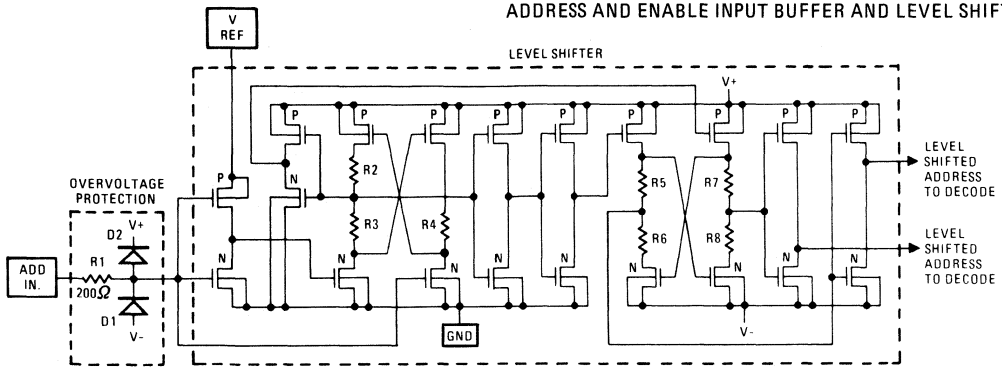
ANALOG INPUT OVERVOLTAGE CHARACTERISTICS



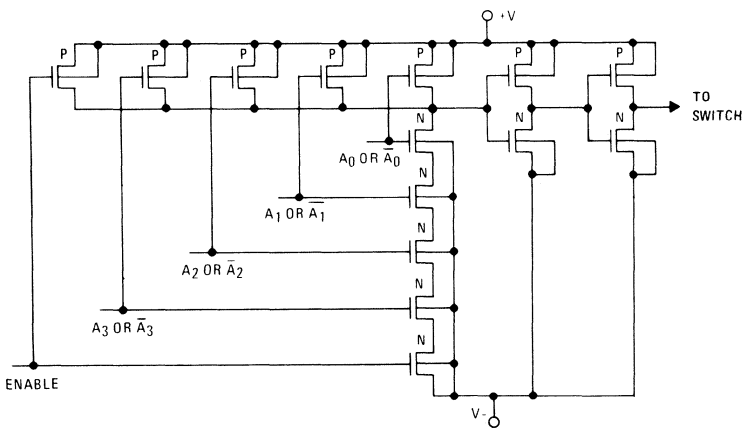
ANALOG INPUT OVERVOLTAGE CHARACTERISTICS



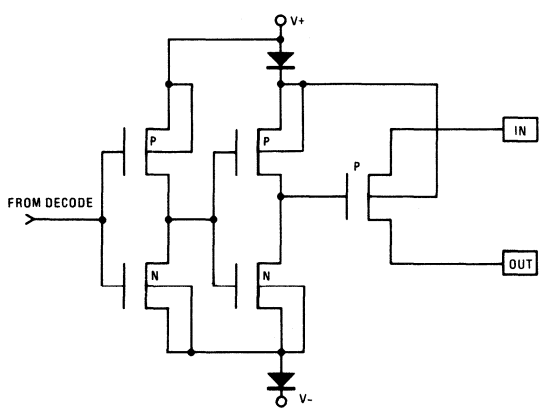
ADDRESS AND ENABLE INPUT BUFFER AND LEVEL SHIFTER



ADDRESS DECODER



MULTIPLEX SWITCH



Data Conversion Products & Voltage References

ABSOLUTE MAXIMUM RATINGS

As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Characteristics" are the only conditions recommended for satisfactory operation.

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HA-1600/02/05

+10V Precision Voltage Reference

FEATURES

- MONOLITHIC CONSTRUCTION
- EXCELLENT TEMPERATURE STABILITY
- LOW NOISE 100 μV_{RMS}
- WIDE INPUT RANGE 14 V TO 20V

APPLICATIONS

- EXTERNAL VOLTAGE REFERENCE FOR DATA CONVERTERS (D/A OR A/D)
- COMPARATOR REFERENCE
- VOLTAGE REGULATOR REFERENCE

DESCRIPTION

HA-1600/02/05 is a monolithic, temperature regulated, +10V precision voltage reference featuring load regulation accuracies to 1 LSB (12 Bit system) over its operating temperature range. This guaranteed accuracy specification is achieved by employing a high gain differential amplifier to sense and regulate the chip temperature.

To enhance accuracy and provide fast warm-up and minimum power drain these devices are thermally isolated from the package. Advanced laser trimming techniques are used to ensure a precision +10V output.

In operation, HA-1600/02/05 will accept an unregulated DC input voltage ranging from +14V to +20V and provide a low noise, extremely accurate +10V DC output at load currents up to 2mA. For higher output currents an external amplifier may be connected inside the feedback loop of HA-1600/02/05.

The outstanding accuracy of these voltage references make them ideal selections for applications requiring maximum precision and minimum drift, such as the external voltage reference for a 12 Bit D/A converter.

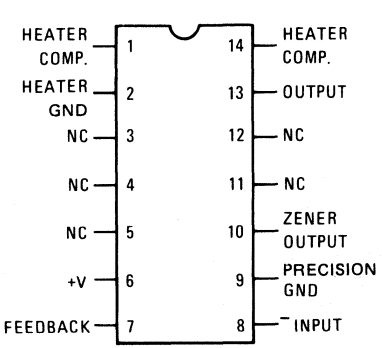
HA-1600/02/05 is packaged in a 14 pin DIP. HA-1600-2 is guaranteed to provide ± 1 LSB accuracy from -55°C to +125°C while the HA-1602-2 offers guaranteed accuracy to ± 2 LSB* over the military temperature range. HA-1605-5 is specified to maintain better than ± 1 LSB* accuracy from 0°C to +75°C.

* Relative to 12 Bit resolution 1 LSB equals one part in 4096 or 2.44mV for a +10V output.

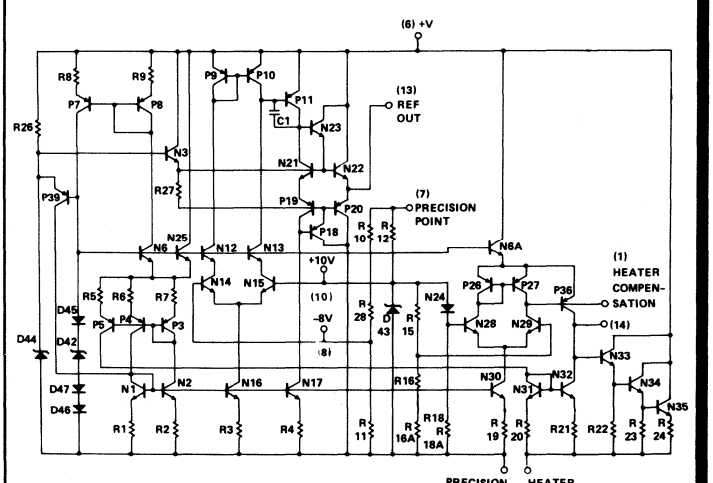
PINOUT

Package Code 4T

TOP VIEW



SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Referred to Ground - Note 1)

Storage Temp. Range	$-65^{o}C \leq T_A \leq +150^{o}C$	Operating Temperature Range:	
Input Voltage	35V	HA-1600-2	$-55^{o}C \leq T_A \leq +125^{o}C$
Power Dissipation	800mW	HA-1602-2	$-55^{o}C \leq T_A \leq +125^{o}C$
		HA-1605-5	$0^{o}C \leq T_A \leq 75^{o}C$

ELECTRICAL CHARACTERISTICS (Note 2,5) V_{IN} = +15V, I_L = 0mA, unless otherwise specified.

PARAMETER	TEMP	HA-1600-2 -55°C to +125°C			HA-1602-2 -55°C to +125°C			HA-1605-5 0°C to +75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
POWER INPUT CHARA.'S											
V_{IN}, Input Voltage Range	25°C	14	15	20	14	15	20	14	15	20	Volts
I_Q, Quiescent Current	-55°C		80	130		80	130				mA
	25°C		50	80		50	80	15	50	80	mA
	+125°C		10	20		10	20				mA
REGULATED OUTPUT CHARA.'S											
Output Voltage (V_O)	25°C	9.995	10.000	10.005	9.995	10.000	10.005	9.995	10.000	10.005	Volts
Output Load Current (I_L)	25°C	2			2			2			mA
Output Noise Voltage (E_N) (0.1Hz to 1MHz)			200			200			200		μV_{RMS}
Line Regulation V_{IN} = 14.5V to 17.5V	Full		0.001	0.002		0.001	0.002		0.001	0.002	%/V
Load Reg., R_L = Open to 5KΩ	Full		0.001	0.002		0.001	0.002		0.001	0.002	%/mA
Output Voltage Temperature Coefficient, R_L = Open	Full			±1.35			±2.7			±3.25	ppm/°C
Output Voltage Error, Total (Note 3)	Full			±1 LSB			±2 LSB			±1 LSB	
TURN-ON CHARACTERISTICS											
Turn-on Current	-55°C		120			120					mA
(Note 4)	+25°C		100			100			100		mA
	+125°C		20			20					mA
Warm-up Time	-55°C		180			180					sec
	+25°C		60			60			60		sec
	+125°C		30			30					sec

NOTES:

1. Absolute maximum ratings are limiting values beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. The specified electrical characteristics apply to suggested hook-up only. The 40Ω heater current limiter is mandatory.
3. Specifications relative to 12 bit accuracy.
4. The maximum current drawn from the input supply that is required to heat the chip to its operating temperature at the specified conditions.
5. Low leakage capacitors are strongly recommended for noise control and other functions. Leaky capacitors can contribute to both accuracy and TC errors.

DEFINITIONS

1. Output Noise Voltage: The peak-to-peak output noise voltage in a specified frequency band.

2. Quiescent Current, I_Q: The current required from the supply to operate the device at no load condition after the device is warmed up.

3. Output Voltage Temperature Coefficient, T_C: The ratio of the output voltage change with temperature to the specified temperature range expressed in ppm/°C; T_C (0°C to 75°C) = $(\Delta V_O/10V)/75^oC$.

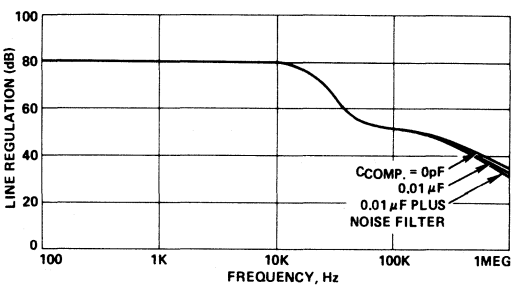
4. Line Regulation: The ratio of the change in output voltage to the change in line voltage producing it; line regulation (%/V) = $[(\Delta V_O/10V) \times 100]/\Delta V_{IN}$.

5. Load Regulation: The ratio of the change in output voltage to the change in load current producing it; load regulation (%/mA) = $[(\Delta V_O/10V) \times 100]/\Delta I_L$.

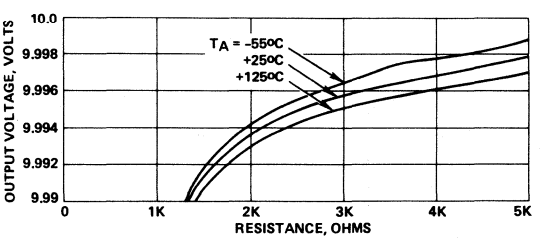
PERFORMANCE CURVES

V_{IN} = +15V, R_L = ∞, T_A = +25°C Unless otherwise specified.

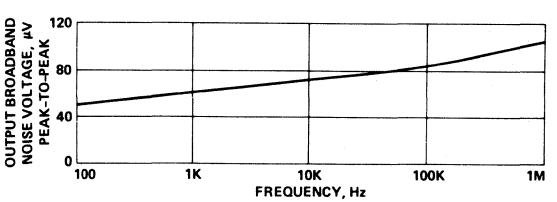
LINE REGULATION VS. FREQUENCY

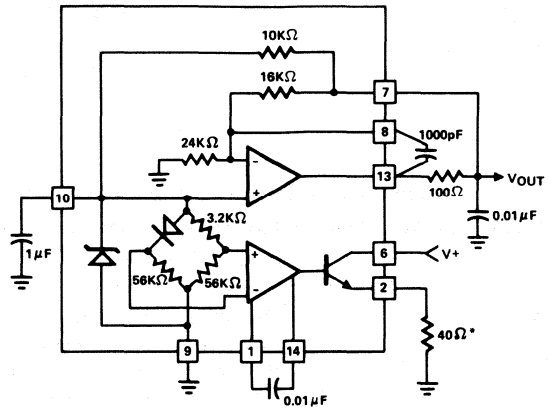


OUTPUT VOLTAGE VS. LOAD RESISTANCE



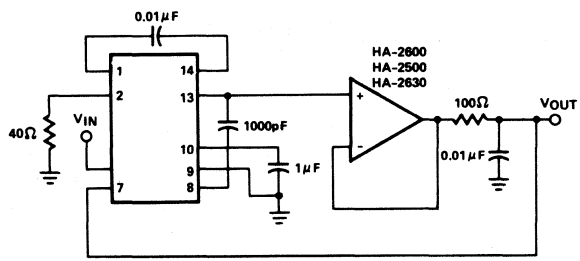
OUTPUT BROADBAND NOISE VOLTAGE VS. FREQUENCY ($C_{COMP.}$ = 0.01 µF)





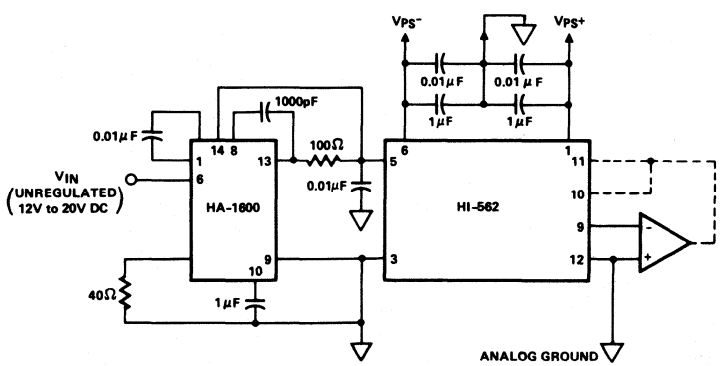
*Current limiting resistor - See note 2.

FUNCTIONAL DIAGRAM/SUGGESTED HOOK-UP



BOOSTING OUTPUT CURRENT

In this circuit an operational amplifier is tied in the feedback loop of HA-1600. Output current capability can be increased from 2mA to several hundred milliamps if required. The errors of the op amp are nullified by HA-1600.



12 BIT D/A CONVERTER USING HA-1600

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HA-1610/1615

+10V Precision Voltage Reference

FEATURES

- MONOLITHIC CONSTRUCTION
- INITIAL ACCURACY +10V ± 0.05%
- EXCELLENT TEMP. STABILITY ±3ppm/°C MAX
- LOW NOISE 100 μV_{RMS}
- WIDE INPUT RANGE 12V TO 30V
- OUTPUT SHORT CIRCUIT PROTECTION

4

APPLICATIONS

- EXTERNAL VOLTAGE REFERENCE FOR DATA CONVERTERS (D/A OR A/D)
- COMPARATOR REFERENCE
- VOLTAGE REGULATOR REFERENCE
- NEGATIVE 10 VOLT REFERENCE

DESCRIPTION

HA-1610/15 is a monolithic +10V precision voltage reference featuring excellent initial accuracy and temperature stability specifications. A reference zener and buffer amplifier hold HA-1610/15's voltage output constant under varying external conditions while an initial accuracy of 10V ± 0.05% and a guaranteed T_C as low as ± 3ppm/°C (Military Temperature Range) are provided by laser trimmed feedback and zener bias resistors.

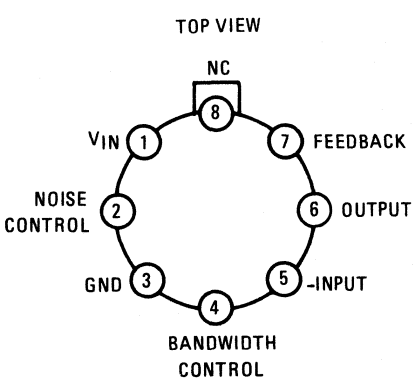
An accurate +10V DC output with 10mA typical load current capability is provided by HA-1610/15 when supplied with an unregulated DC input ranging from 12V to 30V. For higher current output, an external amplifier may be connected inside the feedback loop of HA-1610/15.

These devices are most useful as voltage references for 12 bit D/A or A/D converters where high precision and extreme stability are a necessity. High precision voltage output coupled with low power dissipation (30mW Typ.) makes HA-1610/15 ideal for precision comparator reference and reference stacking circuits. These references are also useful as -10V references.

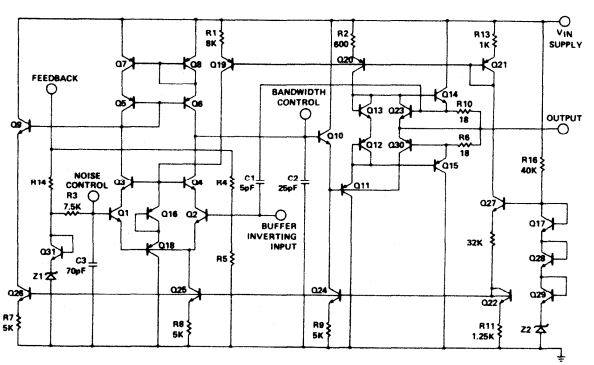
HA-1610/15 is packaged in an 8 pin metal can (TO-99). HA-1610-2 and HA-1615-2 are specified for -55°C to +125°C while HA-1515-5 operates from 0°C to +75°C.

PINOUT

HA-1610 Package Code 2A, 4Q, LA
HA-1615 Package Code 2A, 4Q



SCHEMATIC



ABSOLUTE MAXIMUM RATINGS Note 1.

Input Voltage	40V	Operating Temperature Range	
Output Short Circuit Duration	Indefinitely	HA-1610-2, HA-1615-2	-55°C to +125°C
Power Dissipation	400mW		
Storage Temperature Range	-65°C to +150°C	HA-1610-5, HA-1615-5	0°C to +75°C

ELECTRICAL CHARACTERISTICS (Note 2,3) (V_{IN} = +15V, I_L = 0mA, unless otherwise specified).

PARAMETER	TEMP	HA-1610-2, 1615-2 -55°C to +125°C MIN	TYP	MAX	HA-1610-5, 1615-5 0°C to +75°C MIN	TYP	MAX	UNITS
POWER INPUT CHARACTERISTICS								
Input Voltage Range, V_{IN}	Full	12	15	30	12	15	30	V
Quiescent Current, I_Q	25°C		1.9			1.9		mA
	Full			3.0			3.0	
REGULATED OUTPUT CHARA.'S								
Output Voltage, V_O	25°C	9.995	10.00	10.005	9.995	10.00	10.005	V
Output Load Current, I_L	Full	10			10			mA
Line Regulation (V_{IN} = 12V to 30V)	25°C		0.001			0.001		%/V
	Full			0.004			0.004	
Load Regulation (I_L = 0 to 10mA)	25°C		0.0015			0.0015		%/mA
	Full			0.004			0.004	
Output Voltage Tempco, I_L = 0mA								
(HA-1610)	Full			±3			±3	ppm/°C
(HA-1615)	Full			±5			±5	
Output Noise Voltage, EN (0.1Hz to 1MHz)	Full		200			200		μV_{RMS}
Dynamic Load Settling Time to ±0.1%	25°C		100			100		ns
to ±0.01%	25°C		400			400		
Warm-up Time (to ±0.01%)	25°C		1			1		sec
	Full		3			3		

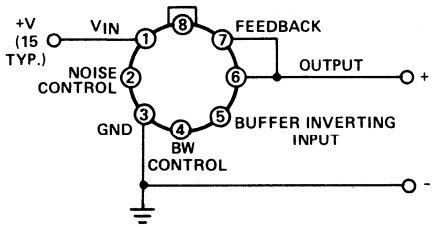
NOTES:

1. Absolute maximum ratings are limiting values beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. The specified electrical characteristics apply to suggested hook-up only.
3. Low leakage capacitors are strongly recommended for noise control and other functions. Leaky capacitors can contribute to both accuracy and TC errors.

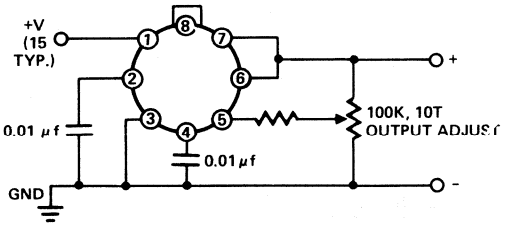
DEFINITIONS

1. Output Noise Voltage - the root mean square output noise voltage in a specified frequency band.
2. Quiescent Current, I_Q - the current required from the supply to operate the device at no load condition after the device is warmed-up.
3. Output Voltage Temperature Coefficient, T_C - the ratio of the output voltage change with temperature to the specified temperature range expressed in ppm/°C such as:
   $T_C(0°C \text{ to } 75°C) = (\Delta V_O/10V)/75°C \times 10^6$.
4. Line Regulation (%/V) - the ratio of the change in output voltage to the change in line voltage producing it; line regulation (%/V) = $[(\Delta V_O/10V) \times 100]/\Delta V_{IN}$.
5. Load Regulation (%/mA) - the ratio of the change in output voltage to the change in load current producing it; load regulation (%/mA) = $[(\Delta V_O/10V) \times 100]/\Delta$ mA.
6. Dynamic Load Settling Time - the time required for the output to settle to within the specified error band for a change in the load current of 1mA (without the bandwidth control capacitor).

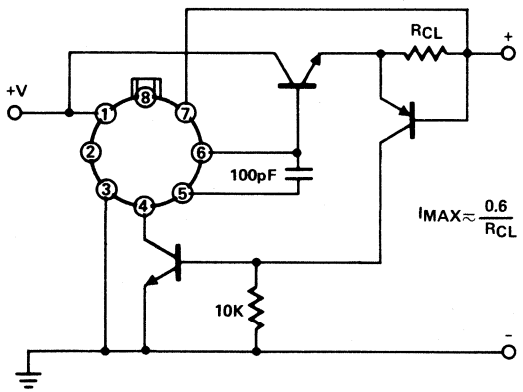
APPLICATIONS



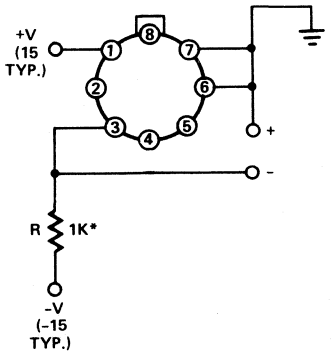
PIN FUNCTION/TYPICAL HOOK-UP



SUGGESTED HOOKUP FOR LOW NOISE AND OUTPUT TRIM



HIGH CURRENT OUTPUT WITH CURRENT LIMITING



NEGATIVE 10 VOLT REFERENCE

*Note: The value of R may reduce the output current available to less than that specified on the data sheet.

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HA-2420/2425

Fast Sample and Hold Gated Operational Amplifier

FEATURES

- SAMPLE CURRENT/HOLD RATIO — 10^6
- ACQUISITION TIME (0.01%) — 5μs
- SLEW RATE — 5V/μs
- BANDWIDTH — 2MHz
- APERTURE DELAY — 50ns
- LOW CHARGE TRANSFER — 10pC
- DTL/TTL COMPATIBLE CONTROL INPUT

APPLICATIONS

- A TO D INPUT (TO 13 BITS)
- D TO A DEGLITCHER
- AUTO ZERO SYSTEMS
- PEAK DETECTOR
- GATED OP AMP

DESCRIPTION

The HA-2420/2425 is a monolithic circuit consisting of a high performance operational amplifier with its output in series with an ultra-low leakage analog switch and a MOSFET input unity gain amplifier.

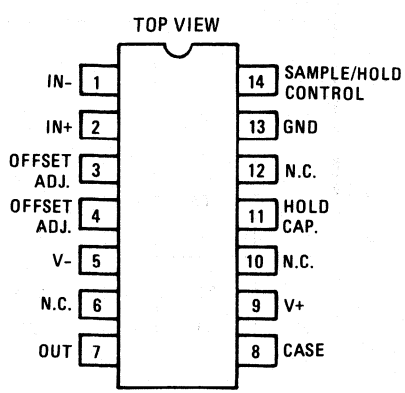
With an external holding capacitor connected to the switch output, a versatile, high performance sample-and-hold or track-and-hold circuit is formed. When the switch is closed, the device behaves as an operational amplifier, and any of the standard op amp feedback networks may be connected around the device to control gain, frequency response, etc. When the switch is opened the output will remain at its last level.

Performance as a sample-and-hold compares very favorably with other monolithic, hybrid, modular, and discrete circuits. Accuracy to better than 0.01% is achievable over the temperature range. Fast acquisition is coupled with superior droop characteristics, even at high temperatures. High slew rate, wide bandwidth, and low acquisition time produce excellent dynamic characteristics. The ability to operate at gains greater than 1 frequently eliminates the need for external scaling amplifiers.

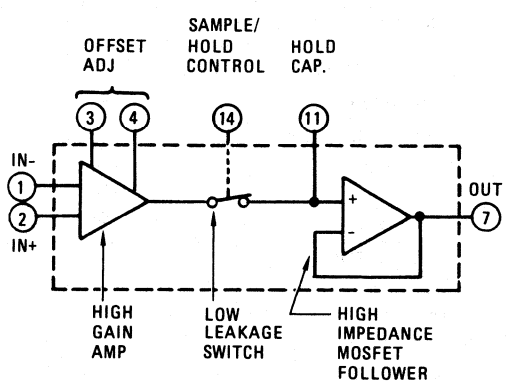
The device may also be used as a versatile operational amplifier with a gated output for applications such as analog switches, peak holding circuits, etc.

PINOUT

Package Code 4U, LA



FUNCTIONAL DIAGRAM



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	40V	Internal Power Dissipation	300mW (Note 7)
Differential Input Voltage	±30V	Operating Temperature Range	
Digital Input Voltage (Pin 14)	+8V, -15V	HA-2420-2/8	$-55^{o}C \leq T_A \leq +125^{o}C$
Output Current	Short Circuit Protected	HA-2425-5	$0^{o}C \leq T_A \leq +75^{o}C$
		Storage Temperature Range	$-65^{o}C \leq T_A \leq +150^{o}C$

ELECTRICAL CHARACTERISTICS

Test Conditions $V_{Supply} = \pm 15.0V$, $C_H = 1000pF$ Unless Otherwise Specified — Digital Input (Pin 14) $V_{IL} = +0.8V$ (Sample), $V_{IH} = +2.0V$ (Hold)

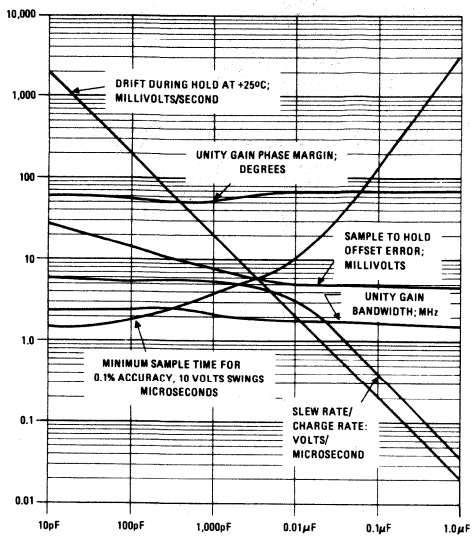
PARAMETER	TEMP.	HA-2420-2 MIN.	HA-2420-2 TYP.	HA-2420-2 MAX.	HA-2425-5 MIN.	HA-2425-5 TYP.	HA-2425-5 MAX.	UNITS
INPUT CHARACTERISTICS								
* Offset Voltage	+25°C		2	4		3	6	mV
	Full		3	6		4	8	mV
*Bias Current	+25°C		50	200		50	200	nA
	Full			400			400	nA
*Offset Current	+25°C		10	50		10	50	nA
	Full			100			100	nA
Input Resistance	+25°C	5	10		5	10		MΩ
Common Mode Range	Full	±10			±10			V
TRANSFER CHARACTERISTICS								
* Large Signal Voltage Gain (Note 1, 4)	Full	25K	50K		25K	50K		V/V
*Common Mode Rejection (Note 2)	Full	80	90		74	90		dB
Gain Bandwidth Product (Note 3)	+25°C		2			2		MHz
OUTPUT CHARACTERISTICS								
* Output Voltage Swing (Note 1)	Full	±10			±10			V
Output Current	+25°C	±10			±10			mA
Full Power Bandwidth (Note 3, 4)	+25°C		70			70		kHz
Output Resistance	+25°C		5			5		Ω
TRANSIENT RESPONSE								
Rise Time (Note 3, 5)	+25°C		100			100		ns
Overshoot (Note 3, 5)	+25°C		20			20		%
Slew Rate (Note 3, 6)	+25°C		5			5		V/μs
DIGITAL INPUT CHARACTERISTICS								
Digital Input Current (V_{IN} = 0V)	Full			0.8			0.8	mA
Digital Input Current (V_{IN} = +5.0V)	Full			20			20	μA
Digital Input Voltage (Low)	Full			0.8			0.8	V
Digital Input Voltage (High)	Full	2.0			2.0			V
SAMPLE/HOLD CHARACTERISTICS								
Acquisition Time to .1% 10V Step (3)	+25°C		4			4		μs
Acquisition Time to .01% 10V Step (3)	+25°C		5			5		μs
Aperture Delay	+25°C		50			50		ns
Aperture Uncertainty	+25°C		5			5		ns
* Drift Current	+25°C		5			5		pA
	Full		0.5	10		.05	1.0	nA
* Charge Transfer	+25°C		10	20		10	20	pC
POWER SUPPLY CHARACTERISTICS								
* Supply Current	+25°C		2.5	5.0		2.5	5.0	mA
* Power Supply Rejection Ratio	Full	80	90		74	90		dB

NOTES:
1. $R_L = 2K\Omega$
2. $V_{CM} = \pm 10VDC$
3. $A_V = +1$, $R_L = 2K\Omega$, $C_L = 50pF$
4. $V_{OUT} = 20V$ peak-to-peak
5. $V_{OUT} = 400mV$ peak-to-peak
6. $V_{OUT} = 10.0V$ peak-to-peak
7. Derate Power Dissipation by 4.3mW/°C above +105°C Ambient Temperature.

*100% Tested For DASH 8

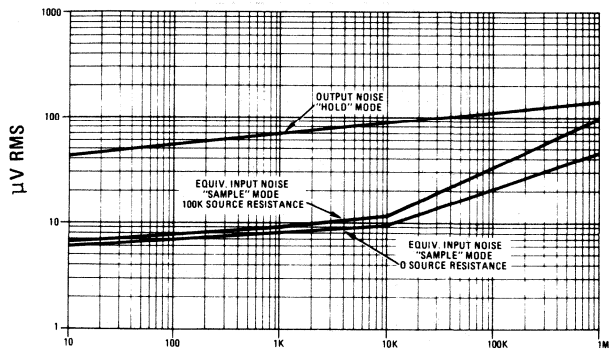
V_{SUPPLY} = ±15VDC, T_A = +25°C, C_H = 1,000pF UNLESS OTHERWISE SPECIFIED

TYPICAL SAMPLE-AND-HOLD PERFORMANCE AS A FUNCTION OF HOLDING CAPACITANCE



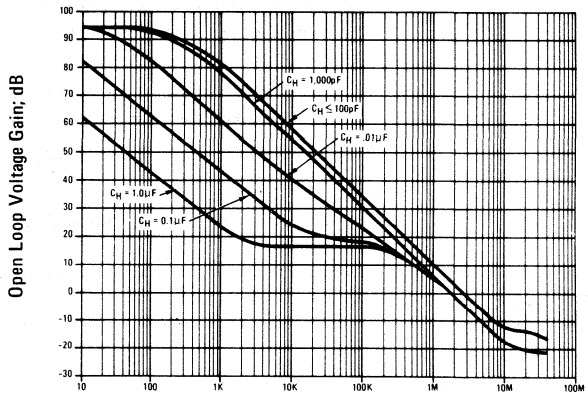
C_H Value

BROADBAND NOISE CHARACTERISTICS



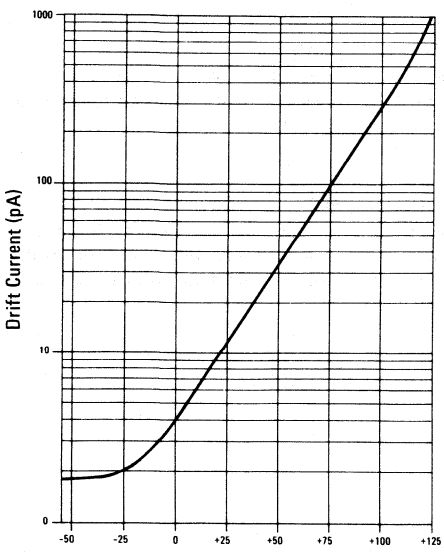
Bandwidth
(Lower 3db Frequency = 10Hz)

OPEN LOOP FREQUENCY RESPONSE



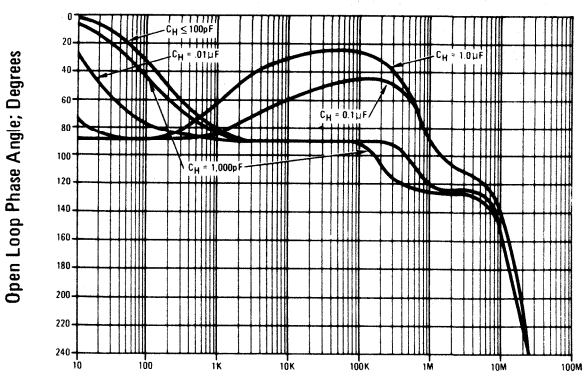
Frequency, Hz

DRIFT CURRENT vs TEMPERATURE



Temperature, (Degrees C)

OPEN LOOP PHASE RESPONSE



Frequency, Hz

4

APPLICATIONS

BASIC SAMPLE-AND-HOLD

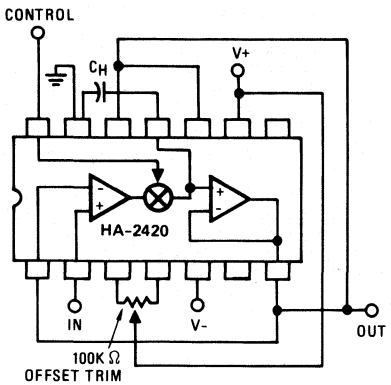


Figure 1

GUARD RING LAYOUT (BOTTOM VIEW)

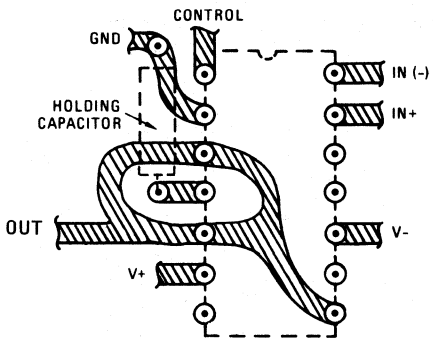


Figure 2

NOTES:
1) Figure 1 shows a typical unity gain circuit, with offset zeroing. All of the other normal op amp feedback configurations may be used with the HA-2420/2425. The input amplifier may be used as a gated amplifier by utilizing Pin 11 as the output. This amplifier has excellent drive capabilities along with exceptionally low switch leakage.
2) The method used to reduce leakage paths on the P.C. board and the device package is shown in Figure 2. This guard ring is recommended to minimize the drift during hold characteristic.
3) The holding capacitor should have extremely high insulation resistance and low dielectric absorption. Polystyrene (below +85°C), Teflon, or Parlene types are recommended.

For more applications, consult Harris Application Note 517.

GLOSSARY OF TERMS

ACQUISITION TIME:
The time required by the device after the "sample" command to reach its final value within ±0.1% or ±0.01%. This time includes switch delay time, slewing time and settling time. This is the minimum sample time required to obtain a given accuracy.

CHARGE TRANSFER:
The small charge transferred to the holding capacitor from the inter-electrode capacitance of the switch when the unit is switched to the Hold mode. Sample-to-Hold offset error is directly proportional to this charge, where:

$$\text{Offset Error (V)} = \frac{\text{Charge (pC)}}{C_H\text{(pF)}}$$

APERTURE DELAY:
The time required after the "hold" command until the switch is fully open. This delays the effective sample timing with rapidly changing input signals.

DRIFT CURRENT:
Leakage currents from the holding capacitor during the Hold mode which cause the output voltage to drift. Drift rate (droop rate) can be calculated from drift current values using the formula:

$$\frac{\Delta V}{\Delta T}\text{(Volts/Sec)} = \frac{I\text{(pA)}}{C_H\text{(pF)}}$$

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

6 a 10 stck 64,15

HI-562

12 Bit High Speed Monolithic Digital-to-Analog Converter

FEATURES

- MONOLITHIC CONSTRUCTION
- EXTREMELY FAST SETTLING — 300ns TO 0.01% (TYP.)
- LOW GAIN DRIFT — ±5ppm/°C (MAX.)
- EXCELLENT LINEARITY — ±1/2 LSB (MAX.)
- DESIGNED FOR MINIMUM GLITCHES
- MONOTONIC OVER TEMPERATURE

APPLICATIONS

- CRT DISPLAY GENERATION
- HIGH SPEED A/D CONVERTERS
- VIDEO SIGNAL RECONSTRUCTION
- WAVEFORM SYNTHESIZERS
- HIGH SPEED DATA ACQUISITION
- HIGH-REL APPLICATIONS
- PRECISION INSTRUMENTS

DESCRIPTION

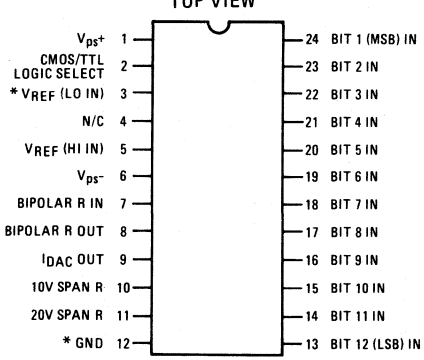
The Harris HI-562 is the first monolithic digital-to-analog converter to combine both ultra-high speed performance and 12-bit accuracy on the same chip. The HI-562's fast output current settling of 300ns to 0.01% is achieved using dielectric isolation processing to reduce internal parasitics for fast rise and fall times during switching. Output glitches are minimized in the HI-562 by incorporating equally weighted current sources switched into an R-2R ladder network for symmetrical turn-ON and turn-OFF switching times. This creates within the chip a very uniform and constant thermal distribution for excellent linearity and also completely eliminates thermal transients during switching. High stability thin film resistor processing together with laser trimming provide the HI-562 with guaranteed true 12-bit linearity to within ±1/2 LSB maximum at +25°C for -4 and -5 parts, and to within ±1/4 LSB maximum at +25°C for -2 and -8 parts. The HI-562 is recommended as a replacement for higher cost hybrid and modular units for increased reliability and accuracy in applications such as CRT displays, precision instruments and data acquisition systems requiring throughput rates as high as 3.3MHz for full range transitions. Its small size makes it an ideal choice as the heart of high speed A/D converter designs or as a building block in high speed or high resolution industrial process control systems. The HI-562 is also ideally suited for aircraft and space instrumentation where operation over a wide temperature range is required.

The HI-562-5 is specified for operation over 0°C to +75°C, the HI-562-4 over -25°C to +85°C and the HI-562-2 and HI-562-8 over -55°C to +125°C. Processing MIL-STD-883A Class B screening is available by selecting the HI-562-8. All are available in a hermetically sealed 24-lead dual-in-line package.

PINOUT

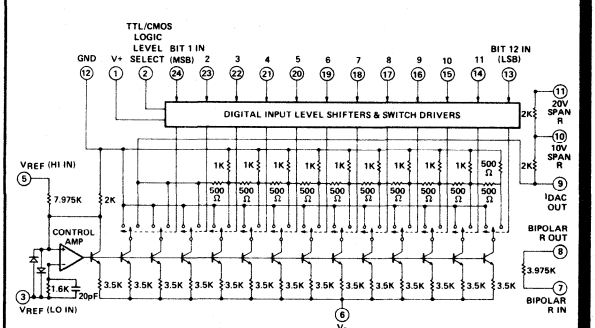
Package Code 1H, LC

TOP VIEW



*Pin 3 connected to bottom case for high frequency shielding.

FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Referred to Ground)[1]

Power Supply Inputs	$V_{PS}+$	+20V
	$V_{PS}-$	-20V
Reference Inputs	VREF (Hi)	$\pm V_{PS}$
Digital Inputs	Bits 1-12	-1V, +12V
	CMOS/TTL Logic Select	-1V, +12V
Outputs	Pins 7, 8, 10, 11	$\pm V_{PS}$
	Pin 9	$+V_{PS}$, -5V

Power Dissipation P_d, Package	1000mW
Operating Temperature Range	
HI-562-2	-55°C to +125°C
HI-562-4	-25°C to +85°C
HI-562-5	0°C to +75°C
HI-562-8	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C

ELECTRICAL CHARACTERISTICS (@ +25°C, $V_{PS}+$, = +5V, $V_{PS}-$ = -15V, V_{REF} = +10V, pin 2 tied to pin 12 unless otherwise noted)

PARAMETER	CONDITIONS	HI-562-2/HI-562-8 MIN	HI-562-2/HI-562-8 TYP	HI-562-2/HI-562-8 MAX	HI-562-4/HI-562-5 MIN	HI-562-4/HI-562-5 TYP	HI-562-4/HI-562-5 MAX	UNITS
INPUT CHARACTERISTICS								
Digital Inputs (3)	Bit ON "Logic 1" Bit OFF "Logic 0"							
TTL Input Voltage (2) Logic "1"	Over full temp. range	2.0			2.0			V
TTL Logic "0"				0.8			0.8	V
TTL Input Current (2) Logic "1"	Pin 2 tied to Pin 12		20	100		20	100	nA
TTL Logic "0"			-50	-100		-50	-100	μA
CMOS Input Voltage Logic "1"	Pin 2 tied to pin 1, +4.75V ≤ $V_{PS}+$ ≤+12V over full temp. range	$0.7V_{PS}+$			$0.7V_{PS}+$			V
CMOS Logic "0"				$0.3V_{PS}+$			$0.3V_{PS}+$	V
CMOS Input Current Logic "1"			20	100		20	100	nA
CMOS Logic "0"			-50	-100		-50	-100	μA
Reference Input								
Input Resistance			8K			8K		Ω
Input Voltage			+10			+10		V
TRANSFER CHARACTERISTICS								
Resolution	Over full temp. range			12			12	Bits
Nonlinearity (3)	@ +25°C			±1/4		±1/4	±1/2	LSB
	Over full temp. range		±1/2	±1			±1	
Differential Nonlinearity (3)	@ +25°C			±1/4		±1/4	±1/2	LSB
	Over full temp. range			MONOTONICITY GUARANTEED				
Relative Accuracy (6)	With 24.9Ω(1%) Trim Resistors							
Gain Error	All Bits ON		±.024	±.10		±.024	±0.25	
Bipolar Offset Error	All Bits OFF		±.024	±0.25		±.024	±0.25	% FSR (4)
Unipolar Offset Error			±.012	±0.05		±.012	±0.05	
Adjustment Range	See Operating Instructions							
Gain	With 50Ω Trim		±0.3			±0.3		% FSR
Bipolar Offset	Potentiometers		±0.6			±0.6		
Temperature Stability	Drift specified with internal span resistors for voltage output							
Gain Drift (3)	Over full temp. range		±6	±10			±10	ppm of FSR/°C
Offset Drift (3)								
Unipolar Offset	All Bits OFF			±2			±2	
Bipolar Offset				±4			±4	
Differential Nonlinearity	Over full temp. range		±1	±2		±2	±2	
Settling Time (3) to ±1/2 LSB	All Bits ON-to-OFF or OFF-to-ON		300	400		300	400	ns

PARAMETER	CONDITIONS	HI-562-2/HI-562-8 MIN	HI-562-2/HI-562-8 TYP	HI-562-2/HI-562-8 MAX	HI-562-4/HI-562-5 MIN	HI-562-4/HI-562-5 TYP	HI-562-4/HI-562-5 MAX	UNITS
Major Carry Transient Peak Amplitude Settling Time to 90% Complete	From 011...1 to 100...0 or 100...0 to 011...1		0.7 35			0.7 35		mA ns
Power Supply Sensitivity (3) Unipolar Offset V_{ps}+ @ +5V or +15V V_{ps}- @ -15V Bipolar Offset V_{ps}+ @ 5V or +15V V_{ps}- @ -15V Gain V_{ps}+ @ +5V or +15V V_{ps}- @ -15V	All Bits OFF All Bits OFF, Bipolar mode All Bits ON		 ±0.5 ±0.5 ±1.5 ±1.5 	 ±3.5 ±3.5		 ±0.5 ±0.5 ±1.5 ±1.5 	 ±3.5 ±3.5	ppm of FSR/% V_{ps}
OUTPUT CHARACTERISTICS								
Output Current Unipolar Bipolar			-5.0 ±2.5			-5.0 ±2.5		mA
Resistance			1000			1000		ohms
Capacitance			20			20		pF
Output Voltage Ranges Unipolar Bipolar	Using external op amp and internal scaling resistors. See Figure 1 and Table 1 for connections		0 to +5 0 to +10 ±2.5 ±5 ±10			0 to +5 0 to +10 ±2.5 ±5 ±10		V
Compliance Limit (3)		-3		+10	-3		+10	V
Compliance Voltage (3)	Over full temp. range		±1.0			±1.0		V
Output Noise	0.1 to 10Hz (All Bits ON) 0.1 to 5MHz (All Bits ON)		30 100			30 100		µV (p-p)
POWER REQUIREMENTS								
V_{ps}+ (7) V_{ps}-	Over full temp. range	4.5 13.5	5 15	5.5 16.5	4.75 13.5	5 15	5.5 16.5	V
I_{ps}+ (5) I_{ps}- (5)	All Bits ON or OFF in either TTL or CMOS mode		9 28	15 40		9 28	15 40	mA
I_{ps}+ (5) I_{ps}- (5)	Same as above except over full temp. range		11 33	20 50		11 33	20 50	mA

NOTES

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.

2. V_{ps}+ tolerance is ±10% for HI-562-2, -8. and ±5% for HI-562-4, -5.

3. See Definitions.

4. FSR is "full scale range" and is 20V for ±10V range, 10V for ±5V range, etc.; or 5mA(±20%) for current output.

5. After 30 seconds warm-up.

6. Using an external op amp with internal span resistors and specified external trim resistors in place of potentiometers R_1 and R_2. Errors are adjustable to zero using R_1 and R_2 potentiometers. (See Operating Instructions Figure 2.)

7. Maximum V_{ps}+ is +12V for high level logic only, i.e. when pin 2 is tied to pin 1.

DEFINITIONS OF SPECIFICATIONS

DIGITAL INPUTS

The HI-562 accepts digital input codes in binary format and may be user connected for any one of three binary codes. Straight Binary, Two's Complement, or Offset Binary, (See Operating Instructions).

	ANALOG OUTPUT		
DIGITAL INPUT	Straight Binary	Offset Binary	Two's Complement*
MSB LSB			
000...000	Zero	-FS (Full Scale)	Zero
100...000	½FS	Zero	-FS
111...111	+FS – 1 LSB	+FS – 1 LSB	½FS – 1 LSB
011...111	½FS – 1 LSB	Zero – 1 LSB	+FS – 1 LSB

*Invert MSB with external inverter to obtain Two's Complement Coding

ACCURACY

NONLINEARITY – Nonlinearity of a D/A converter is an important measure of its accuracy. It describes the deviation from an ideal straight line transfer curve drawn between zero (all bits OFF) and full scale (all bits ON).

DIFFERENTIAL NONLINEARITY – For a D/A converter, it is the difference between the actual output voltage change and the ideal (1 LSB) voltage change for a one bit change in code. A Differential Nonlinearity of ±1 LSB or less guarantees monotonictiy; i.e., the output always increases and never decreases for an increasing input.

SETTLING TIME

Settling time is the time required for the output to settle to within the specified error band for any input code transition. It is usually specified for a full scale or major carry transition.

DRIFT

GAIN DRIFT – The change in full scale analog output over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Gain error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Gain drift is calculated for both high (T_H -25°C) and low ranges (+25°C -T_L) by dividing the gain error by the respective change in temperature. The specification is the larger of the two representing worst case drift.

OFFSET DRIFT – The change in analog output with all bits OFF over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Offset error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Offset Drift is calculated for both high (T_H -25°C) and low (+25°C -T_L) ranges by dividing the offset error by the respective change in temperature. The specification given is the larger of the two, representing worst-case drift.

POWER SUPPLY SENSITIVITY

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in -15V, +5V or +15V supplies. It is specified under DC conditions and expressed as parts per million of full scale range per percent of change in power supply (ppm of FSR/%).

COMPLIANCE

Compliance voltage is the maximum output voltage range that can be tolerated and still maintain its specified accuracy. Compliance limit implies functional operation only and makes no claims to accuracy.

GLITCH

A glitch on the output of a D/A converter is a large transient spike resulting from unequal internal ON-OFF switching times. Worst case glitches usually occur at half-scale or the major carry code transition from 011...1 to 100...0 or vice versa. For example, if turn ON is greater than turn OFF for 011...1 to 100...0, an intermediate state of 000...0 exists, such that, the output momentarily glitches to zero output. Matched switching times and fast switching will reduce glitches considerably.

DECOUPLING AND GROUNDING

For best accuracy and high frequency performance, the grounding and decoupling scheme shown in Figure 1 should be used. Decoupling capacitors should be connected close to the HI-562 (preferrably to the device pins) and should be tantalum or electrolytic bypassed with ceramic types for best high frequency noise rejection.

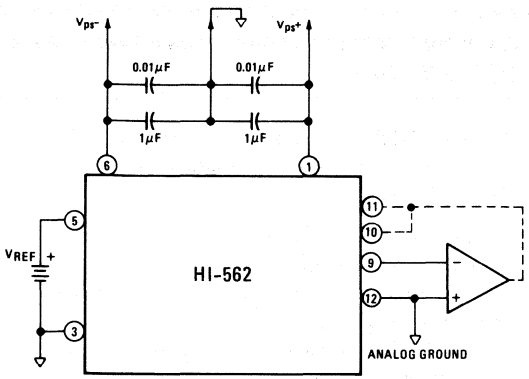
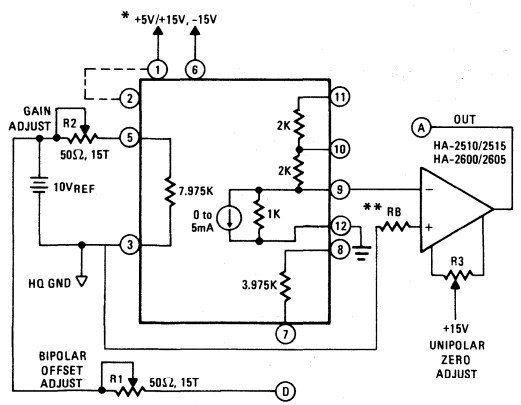


Figure 1

UNIPOLAR AND BIPOLAR VOLTAGE OUTPUT CONNECTIONS

CONNECTIONS – Using an external resistive load, the output compliance should not exceed ±1V to maintain specified accuracy. For higher output voltages, accuracy can be maintained by using an external op amp and the internal span resistors as shown in Figure 2 and defined in Table 1 for unipolar and bipolar modes.



* For TTL and DTL compatibility, connect +5V to pin 1 and tie pin 2 to pin 12. For CMOS compatibility, connect digital power supply ($+4.85V \leq V_{DD} \leq +12V$) to pin 1 and short pin 2 to pin 1.

** Bias resistor, RB, should be chosen to equalize op amp offset voltage due to bias current. Its value is calculated from the parallel combination of the current source output resistance (1K) and the op amp feedback resistor. See Table 1 for values of RB.

Figure 2

Table 1

	OUTPUT RANGE	CONNECTIONS Pin 7 to	Pin 8 to	Pin 10 to	Pin 11 to	BIAS (R_B) RESISTOR
Unipolar Mode	0 to +10V	N.C.	N.C.	A	N.C.	667Ω
	0 to +5V	N.C.	N.C.	A	9	500Ω
Bipolar Mode	±10V	D	9	N.C.	A	667Ω
	±5V	D	9	A	N.C.	580Ω
	±2.5V	D	9	A	9	444Ω

EXTERNAL GAIN AND ZERO CALIBRATION (See Figure 2)

The input reference resistor (7.975K) and bipolar offset resistors shown in Figure 2 are both intentionally set low by 25Ω to allow the user to externally trim-out initial errors to a very high degree of precision. The adjustments are made in the voltage output mode using an external op amp as current-to-voltage converter and the HI-562 internal scaling resistors as feedback elements for optimum accuracy and temperature coefficient. For best accuracy over temperature, select an op amp that has good front-end temperature coefficients such as the HA-2600/2605 with offset voltage and offset current tempco's of 5μV/°C and 1nA/°C, respectively. For high speed voltage mode applications where fast settling is required, the HA-2510/2515 is recommended for better than 1.5μs settling to 0.01%. Using either one, potentiometer R_3 conveniently nulls unipolar offset plus op amp offset in one operation (for HA-2510/2515 and HA-2600/2605 use R_3 = 20K and 100K, respectively). For bipolar mode operation, R_3 should be used to null op amp offset to optimize its tempco (i.e., short 9 to A and adjust R_3 for zero before calibrating in bipolar mode). The gain and bipolar offset adjustment range using 50Ω potentiometers is ±12 LSB and ±25 LSB respectively. If desired, the potentiometers can be replaced with fixed 24.9 Ω (1%) resistors resulting in an initial gain and bipolar offset accuracy of typically ±1/2 LSB.

UNIPOLAR CALIBRATION

Step 1: Unipolar Offset
- Turn all bits OFF
- Adjust R3 for zero volts output

Step 2: Gain
- Turn all bits ON
- Adjust R2 for an output of FS -1 LSB
  That is, adjust for:
  9.9976V for 0V to +10V range
  4.9988V for 0V to +5V range

BIPOLAR CALIBRATION

Step 1: Bipolar Offset
- Turn all bits OFF
- Adjust R1 for an output of:
  -10V for ±10V range
  -5V for ±5V range
  -2.5V for ±2.5V range

Step 2: Gain
- Turn bit 1 (MSB) ON; all other bits OFF
- Adjust R2 for zero volts output

4

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HI-1080/1085

Precision Monolithic 8-Bit D to A Converter

4

FEATURES

- GUARANTEED ±1 L.S.B. ACCURACY OVER TEMPERATURE
  - HI-1080 -55°C to +125°C
  - HI-1085 0°C to +75°C
- FAST SETTLING 1.5 μs to ½ L.S.B.
- EXPANDABLE FOR HIGHER RESOLUTIONS
- MONOLITHIC CONSTRUCTION
- DTL/TTL COMPATIBLE INPUTS
- RELIABLE MONOLITHIC CONSTRUCTION MEETS REQUIREMENTS OF MIL-STD-883

APPLICATIONS

- WAVEFORM SYNTHESIZERS
- MICROPROCESSOR I/O INTERFACE
- HIGH REL APPLICATIONS
- A TO D CONVERTER (USING COMPARATOR AND DIGITAL LOGIC)
- DATA ACQUISITION SYSTEMS

DESCRIPTION

The HI-1080/1085 is a monolithic 8 bit digital-to-analog converter employing bipolar current switches feeding a thin film R-2R ladder network.

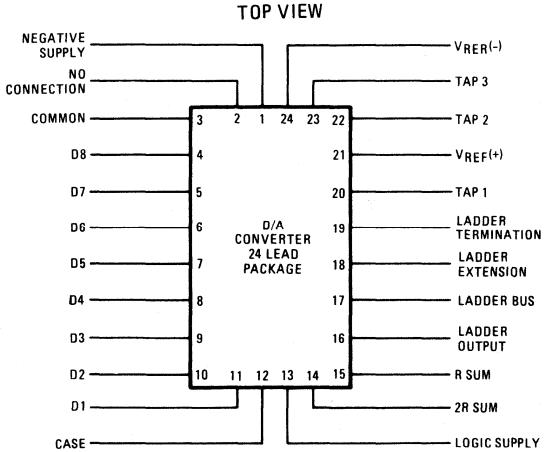
Because of the excellent stability of this device, it is practical to specify one all-inclusive accuracy parameter: ±1L.S.B. accuracy over the operating temperature range. This means that once the desired full scale output level is set at room temperature by adjustment of the input reference current, each of the 256 output levels will always measure within ±1 L.S.B. of the corresponding output of a "perfect" DAC. Thus the accuracy specification includes the worst case effects of all of the normally published errors such as non-linearity, zero drift, full scale drift, etc.

The device is exceptionally versatile, since it may be used in a voltage or current output mode, and may be offset to produce bipolar operation. Matched auxillary resistors are provided for amplifier feedback or current summing. Provisions are also made for scale factor adjustment and for cascading of additional D/A converters for extended resolution.

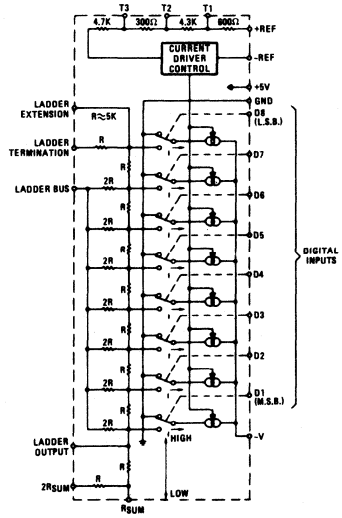
PINOUT

Package Code 4K

TOP VIEW



FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Maximum Ratings are limiting values above which permanent circuit damage may occur.

Voltage
- V+ +8.0V
- V- -18.0V

Digital Inputs: +5.5V

Ladder Common: +8.0V

I_{REF}: 1.6mA

Storage Temperature: $-65^{o}C \leq TA \leq +150^{o}C$

Power Dissipation: 450mW *

*Derate at 4mW/°C above 85°C ambient.

ELECTRICAL CHARACTERISTICS

Unless otherwise stated all measurements taken at V+ = +5V, V- = -15V
V_{REF} = +5V, V_{in}High = +2.4V, V_{in}Low = +0.4V
Unipolar, zero reference connection (Figure 3)

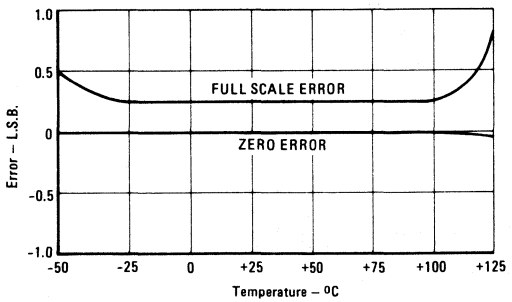
	TEMP	HI-1080 MIN	HI-1080 TYP	HI-1080 MAX	TEMP	HI-1085 MIN	HI-1085 TYP	HI-1085 MAX	UNITS
Resolution		8				8			Bits
Accuracy	+25°C		1/4	1/2					
(Calibrated at 25°C) (Note 1)	-55°C to +125°C		1/2	1	0°C to +75°C		1/2	1	L.S.B.
$V_{Full\ Scale}$ (Note 2) (Uncalibrated)	+25°C	-4.5	-4.98	-5.5	+25°C	-4.5	-4.98	-5.5	Volts
Power Supply Rejection (Note 3)	-55°C to +125°C	.05	.001		0°C to +75°C	.05	.001		L.S.B. per Volt
Settling Time (Note 4)	+25°C		1.5	3.0	+25°C		1.5		μs
Digital Inputs:									
High Threshold				2.0				2.0	Volts
Low Threshold (Note 5)		0.8				0.8			Volts
I_{in}High			.01	1	0°C		.01	1	mA
Iin Low (Note 6)	-55°C to +125°C		-0.7	-1.0	to +75°C		-0.7	-1.0	mA
Supply Current:									
I+	-55°C		8	10	0°C		8	10	mA
I-	to		8	10	to		8	10	mA
I_{REF} (Note 7)	+125°C		0.5	0.6	+75°C		0.5	0.6	mA

NOTES: Test Conditions -

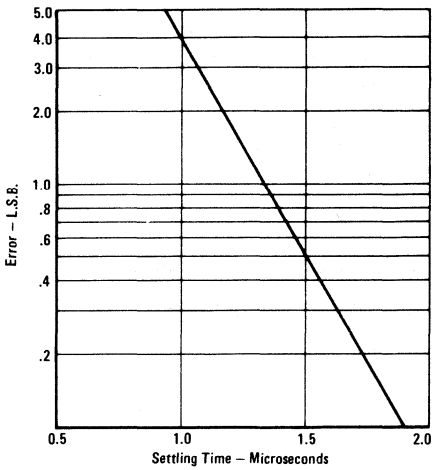
1. Any Input Combination
2. Inputs all low
3. $\Delta V_{OUT}/\Delta V_{SUPPLY}$
   V+ = +5 ± 0.5V
   V- = -15 ± 3V
4. To ±0.2% of full scale after full scale input step
   $R_L > 10M$
   $C_L < 5pF$
5. V+ = 4.5V
6. V_{in} = 2.4 Volts
   V+ = 5.5V
   V_{in} = 0.4 Volts
   V+ = 5.5V
7. V+ = +5.0V
   V- = -15.0V
   V_{REF} = +5.0V
   Inputs all low

PERFORMANCE CURVES

TYPICAL OUTPUT ACCURACY vs. TEMPERATURE



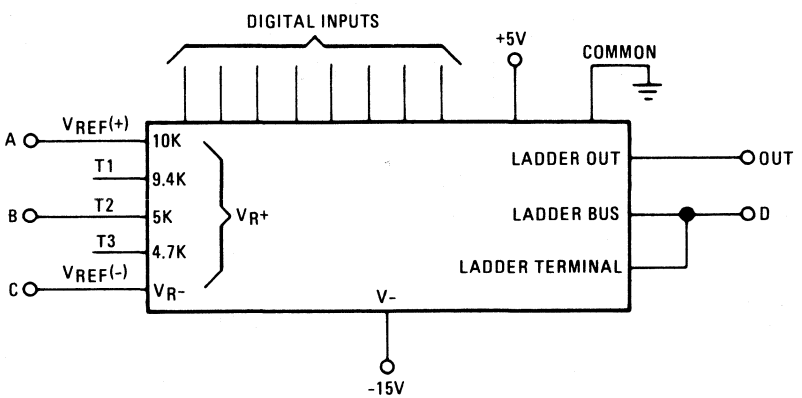
TYPICAL SETTLING TIME



OPERATING MODES

4

D/A CONVERTER OPERATION MODES

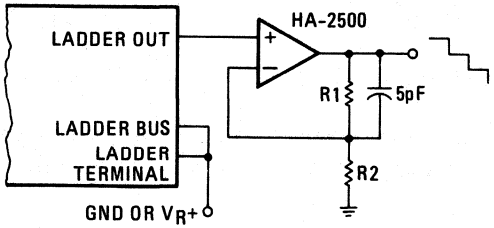


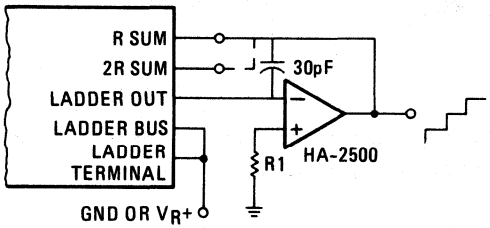
MODE	OUTPUT RANGE INPUTS: ALL HIGH TO ALLLOW	CONNECTIONS			
		A*	B*	C	D
UNIPOLAR ZERO REFERENCE	0 TO -V_{R+} -1L.S.B.	V_{R+}	N.C.	GND	GND
UNIPOLAR ZERO F.S.	+/V_{R+}/TO 0 +1L.S.B.	V_{R+}	N.C.	GND	V_R
BIPOLAR	/V_{R+}/TO -V_R +1L.S.B.	N.C.	V_{R+}	GND	V_{R+}

OPERATING MODES

*Tap 1 or Tap 3 with selected external series resistors may be substituted for points A or B, respectively, for fine adjustment of output range.

BUFFER AMPLIFIER CONNECTION





NON-INVERTING OUTPUT

(MORE NEGATIVE WITH INCREASING COMPLEMENT OF INPUT NUMBER)

OUTPUT RANGE: SAME AS SHOWN ON 'OPERATING MODE' CHART

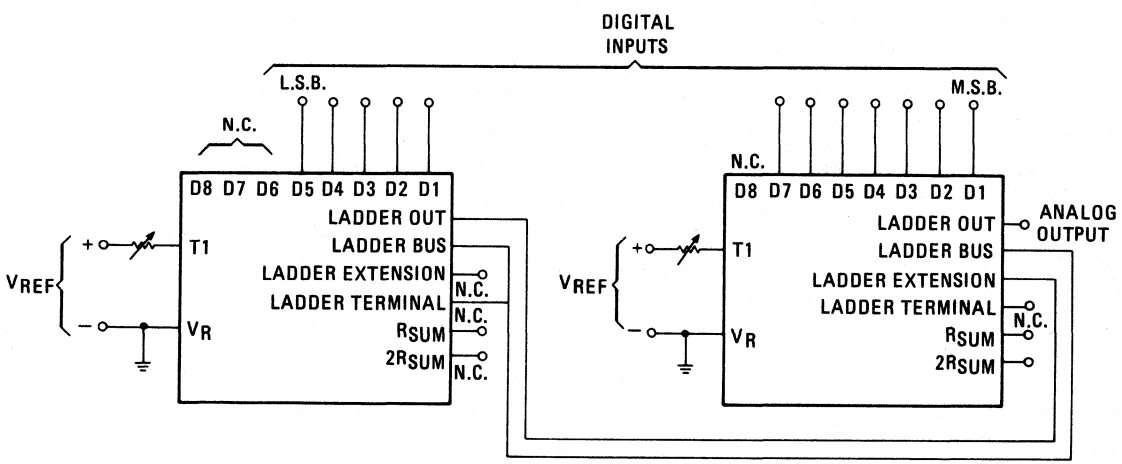
MULTIPLIED BY $1 + \frac{R1}{R2}$

INVERTING OUTPUT

(MORE POSITIVE WITH INCREASING COMPLEMENT OF INPUT NUMBER)

*FULL SCALE OUTPUT	OUTPUT FEEDBACK CONNECTED TO	R1
+4.98V	R_{SUM}	2.5K
+9.96V	$2R_{SUM}$	3.3K

CASCADED UNITS FOR 12 BIT RESOLUTION



HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HI-5610

10 Bit High Speed Monolithic Digital-to-Analog Converter

Preliminary

FEATURES

- MONOLITHIC CONSTRUCTION
- EXTREMELY FAST SETTLING. . . . . 85ns TO ½LSB TYP.
- LOW GAIN DRIFT. . . . . ±5ppm/°C TYP.
- EXCELLENT LINEARITY OVER TEMPERATURE . . . . . ±½LSB MAX.
- DESIGNED FOR MINIMUM GLITCHES
- MONOTONIC OVER TEMPERATURE

APPLICATIONS

- CRT DISPLAY GENERATION
- HIGH SPEED A/D CONVERTERS
- VIDEO SIGNAL RECONSTRUCTION
- WAVEFORM SYNTHESIZERS
- HIGH SPEED DATA ACQUISITION
- HIGH RELIABILITY APPLICATIONS
- PRECISION INSTRUMENTS

DESCRIPTION

The HI-5610 is an ultra-high speed 10 bit monolithic current output digital-to-analog converter. The fast output current settling of 85ns to ½LSB of its final value is achieved using dielectric isolation processing to reduce internal parasitics for fast rise and fall times during switching. Output glitches are minimized in the HI-5610 by incorporating equally weighted current sources switched into an R-2R ladder network for symmetrical turn-on and turn-off switching times. This creates within the chip a very uniform and constant thermal distribution for excellent linearity and also eliminates thermal transients during switching. High stability thin film resistor processing, together with laser trimming provide the HI-5610 with true 10 bit linearity to within ± ½LSB maximum over operating temperature range. The HI-5610's low offset and gain drift over the operating temperature range assures that its absolute accuracy when referred to a fixed 10V reference will not deviate more than ±1LSB for both unipolar and bipolar operation.

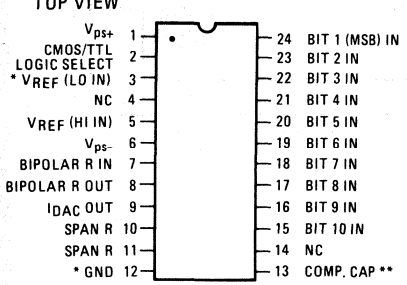
The HI-5610 is recommended as a replacement for high cost hybrid and modular units for increased reliability and accuracy in applications such as CRT Displays, precision instruments and data acquisition system requiring through-put rates as high as 12mHz for full range transitions. Its small size makes it an ideal choice as the essential part of high speed A/D converter designs or as a building block in high speed or high resolution industrial process control systems. The HI-5610 is also ideally suited for aircraft and space instrumentation where operation over a wide temperature range is required.

The HI-5610-5 is specified for operation over 0°C to +75°C, the HI-5610-2 and HI-5610-8 over -55°C to +125°C. Processing to MIL-STD-883A class B screening is available by selecting the HI-5610-8. All are available in a hermetically sealed 24 lead dual-in-line package.

PINOUT

TOP VIEW

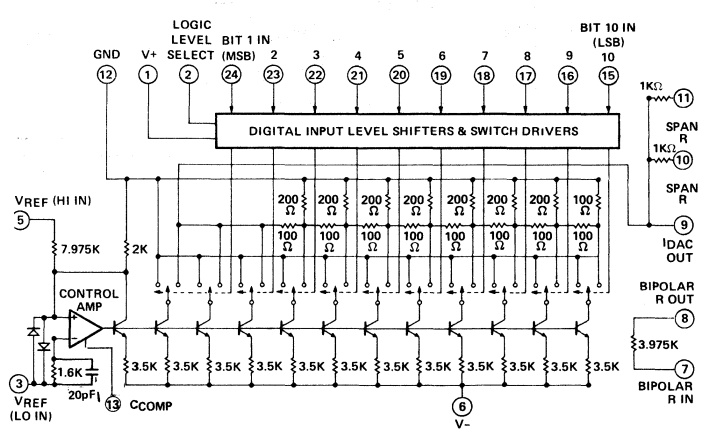
Package Code 1H



* Pin 3 connected to bottom case for high frequency shielding.

** For high speed operation, connect 0.01μF between Pin 13 and GND. Otherwise, leave Pin 13 open.

FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Referred to Ground)[1]

Power Supply Inputs	$V_{ps}+$	+20V
	$V_{ps}-$	-20V
Reference Inputs	VREF (Hi)	$\pm V_{ps}$
	VREF(Lo)	0V
Digital Inputs	Bits 1 - 12	-1V, +12V
	CMOS/TTL Logic Select	-1V, +12V
Outputs	Pins 7, 8, 10, 11	$\pm V_{ps}$
	Pin 9	$+V_{ps}$, -5V

Power Dissipation Pd, Package	1000mW
Operating Temperature Range	
HI-5610-2	-55°C to +125°C
HI-5610-5	0°C to +75°C
HI-5610-8	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C

ELECTRICAL CHARACTERISTICS (@ +25°C, $V_{ps}+$, = +5V, $V_{ps}-$ = -15V, V_{REF} = +10V, pin 2 ground unless otherwise noted)

		HI-5610-2 HI-5610-8			HI-5610-5			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS								
Digital Inputs (2)								
TTL Logic Input Voltage (3)								
Logic "1"	Full	2.0			2.0			V
Logic "0"	Full			0.8			0.8	V
Input Current								
Logic "1"	Full		20	100		20	100	nA
Logic "0"	Full		-50	-100		-50	-100	μA
CMOS Logic Input Voltage (4)								
Logic "1"	Full	$0.7V_{ps}+$			$0.7V_{ps}+$			V
Logic "0"	Full			$0.3V_{ps}+$			$0.3V_{ps}+$	V
Input Current								
Logic "1"	Full		20	100		20	100	nA
Logic "0"	Full		-50	-100		-50	-100	μA
Reference Input								
Input Resistance			8K			8K		Ω
Input Voltage (I_{OUT} = 5mA + 20%)			+10			+10		V
TRANSFER CHARACTERISTICS								
Resolution	Full			10			10	Bits
Nonlinearity (5)	25°C			±½			±½	LSB
Differential Nonlinearity (5)	25°C			±½			±½	LSB
Relative Accuracy (6)								
Gain Error								(9)
(Input Code 11....1)			±0.05			±0.05		% FSR
Unipolar Offset Error								
(Input Code 00....0)			±0.05			±0.05		% FSR
Bipolar Offset Error								
(Input Code 00....0) (Adjustable to zero, see Figure 4, 5)			±0.05			±0.05		% FSR
Adjustment Range								
Gain			±0.25			±0.25		% FSR
Bipolar Offset			±0.25			±0.25		% FSR
Temperature Stability								
Gain Drift	Full		±5			±5		ppm/°C
Unipolar Offset Drift	Full		±3			±3		ppm/°C
Bipolar Offset Drift	Full		±3			±3		ppm/°C
Differential Nonlinearity	Full		±2			±2		ppm/°C
MONOTONICITY - GUARANTEED OVER FULL OPERATING TEMPERATURE RANGE								
Settling Time to ½LSB (5)								
From all 0's to all 1's			85			85		ns
From all 1's to all 0's			85			85		ns
Major Carry Switching to 90% Complete			40			40		ns

PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Power Supply Sensitivity (5) $V_{ps}+$ = +5V, $V_{ps}-$ = -13.5V to -16.5V Gain (Input Code 11....1) Unipolar Offset (Input Code 00....0) Bipolar Offset (Input Code 00....0)			 ±0.5 ±1.5	±2		 ±0.5 ±1.5	±2	ppm of FSR/%V_{ps}
$V_{ps}-$ = -15V, $V_{ps}+$ = 4.5V to 5.5V Gain (Input Code 11....1) Unipolar Offset (Input Code 00....0) Bipolar Offset (Input Code 00....0)			 ±0.5 ±1.5	±1		 ±0.5 ±1.5	±1	
OUTPUT CHARACTERISTICS								
Output Current Unipolar Bipolar			 -5.0 ±2.5			 -5.0 ±2.5		 mA mA
Output Resistance			200			200		Ω
Output Capacitance			20			20		pF
Output Voltage Range (7) Unipolar Bipolar			 +5 +2.5 ±2.5 ±1.25			 +5 +2.5 ±2.5 ±1.25		 V V V V
Output Compliance Limit (5)		-3		+10	-3		+10	V
Output Compliance Voltage (5)	Full		±1.5			±1.5		V
Output Noise Voltage (8) 0.1Hz to 100Hz 0.1Hz to 1MHz			 10 100			 10 100		 μV_{p-p} μV_{p-p}
POWER REQUIREMENTS								
$V_{ps}+$ (4)	Full	4.5	5	15	4.75	5	15	V
$V_{ps}-$	Full	13.5	15	16.5	13.5	15	16.5	V
$I_{ps}+$ (All 1's or all 0's in (10) either TTL or CMOS Mode)	25°C Full		9 20			9 20		mA mA
$I_{ps}-$ (Same as above) (10)	25°C Full		25 30			25 30		mA mA

NOTES

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. The HI-5610 accepts digital input codes in binary format and may be user connected for any one of three binary codes. Straight binary, offset binary, or two's complement binary. (See operating instructions)
3. For TTL and DTL compatibility connect +5V to pin 1 and ground pin 2. The V_{ps+} tolerance is ±10% for HI-5610-2, -8. And ± 5% for HI-5610-5.
4. For CMOS compatibility connect digital power supply ($+4.5V \leq V_{DD} \leq +10V$) to pin 1 and short pin 2 to pin 1.
5. See definitions.
6. Using an external op amp with internal span resistors and 24.9Ω ± 1% external trim resistors in place of potentiometers R1 and R2. These errors are adjustable to zero using R1 and R2. (See operating instructions)
7. Using an external op amp and internal span resistors. (See operating instructions for connections)
8. Specified for digital input in all '1's or all '0's.
9. FSR is "Full Scale Range" and is 5V for ± 2.5V range, 2.5V for ± 1.25V range, etc., or 5mA (± 20%) for current output.
10. After 30 seconds warm-up.

DEFINITIONS OF SPECIFICATIONS

ACCURACY

NONLINEARITY - Nonlinearity of a D/A converter is an important measure of its accuracy. It describes the deviation from an ideal straight line transfer curve drawn between zero (all bits OFF) and full scale (all bits ON).

DIFFERENTIAL NONLINEARITY - For a D/A converter, it is the difference between the actual output voltage change and the ideal (1LSB) voltage change for a one bit change in code. A Differential Nonlinearity of ± 1LSB or less guarantees monotonicitiy; i.e., the output always increases and never decreases for and increasing input.

SETTLING TIME

Settling time is the time required for the output to settle to within the specified error band for any input code transition. It is usually specified for a full scale or major carry transition (01.....1 to 10.....0 or vice versa)

DRIFT

GAIN DRIFT - The change in full scale analog output over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Gain error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Gain drift is calculated for both high (T_H -25°C) and low ranges (+25°C - T_L) by dividing the gain error by the respective change in temperature. The specification is the larger of the two representing worst case drift.

OFFSET DRIFT - The change in analog output with all bits OFF over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Offset error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Offset Drift is calculated for both high (T_H -25°C) and low (+25°C -T_L) ranges by dividing the offset error by the respective change in temperature. The specification given is the larger of the two, representing worst case drift.

POWER SUPPLY SENSITIVITY

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in -15V, +5V or +15V supplies. It is specified under DC conditions and expressed as parts per million of full scale range per percent of change in power supply (ppm of FSR/%).

COMPLIANCE

Compliance voltage is the maximum output voltage range that can be tolerated and still maintain its specified accuracy. Compliance limit implies functional operation only and makes no claims to accuracy.

GLITCH

A glitch on the output of a D/A converter is a large transient spike resulting from unequal internal ON-OFF switching times. Worst case glitches usually occur at half-scale or the major carry code transition from 011.....1 to 100.....0 or vice versa. For example, if turn ON is greater than turn OFF for 011.....1 to 100.....0, an intermediate state of 000.....0 exists, such that, the output momentarily glitches to zero output. Matched switching times and fast switching will reduce glitches considerably.

OPERATING INSTRUCTIONS

DECOUPLING AND GROUNDING

For best accuracy and high speed performance, the grounding and decoupling scheme shown in Figure 1 should be used. Decoupling capacitors should be connected close to the HI-5610 (preferrably to the device pin) and should be tantalum or electrolytic bypassed with ceramic types for best high frequency noise rejection.

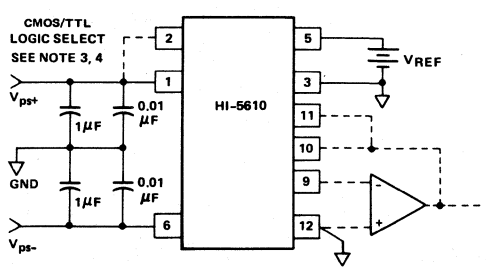


FIGURE 1

HIGH PERCISION PERFORMANCE

The output accuracy of the HI-5610 depends mainly on the accuracy of the voltage applied to the VREF input of HI-5610 and it can be described roughly as VREF/8KΩ = ¼ full scale output current. This means the output of HI-5610 will change whenever VREF varies. For high precision performance a precision +10V voltage reference with reasonably low temperature coefficient such as HA-1600 is highly recommended. For voltage output operation use an external op amp as current-to-voltage converter and the HI-5610 internal scaling resistors as feedback elements for optimum accuracy and temperature coefficient. The selected op amp should have a good front-end temperature coefficient such as HA-2600/2605 with offset voltage and offset current tempco's of 5 μV/°C and 1nA/°C, respectively. The input reference resistor (7.975K Ω) and bipolar offset resistor (3.975K Ω) are both intentionally set low by 25 Ω to allow the user to externally trim-out initial errors to a very high degree of precision. For high speed voltage output applications where fast settling is required, the HA-2510/2515 is recommended for better than 1 μs settling to ½LSB.

UNIPOLAR VOLTAGE OUTPUT CONNECTIONS AND CALIBRATION

The connections for unipolar +5V and +2.5V voltage output using an external op amp and the internal span resistors are shown in Figure 2 and Figure 3, respectively.

CALIBRATION - UNIPOLAR

Step 1 Offset
- Turn all bits off (all 0's)
- Adjust R3 for zero volts output

Step 2 Gain
- Turn all bits on (all 1's)
- Adjust R1 for an output of FS-1LSB
  That is, adjust for:
  4.99512V for 0V to +5V range
  2.49756V for 0V to +2.5V range

UNIPOLAR - STRAIGHT BINARY
0V TO +5V OUTPUT RANGE

DIGITAL INPUT	ANALOG OUTPUT	
11 1	FS - 1LSB	= 4.99512V
10 0	½FS	= 2.50000V
01 1	½FS -1LSB	= 2.49512V
00 0	Zero	= 0.00000V

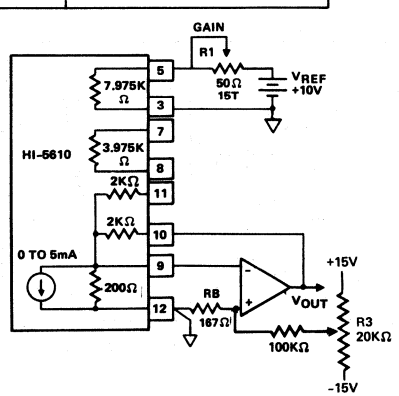


FIGURE 2

UNIPOLAR - STRAIGHT BINARY
0V TO +2.5V OUTPUT RANGE

DIGITAL INPUT	ANALOG OUTPUT	
11 1	FS - 1LSB	= 2.49756V
10 0	½FS	= 1.25000V
01 1	½FS -1LSB	= 1.24756V
00 0	Zero	= 0.00000V

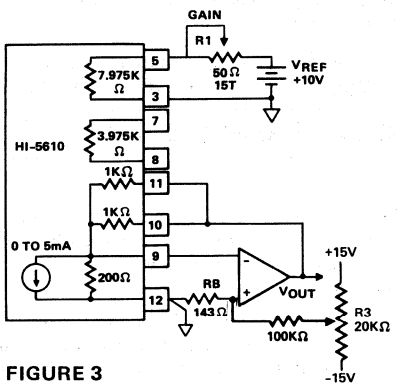


FIGURE 3

BIPOLAR VOLTAGE OUTPUT CONNECTIONS AND CALIBRATION

The connections for Bipolar ± 2.5V and ± 1.25V voltage output using an external op amp and the internal span resistors are shown in Figure 4 and Figure 5, respectively.

CALIBRATION - BIPOLAR

Step 1 Op Amp Null
- Short op amp output to op amp -input
- Adjust R3 for zero volts output

Step 2 Gain
- Turn all bits on (all 1's) record output voltage
- Turn all bits off (all 0's) record output voltage
- Adjust R1 till the difference between the readings is equal to:
  4.99512V for ± 2.5V range
  2.49756V for ±1.25V range

Step 3 Offset
- Turn bit 1 (MSB) on, all other bits off (10....0)
- Adjust R2 for zero volts output

BIPOLAR - OFFSET BINARY
±2.5V OUTPUT VOLTAGE RANGE

DIGITAL INPUT	ANALOG OUTPUT	
11 1	+FS - 1 LSB	= +2.49512V
10 0	ZERO	= +0.00000V
01 1	Zero - 1 LSB	= -0.00488V
00 0	-FS	= -2.50000V

BIPOLAR TWO'S COMPLEMENT **
±2.5V OUTPUT VOLTAGE RANGE

DIGITAL INPUT	ANALOG OUTPUT	
01 1	+FS - 1LSB	= +2.49512V
00 0	Zero	= +0.00000V
11 1	Zero - 1LSB	= -0.00488V
10 0	-FS	= -2.50000V

** Invert MSB with external inverter
to obtain two's complement coding.

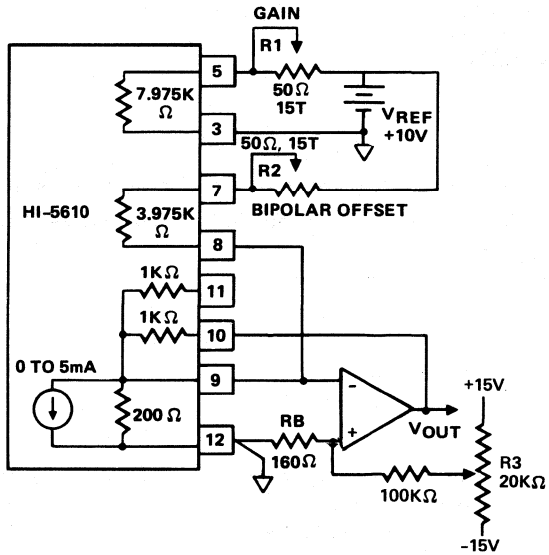


FIGURE 4

BIPOLAR - OFFSET BINARY
±1.25V OUTPUT VOLTAGE RANGE

DIGITAL INPUT	ANALOG OUTPUT	
11 1	+FS - 1LSB	= +1.24756V
10 0	Zero	= +0.00000V
01 1	Zero - 1LSB	= -0.00244V
00 0	-FS	= -1.25000V

BIPOLAR - TWO'S COMPLEMENT **
±1.25V OUTPUT VOLTAGE RANGE

DIGITAL INPUT	ANALOG OUTPUT	
01 1	+FS - 1LSB	= +1.24756V
00 0	Zero	= +0.00000V
11 1	Zero - 1LSB	= -0.00244V
10	-FS	= -1.25000V

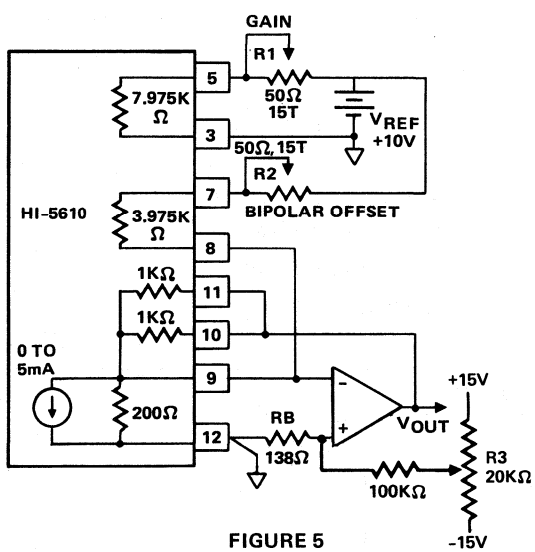


FIGURE 5

4

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HI-5618A/5618B

8 Bit High Speed Digital-to-Analog Converters

Preliminary

FEATURES

- VERY FAST SETTLING CURRENT OUTPUT 45ns TYP.
- MAXIMUM NONLINEARITY
  - HI-5618A ±1/4 LSB
  - HI-5618B ±1/2 LSB
- ON-CHIP RESISTORS FOR GAIN AND BIPOLAR OFFSET
- GUARANTEED MONOTONIC OVER TEMPERATURE
- DESIGNED FOR MINIMUM GLITCHES
- CMOS OR TTL INPUT COMPATIBLE

APPLICATIONS

- HIGH SPEED PROCESS CONTROL
- CRT DISPLAY GENERATION
- HIGH SPEED A/D CONVERTERS
- VIDEO SIGNAL RECONSTRUCTION
- WAVEFORM SYNTHESIZERS
- HIGH RELIABLIITY APPLICATIONS

DESCRIPTION

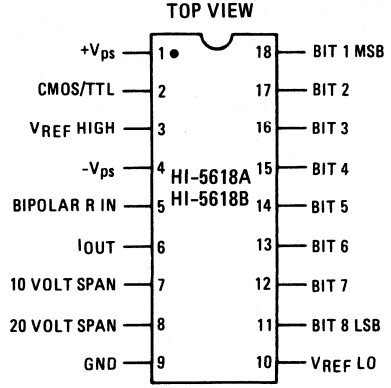
The HI-5618A/B are very high speed 8 bit current output D/A converters. These monolithic devices are constructed using dielectrically isolated bipolar processing which reduces internal parasitic capacitances allowing fast rise and fall times. This achieves a typical full scale settling time of 45ns to ±½ LSB. Output glitches are minimized by incorporating equally weighted current sources switched into either an R-2R ladder network or ground for symmetrical turn ON and turn OFF times. High stability thin film resistor processing and laser trimming provide these devices with excellent accuracies over the full operating temperature range. The HI-5618A has a maximum nonlinearity error of ± ¼ LSB and a guaranteed relative accuracy of ± ½ LSB over the full operating temperature range.

The HI-5618A/B are recommended for applications requiring high speed and accurate conversion over the full operating temperature range. These devices can be used in CRT displays and data acquisition systems requiring throughput rates as high as 20MHz for full range transitions. These 8 bit D/A converters are ideally suited for applications in avionics, space instrumentation and defense systems where high speed and accurate conversions are required. Other applications include high speed process control systems.

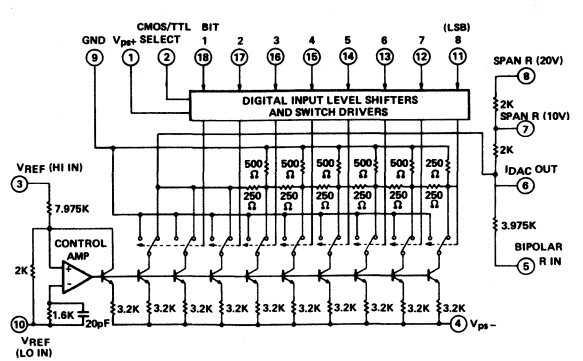
The HI-5618A/B in the -5 version are specified for operation from 0°C to +75°C. The HI-5618A/B in the -2 and -8 versions are specified from -55°C to +125°C. Processing to MIL-STD-883A, Class B screening is available by selecting the -8 devices.

PINOUT

TOP VIEW



FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Referred to Ground)[1]

Power Supply Inputs	$V_{PS}+$	+20V
	$V_{PS}-$	-20V
Reference Inputs	V_{REF} (Hi)	$\pm V_{PS}$
	V_{REF}(Lo)	0V
Digital Inputs	Bits 1 - 8	-1V, +12V
CMOS/TTL Logic Select		-1V, +12V
Outputs	Pins 5, 7, 8	$\pm V_{PS}$
	Pin 6	$+V_{PS}$, -2.5V

Power Dissipation Pd, Package	700mW
Operating Temperature Range	
HI-5618A/B-2	-55°C to +125°C
HI-5618A/B-5	0°C to +75°C
HI-5618A/B-8	-55°C to +125°C
Storage Temperature Range	-65°C to 150°C

ELECTRICAL CHARACTERISTICS

(@ +25°C, $V_{PS}+$ = +5V, $V_{PS}-$ = -15V, V_{REF} = +10V Pin 2 to GND, Unless otherwise noted)

PARAMETER		TEMP.	HI-5618A/B-2 HI-5618A/B-8 MIN.	TYP.	MAX.	HI-5618A/B-5 MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS									
Digital Inputs (2)									
TTL Logic Input Voltage (3)	Logic "1"	Full	2.0			2.0			V
	Logic "0"	Full			0.8			0.8	V
Input Current	Logic "1"	Full		20	100		20	100	nA
	Logic "0"	Full		-50	-100		-50	-100	μA
CMOS Logic Input Voltage (4)	Logic "1"	Full	$0.7V_{PS}+$			$0.7V_{PS}+$			V
	Logic "0"	Full			$0.3V_{PS}+$			$0.3V_{PS}+$	V
Input Current	Logic "1"	Full		20	100		20	100	nA
	Logic "0"	Full		-50	-100		-50	-100	μA
Reference Input									
Input Resistance		+25°C		8K			8K		Ω
Input Voltage (I_{OUT} = 5mA + 20%)		+25°C		+10			+10		V
TRANSFER CHARACTERISTICS									
Resolution		Full		8			8		Bits
Nonlinearity	HI-5618A	25°C			± 1/4			± 1/4	LSB
		Full			± 3/8			± 3/8	LSB
	HI-5618B	25°C			± 1/2			±1/2	LSB
		Full			± 5/8			± 5/8	LSB
Initial Accuracy (6) (Relative to External +10 V Reference)									
Gain		25°C			± 2			± 2	LSB
Unipolar Zero		25°C			± 1/8			±1/8	LSB
Bipolar Zero		25°C			±2			± 2	LSB
Gain Adjustment		25°C	± 3			± 3			LSB
Bipolar Zero Adjustment		25°C	± 3			± 3			LSB
Stability									
Gain		Full			± 1/8			± 1/8	LSB
Unipolar Zero		Full			± 1/16			± 1/16	LSB
Bipolar Zero		Full			± 1/8			±1/8	LSB

PARAMETER	TEMP.	HI-5618A/B-2 HI-5618A/B-8 MIN.	TYP.	MAX.	HI-5618A/B-5 MIN.	TYP.	MAX.	UNITS
Settling Time (5) to 1/2 LSB								
High Impedance (11) (from all 0's to all 1's) or (from all 1's to all 0's)	+25°C		55	75		55	75	ns
50Ω Load (12) (from all 0's to all 1's) or (from all 1's to all 0's)	+25°C		45			45		ns
Low Impedance (13) (from all 0's to all 1's) or (from all 1's to all 0's)	+25°C		55			55		ns
Major Carry Transition (5)								
Duration, t_0	+25°C		20			20		ns
Amplitude, V_A	+25°C		350			350		mV
Power Supply Sensitivity (5)								
$V_{ps}+$ = +5V, $V_{ps}-$ = -13.5V to -16.5V								
Gain (Input Code 11 . . . 1)	+25°C			±3.5			±3.5	
Unipolar Offset (Input Code 00 . . . 0)	+25°C		±0.5			±0.5		ppm of FSR/% V_{ps}
Bipolar Offset (Input Code 00 . . . 0)	+25°C		±1.5			±1.5		
$V_{ps}-$ = -15V, $V_{ps}+$ = 4.5V to 5.5V								
Gain (Input Code 11 . . . 1)	+25°C			±3.5			±3.5	
Unipolar Offset (Input Code 00 . . . 0)	+25°C		±0.5			±0.5		
Bipolar Offset (Input Code 00 . . . 0)	+25°C		±1.5			±1.5		

OUTPUT CHARACTERISTICS

Output Current	Unipolar	+25°C		-5			-5		mA
	Bipolar	+25°C		±2.5			±2.5		mA
Output Resistance		+25°C		500			500		Ω
Output Capacitance		+25°C		20			20		pF
Output Voltage Range (7)	Unipolar	+25°C		+10			+10		V
		+25°C		+5			+5		V
	Bipolar	+25°C		±10			±10		V
		+25°C		±5			±5		V
		+25°C		±2.5			±2.5		V
Output Compliance Voltage (5)		+25°C		±1.5			±1.5		V
Output Noise Voltage (8) 0.1Hz to 100Hz		+25°C		30			30		μV_{p-p}
0.1Hz to 1MHz		+25°C		100			100		μV_{p-p}

POWER REQUIREMENTS (4)

$V_{ps}+$	Full	4.5	5	15	4.75	5	15	V
$V_{ps}-$	Full	13.5	15	16.5	14.25	15	15.75	V
$I_{ps}+$ (10) (All 1's or all 0's in either TTL or CMOS mode)	+25°C		9			9		mA
	Full			12			12	mA
$I_{ps}-$ (10) (All 1's or all 0's in either TTL or CMOS mode)	+25°C		19			19		mA
	Full			24			24	mA

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. The HI-5618 accepts digital input codes in binary format and may be user connected for any one of three binary codes. Straight binary, offset binary, or two's complement binary. (See operating instructions)
3. For TTL and DTL compatibility connect +5V to pin 1 and ground pin 2. The $V_{ps}+$ tolerance is ±10% for HI-5618A/B 2, -8; and ±5% for HI-5618A/B-5.
4. For CMOS compatibility connect digital power supply ($+4.5V \leq V_{DD} \leq +10V$) to pin 1 and short pin 2 to pin 1.
5. See definitions.
6. Using an external op amp with internal span resistors and 24.9Ω ± 1% external trim resistors in place of potentiometers R1 and R2. These errors are adjustable to zero using R1 and R2. (See operating instructions)
7. Using an external op amp and internal span resistors. (See operating instructions for connections)
8. Specified for digital input in all "1's" or all "0's".
9. FSR is "Full Scale Range" and is 5V for ±2.5V range, 2.5V for ±1.25V range, etc., or 5mA (± 20%) for current output.
10. After 30 seconds warm-up.
11. See Figure 7 for Test Circuit used.
12. See Figure 8 for Test Circuit used.
13. See Figure 9 for Test Circuit used.

DEFINITIONS OF SPECIFICATIONS

ACCURACY

NONLINEARITY - Nonlinearity of a D/A converter is an important measure of its accuracy. It describes the deviation from an ideal straightline transfer curve drawn between zero (all bits OFF) and full scale (all bits ON).

DIFFERENTIAL NONLINEARITY – For a D/A converter, it is the difference between the actual output voltage change and the ideal (1 LSB) voltage change for any two adjacent codes. A Differential Nonlinearity of ± 1 LSB or less guarantees monotonicity; i.e., the output always increases and never decreases for an increasing input.

DRIFT

GAIN DRIFT - The change in full scale analog output over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Gain error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Gain drift is calculated for both high (T_H -25°C) and low ranges (+25°C -T_L) by dividing the gain error by the respective change in temperature. The specification is the larger of the two representing worst case drift.

OFFSET DRIFT - The change in analog output with all bits OFF over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Offset error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Offset Drift is calculated for both high (T_H -25°C) and low (+25°C -T_L) ranges by dividing the offset error by the respective change in temperature. The specification given is the larger of the two, representing worst case drift.

ABSOLUTE ACCURACY - The absolute accuracy error of a D/A converter is defined as the difference between the ideal transfer characteristic and the actual output at the D/A over the full operating temperature range. The absolute accuracy error includes nonlinearity, initial gain and offset errors, and gain and offset drift errors over temperature. For the HI-5618A/B, the absolute accuracy is measured with the gain and bipolar adjustment potentiometers replaced by 24.9Ω (1%) trim resistors.

SETTLING TIME

Settling time is the time required for the output to settle to within the specified error band for any input code transition. It is usually specified for a full scale or major carry transition (01 .....1 to 10 ..... 0 or vice versa). D/A settling time may vary depending upon the impedance level being driven. A comparator presents a high impedance level while an op amp connected for current to voltage conversion presents a low impedance level. Figure 7, 8, and 9 show the test circuits used for testing the settling time of the HI-5618A/B

GLITCH

A glitch on the output of a D/A converter is a large transient spike resulting from unequal internal ON-OFF switching times. Worst case glitches usually occur at half-scale or the major carry code transition from 011 .... 1 to 100 .... 0 or vice versa. For example, if turn ON is greater than furn OFF for 011 .... 1 to 100 .... 0, an intermediate state of 000 .... 0 exists, such that, the output momentarily glitches to zero output. In general, when a D/A is driven by a set of external logic gates, the unmatched turn on - turn off times at the gates will add to the glitch problem. Test circuits and waveforms for the HI-5618A/B are shown in figures 10 and 11.

POWER SUPPLY SENSITIVITY

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in -15V, +5V or +15V supplies. It is specified under DC conditions and expressed as parts per million of full scale range per percent of change in power supply (ppm of FSR/%).

COMPLIANCE

Compliance voltage is the maximum output voltage range that can be tolerated and still maintain its specified accuracy.

OPERATING INSTRUCTIONS

DECOUPLING AND GROUNDING

For best accuracy and high speed performance, the grounding and decoupling scheme shown in Figure 1 should be used. Decoupling capacitors should be connected close to the HI-5618A/B; preferably to the device pin. A solid tantalum or electrolytic capacitor in parallel with a smaller ceramic type is recommended.

HIGH PRECISION PERFORMANCE

The output accuracy of the HI-5618A/B depends mainly on the accuracy of the voltage applied to the V_{REF} input of HI-5618A/B and it can be described roughly as $V_{REF}/8K\Omega$=¼ full scale output current. This means the output of HI-5618A/B will change whenever V_{REF} varies. For precision performance, a stable +10V reference with low temperature coefficient such as the HA-1600 is highly recommended. For voltage output operation use an external op amp as current-to-voltage converter and the HI-5618A/B internal scaling resistors as feedback elements for optimum

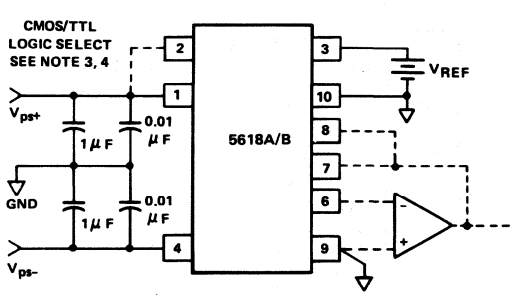


FIGURE 1

accuracy over temperature. The op amp should have good front-end temperature coefficients. For example, the HA-2600/2605 is well suited to this application, with offset voltage and offset current tempco's of 5 μV/°C and 1nA/°C respectively. The input reference resistor (7.975kΩ) and bipolar offset resistor (3.975kΩ) are both intentionally set low by 25Ω to allow the user to externally trim-out initial errors to a high degree of precision. For high speed voltage output applications where fast settling is required, the HA-2510/25 is recommended for settling times better than 250ns to 1/2 LSB. The HA-5190/95 is recommended for applications requiring settling times less than 150ns.

UNIPOLAR VOLTAGE OUTPUT CONNECTIONS AND CALIBRATION

The connections for unipolar +10V and +5V voltage output using external op amp and the internal span resistors are shown in Figure 2 and Figure 3, respectively.

CALIBRATION - UNIPOLAR

Step 1 Offset

Turn all bits off (all 0's)
Adjust R3 for zero volts output

Step 2 Gain

Turn all bits on (all 1's)
Adjust R1 for an output of FS -1 LSB
That is, adjust for:
9.96094V for 0V to +10V range
4.98047V for 0V to +5V range

UNIPOLAR - STRAIGHT BINARY
0V TO +10V OUTPUT RANGE

DIGITAL INPUT	ANALOG OUTPUT	
11 1	FS - 1 LSB	= 9.96094V
10 0	½FS	= 5.00000V
01 1	½FS - 1 LSB	= 4.96094V
00 0	Zero	= 0.00000V

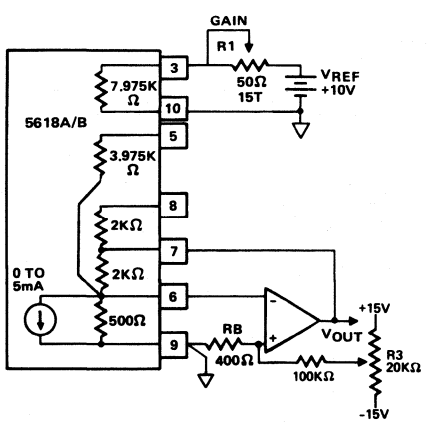


FIGURE 2

UNIPOLAR - STRAIGHT BINARY
0V TO +5V OUTPUT RANGE

DIGITAL INPUT	ANALOG OUTPUT	
11 1	FS - 1 LSB	= 4.98047V
10 0	½FS	= 2.50000V
01 1	½FS - 1 LSB	= 2.48047V
00 0	Zero	= 0.00000V

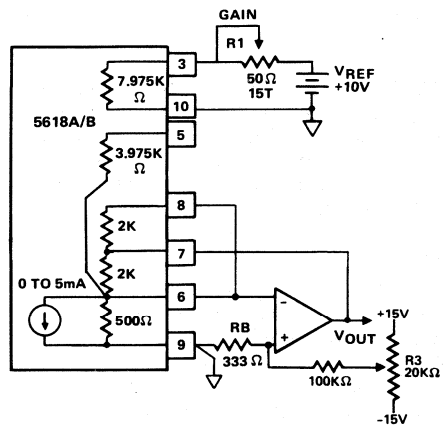


FIGURE 3

BIPOLAR VOLTAGE OUTPUT CONNECTIONS AND CALIBRATION

The connections for Bipolar ± 10V, ± 5V and ± 2.5V voltage output using an external op amp and the internal span resistors are shown in Figure 4, 5 and 6, respectively.

CALIBRATION - BIPOLAR

Step 1 Op Amp Null

Short op amp output to op amp - input
Adjust R3 for zero volts output

Step 2 Gain

Turn all bits on (all 1's) record output voltage
Turn all bits off (all 0's) record output voltage
Adjust R1 till the difference between the readings is equal to: 19.9219V for ±10V range
9.96094V for ± 5V range
4.98047V for ± 2.5V range

Step 3 Offset

Turn bit 1 (MSB) on, all other bits off (10 . . . 0)
Adjust R2 for zero volts output

BIPOLAR - OFFSET BINARY
±10V OUTPUT VOLTAGE RANGE

DIGITAL INPUT	ANALOG OUTPUT	
11 1	+FS -1 LSB	= +9.92188V
10 0	Zero	= +0.00000V
01 1	Zero -1 LSB	= -0.07813V
00 0	-FS	= -10.0000V

BIPOLAR - TWO'S COMPLEMENT **
±10V OUTPUT VOLTAGE RANGE

DIGITAL INPUT	ANALOG OUTPUT	
01 1	+FS - 1 LSB	= +9.92188V
00 0	Zero	= +0.00000V
11 1	Zero - 1 LSB	= -0.07813V
10 0	-FS	= -10.0000V

** Invert MSB with external inverter to obtain two's complement coding.

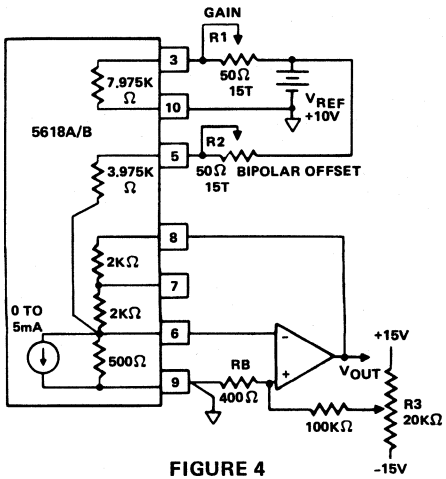


FIGURE 4

BIPOLAR - OFFSET BINARY
±5V OUTPUT VOLTAGE RANGE

DIGITAL INPUT	ANALOG OUTPUT	
11 1	+FS -1 LSB	= +4.96094V
10 0	Zero	= +0.00000V
01 1	Zero -1 LSB	= -0.03906V
00 0	-FS	= -5.00000V

BIPOLAR - TWO'S COMPLEMENT **
±5V OUTPUT VOLTAGE RANGE

DIGITAL INPUT	ANALOG OUTPUT	
01 1	+FS - 1 LSB	= +4.96094V
00 0	Zero	= +0.00000V
11 1	Zero - 1 LSB	= -0.03906V
10 0	-FS	= -5.00000V

** Invert MSB with external inverter to obtain two's complement coding.

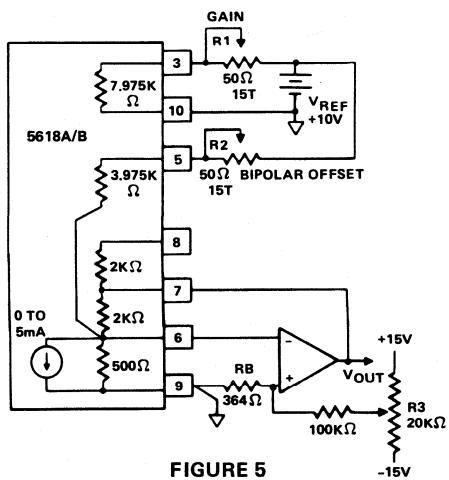


FIGURE 5

BIPOLAR - OFFSET BINARY
±2.5V OUTPUT VOLTAGE RANGE

DIGITAL INPUT	ANALOG OUTPUT	
11 1	+FS -1 LSB	= +2.48047V
10 0	Zero	= +0.00000V
01 1	Zero -1 LSB	= -0.01953V
00 0	-FS	= -2.50000V

BIPOLAR - TWO'S COMPLEMENT **
±2.5V OUTPUT VOLTAGE RANGE

DIGITAL INPUT	ANALOG OUTPUT	
01 1	+FS - 1 LSB	= +2.48047V
00 0	Zero	= +0.00000V
11 1	Zero - 1 LSB	= -0.01953V
10 0	-FS	= -2.50000V

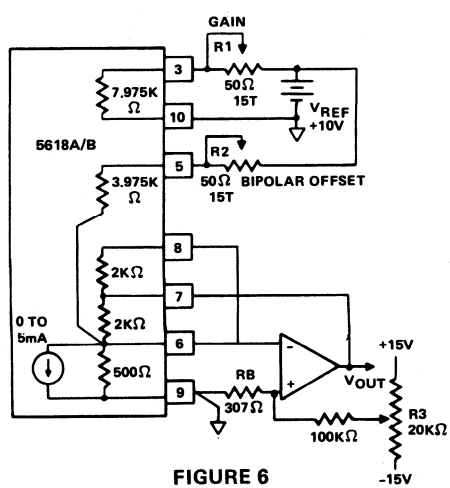


FIGURE 6

4

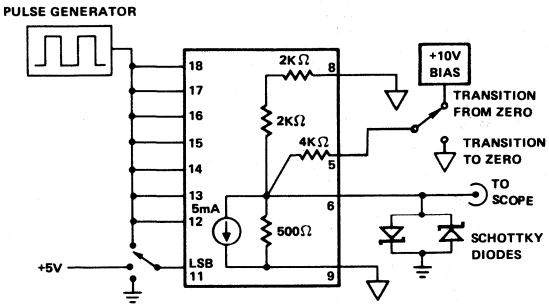


FIGURE 7. Settling time test circuit - High Impedance

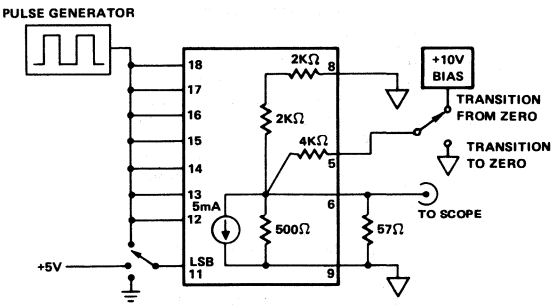
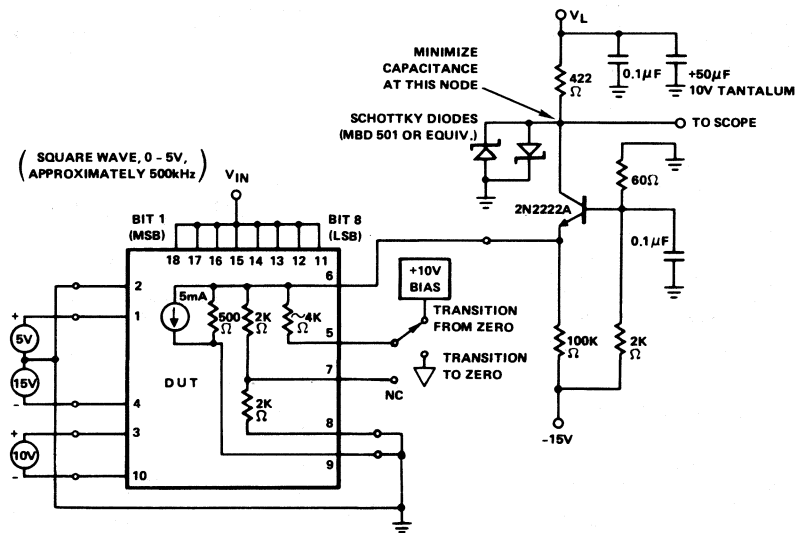


FIGURE 8. Settling time test circuit - 50Ω Load



NOTES:
1. Use oscilloscope with minimum 50MHz bandwidth.
2. Avoid saturation of scope pre-amp.

FIGURE 9. Settling time test circuit - Low Impedance

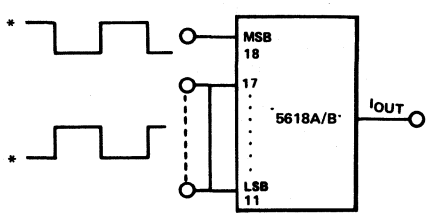


FIGURE 10

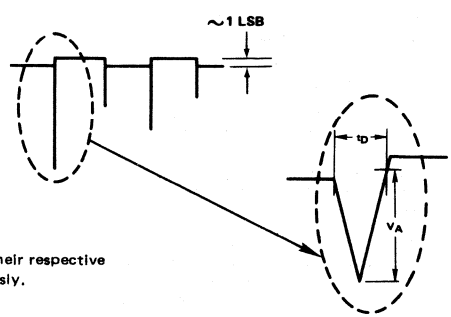


FIGURE 11

* Input drive signals should cross their respective switching thresholds simultaneously.

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HI-5900

Analog Data Acquisition Signal Processor

Preliminary

FEATURES

- 50kHz THOUGHPUT
- 12-BIT ACCURACY
- OUTPUT TRACK/HOLD AMPLIFIER
- DIFFERENTIAL INPUT CHANNELS
- SOFTWARE CONTROLLED GAIN AND CHANNEL SELECT
- 80dB CMRR
- COMPACT 32 PIN DIP
- MIL-STD-883 SCREENING AVAILABLE

APPLICATIONS

- HIGH PERFORMANCE DATA ACQUISITION
- MILITARY SYSTEMS

DESCRIPTION

The HI-5900 comprises "front end" components of a data acquisition system including an eight channel differential multiplexer, programmable gain instrumentation amplifier (PGA), and track and hold amplifier. Adding a timing circuit and A to D converter forms a complete data acquisition system. A minimum 50kHz channel-to-channel throughput rate is possible when the HI-5900 is used with a fast 12 bit A to D converter such as HARRIS' HI-5712.

Each output line of the input multiplexer is buffered by a high-quality non-inverting amplifier. This isolates each line from source resistance external to the 5900, preserving the high CMRR of the following instrumentation amplifier. Also, the buffers provide a high input impedance for each channel.

The PGA, which includes an op amp, monolithic resistor network and four channel differential multiplexer, offers precision gain values of 1, 2, 4, and 8. This voltage gain is selected by a two bit digital word. Output of the PGA drives the track and hold amplifier, and the low side of the PGA signal path is isolated by a third buffer amplifier, again to preserve the high CMRR in the PGA.

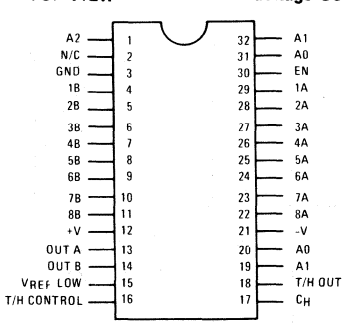
The output track/hold amplifier is a monolithic device, internally connected for non-inverting unity gain. In the sample mode it operates as a high performance buffer amplifier. With an external holding capacitor, it may be switched to HOLD with only 50ns aperture delay and 10pc of charge transfer.

The packaging technique involves monolithic chips mounted in leadless chip carriers (LCC's) and soldered to both sides of a multilayer ceramic substrate. Each LCC may undergo reliability screening such as MIL-STD-883, Method 5004/Class B, before assembly on the substrate. The resulting package is a compact 32 pin DIP; power requirements are ±15V.

The HI-5900 is offered as a high performance front-end section for military and industrial data acquisition systems. It is designed for interface with computers and is well suited for high-rel applications.

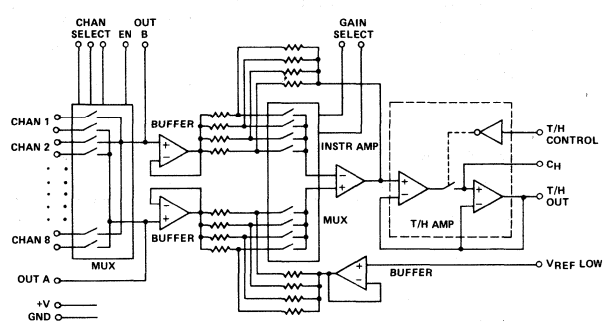
PINOUT

TOP VIEW — **Package Code MB**



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on page 1-4.

FUNCTIONAL DIAGRAM



4

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	30V	Output Current	Short Circuit Protected
Digital Input Overvoltage		Operating Temperature Range	
V_{Supply} (+)	+4V	HA-5900-5	$0^oC \leq T_A \leq +75^oC$
V_{Supply} (-)	-20V	HA-5900-2	$-55^oC \leq T_A \leq +150^oC$
Analog Input Overvoltage		Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$
V_{Supply} (+)	+20V	Internal Power Dissipation	650mW
V_{Supply} (-)	-20V		

ELECTRICAL CHARACTERISTICS

Unless otherwise specified: $V_S = +15V$; $C_H = 1000pF$; $V_{IH} = 4.0V$; $V_{IL} = 0.8V$

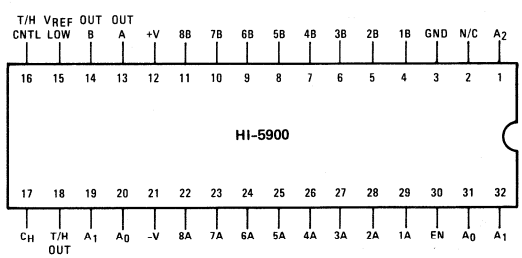
		HI-5900-2 -55°C to +125°C			HI-5900-5 0°C to +70°C			
PARAMETER	TEMP	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS, EACH CHANNEL								
Offset Voltage	+25°C		0.5			2.5		mV
	Full		1.0			3.0		mV
Bias Current	+25°C		80			80		nA
	Full		90			80		nA
Offset Current	+25°C		15			20		nA
	Full		30			30		nA
Common Mode Range	Full	±10			±10			V
Common Mode Rejection Ratio ($V_{CM} = \pm 10V$)	Full		85			85		dB
Digital Input Current (High or Low)	Full		1			1		μA
TRANSFER CHARACTERISTICS								
Small Signal Bandwidth (Gain = 1)	+25°C		2			2		MHz
Full Power Bandwidth (Gain = 1, $V_O = \pm 10V$)	+25°C		70			70		kHz
Slew Rate	+25°C		4			4		V/μs
Crosstalk (Sample Mode, Gain = 8, 1kHz 20Vp-p Input on all but Selected Channel)	+25°C		-80			-80		dB
"Off Isolation (Hold Mode, Gain = 1, 1kHz 20Vp-p Input)	+25°C		-80			-80		dB
Acquisition Time (Note 1), to 0.01%	+25°C		9			9		μs
OUTPUT CHARACTERISTICS								
Output Voltage Swing	Full	±10			±10			V
Output Current	+25°C	±10			±10			mA
Output Resistance	+25°C		5			5		Ω
Gain – Absolute Error 1	+25°C		.1			.1		%
2	+25°C		.1			.1		%
4	+25°C		.2			.2		%
8	+25°C		.2			.2		%
DYNAMIC CHARACTERISTICS								
t_{ON}, Enable (MUX)	+25°C		300			300		ns
t_{OFF}, Enable (MUX)	+25°C		300			300		ns
Droop Rate (T/H)	+25°C		1			1		V/μs
	Full		5			20		V/μs
Charge Transfer (T/H)	+25°C		10			10		pc
Aperture Delay (T/H)	+25°C		100			100		ns
Aperture Uncertainty (T/H)	+25°C		5			5		ns
POWER SUPPLY CHARACTERISTICS								
I+	Full		8.5			8.0		mA
I-	Full		6.5			6.0		mA
Power Supply Rejection Ratio, V+	Full		90			90		dB
Power Supply Rejection Ratio, V-	Full		100			100		dB

Note 1: Acquisition Time is defined for a change of channel (+10V on chan.1 to 0V on chan. 8) with simultaneous change from HOLD to TRACK mode. Gain = 1.

PIN	SYMBOL	DESCRIPTION
4	1B	Non-Inverting Side of the Eight Differential Input Channels
5	2B	
6	3B	
7	4B	
8	5B	
9	6B	
10	7B	
11	8B	
29	1A	Inverting Side of the Eight Differential Input Channels
28	2A	
26	4A	
25	5A	
24	6A	
23	7A	
22	8A	
31	A_0	Digital Channel Select Inputs*
32	A_1	
1	A_2	
20	A_0	Digital Gain Select Inputs*
19	A_1	

PIN	SYMBOL	DESCRIPTION
16	T/H CONTROL	Track/Hold Mode Select*
2	NC	No Connection
3	GND	Signal and Power Ground
12	+V	Positive Supply (+15V)
21	-V	Negative Supply (-15V)
18	T/H OUT	Output of the HI-5900
17	C_H	Hold Capacitor Connection
15	V_{REF} LOW	Reference for the Output on Pin 18
13	OUT A	"A" Output of the Input Multiplexer (Inverting Side of each Channel)
14	OUT B	"B" Output of the Input Multiplexer (Non-Inverting Side of each Channel)
30	EN	Enable Strobe for the Input Multiplexer; Normally Wired High. EN may be used in Conjunction with OUT A and OUT B, to Poll Additional Channels through an External Multiplexer.

* See Programmable Functions



PROGRAMMABLE FUNCTIONS

Input Codes are as follows:

X = DON'T CARE
0 = $V_{IN} \leq +0.8V$;
1 = $V_{IN} \geq +4.0V$, where V_{IN} is the digital input voltage.

1. T/H Control (PIN 16)

0	Track
1	Hold

2. Gain Select

A_0 (PIN 20)	A_1 (PIN 19)	GAIN
0	0	1
0	1	2
1	0	4
1	1	8

3. Channel Select

A_0 (PIN 31)	A_1 (PIN 32)	A_2 (PIN 1)	EN (PIN 30)	CHANNEL
X	X	X	0	None
0	0	0	1	0
0	0	1	1	1
0	1	0	1	2
0	1	1	1	3
1	0	0	1	4
1	0	1	1	5
1	1	0	1	6
1	1	1	1	7

PERFORMANCE CURVES

ACQUISITION TIME vs. OUTPUT STEP CHANGE

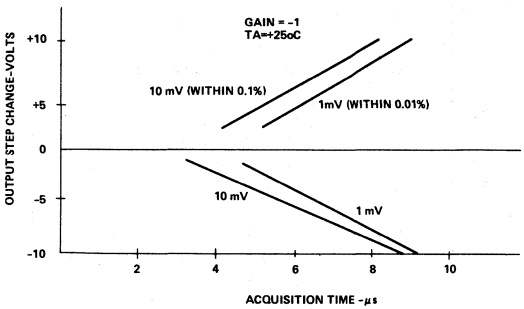


FIGURE 1

INPUT VOLTAGE NOISE vs. FREQUENCY

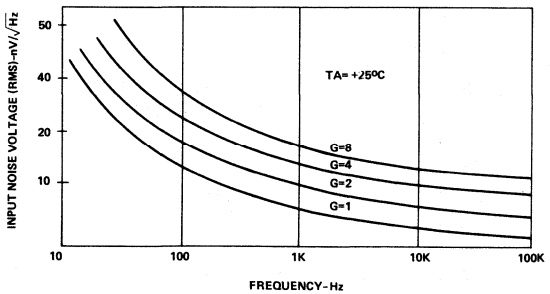


FIGURE 2

TYPICAL T/H AMPLIFIER PERFORMANCE vs. HOLD CAPACITANCE Ch

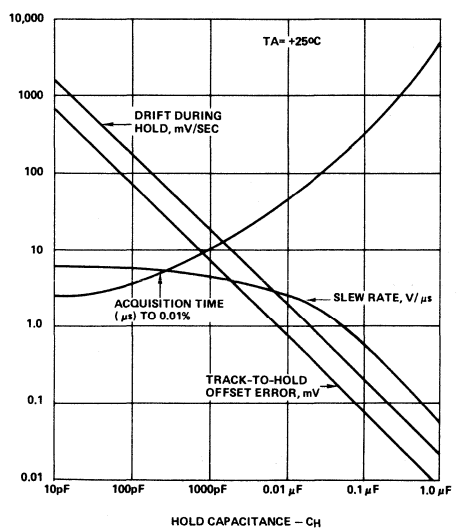


FIGURE 3

INPUT LEAKAGE, BIAS & OFFSET CURRENT vs. TEMPERATURE

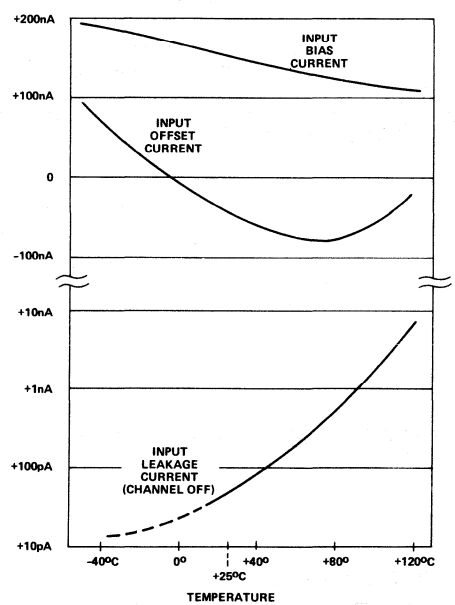


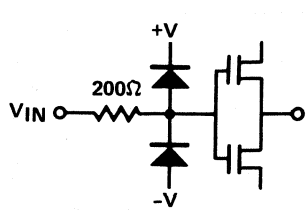
FIGURE 4

APPLYING THE HI-5900

GENERAL CONSIDERATIONS

The HI-5900 was designed to provide a versatile front-end section for a data acquisition system. Both hardwired and computer-controlled systems may be implemented in a variety of configurations. The following general considerations and precautions should be observed.

1. HANDLING – Each digital input is protected by a resistor-diode network, to minimize failures due to static discharge through the MOS gate:



For additional protection, it is wise to observe all of the proper shipping and handling procedures customary for CMOS devices.

2. POWER SUPPLY CONNECTIONS – Each of the four active chips in the HI-5900 are bypassed to ground by internal .01 μF capacitors. These eight nonpolarized capacitors prevent high frequency variations in the supply voltage.

   To bypass lower frequencies, connect a polarized capacitor from the ground pin to each supply pin, with value from 10μF to 50μF.

3. LAYOUT

   A. Distributed capacitance between signal paths external to the HI-5900 is a major source of crosstalk. Within the HI-5900, careful substrate design and packaging have ensured that "static" crosstalk will not exceed -80dB. ("Static") refers to the absence of channel-to-channel switching. Thus, a maximum of 2mV p-p can feed into a selected channel, from 20V p-p applied to one or more OFF channels.)

   When a multiplexer is continuously cycled from channel to channel, two other forms of crosstalk arise. These are dynamic crosstalk and adjacent* channel crosstalk, which are both minimized along with static crosstalk by careful attention to circuit board layout. A strip of ground plane should separate conductors for adjacent channels on a printed circuit board. See Fig. 5. Make these traces (and the conductors) short, and as narrow as practical for maximum separation.

   *Adjacent in time – for example, channels 1 and 8 may occupy adjacent time slots during time – division multiplexing.

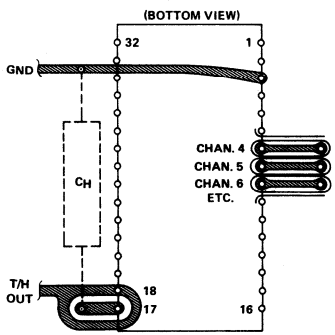


FIGURE 5
HI-5900 GUARD RING LAYOUT

   B. The holding capacitor C_H is the only essential external component required for operation of the HI-5900. The value selected determines droop rate, offset error and acquisition time according to curves shown in Fig. 3. Board layout should include a guard ring to prevent voltage-driven leakage at the capacitor terminal. See Fig. 5.

   For minimum droop error in the HOLD mode, choose a capacitor with high insulation resistance and low dielectric absorption. Since type of dielectric is the best performance indicator for hold capacitor applications, consider these guidelines: Teflon is best (especially at high temperature) but the most expensive. In descending order of choice, polystyrene, polypropylene, and polycarbonate are all acceptable. Least acceptable are ceramic and mica, which can allow several percent of change in the held voltage due to dielectric absorption (vs. .01% for the other types).

OFFSET ADJUSTMENT

The V_{REF} LOW input (pin 15) is a convenient point for nulling any DC offset voltage in an HI-5900 system. This can be done with a simple manual trim:

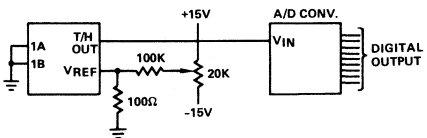


FIGURE 6

With zero volts on the selected input channel, the HI-5900 output (T/H OUT) may be adjusted to zero. If the system includes an A to D converter, net DC offset may be nulled by adjusting the converter's digital output to zero. In either case, readjustment is required after a change in temperature or a change in the HI-5900 gain. The need for readjustment may be eliminated by using an auto-zero circuit as shown in Fig. 7.

The offset at V_O is driven to zero by application of a voltage at V_{REF} LOW, opposite in sign and with magnitude (G + 1) V_O, where G is the digitally selected gain. This voltage is updated each time channel 8 is addressed. Since channel 8 is chosen for the zero (ground) reference input, the SN7420 decoder output is wired to go low only when channel 8 is addressed. The HA-2420 track/hold amplifier acquires a new sample of the offset at V_O during this interval. This sample is of opposite sign to V_O and approximately 100X (G + 1) in magnitude, due to the 10K/100Ω attenuator. Storing 100X the actual correction value minimizes the percent droop error during hold. Finally, OFFSET TRIM is used to remove any residual offset at V_O, introduced by the HA-2420.

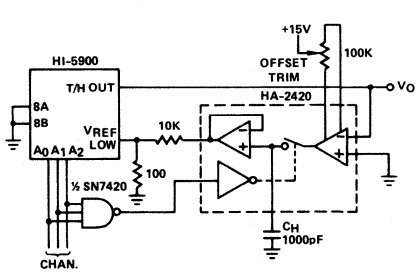


FIGURE 7

TIMING AND CONTROL

The HI-5900 is intended to operate with a fast A to D converter such as HARRIS' 12 bit HI-5712. A single monostable (one-shot) multivibrator such as half of the dual SN74123 provides the necessary timing and control:

The pulse rate at $\overline{Q}$ is equal to the conversion rate of the A to D converter, since the one-shot is driven by the converter's STATUS output. Polarity of the Q output is correct for initiating a conversion each time the HI-5900 returns to the HOLD mode. For maximum channel-to-channel throughput rate, the $\overline{Q}$ pulse duration (determined by R and C) may be set equal to the HI-5900 acquisition time.

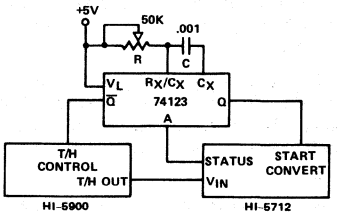


FIGURE 8

ABSOLUTE MAXIMUM RATINGS

As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Characteristics" are the only conditions recommended for satisfactory operation.

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HC-55516/55532

All-Digital Continuously Variable Slope Delta Modulator (CVSD)

FEATURES

- REQUIRES FEWER EXTERNAL PARTS
- LOW POWER DRAIN: 6mW FROM SINGLE 5V-7V SUPPLY
- TIME CONSTANTS DETERMINED BY CLOCK FREQUENCY; NO CALIBRATION OR DRIFT PROBLEMS; AUTOMATIC OFFSET ADJUSTMENT
- HALF DUPLEX OPERATION BY DIGITAL CONTROL
- FILTER RESET BY DIGITAL CONTROL
- AUTOMATIC OVERLOAD RECOVERY
- AUTOMATIC "QUIET" PATTERN GENERATION
- AGC CONTROL SIGNAL AVAILABLE

APPLICATIONS

- VOICE TRANSMISSION OVER DATA CHANNELS
- VOICE ENCRYPTION/SCRAMBLING
- VOICE I/O FOR DIGITAL SYSTEMS
- AUDIO MANIPULATIONS: DELAY LINES, TIME COMPRESSION, ECHO GENERATION/ SURPRESSION, SPECIAL EFFECTS, ETC.

DESCRIPTION

The HC-55516 and HC-55532 are half duplex modulator/ demodulator CMOS integrated circuits used to convert voice signals into serial NRZ digital data, and to reconvert that data into voice. The conversion is by delta modulation, using the continuously variable slope (CVSD) method of companding.

While signals are compatible with other CVSD circuits, internal design is unique. The analog loop filters have been replaced by digital filters, using very low power, and requiring no external timing components. This approach allows inclusion of many desirable features which would be difficult to implement using other approaches.

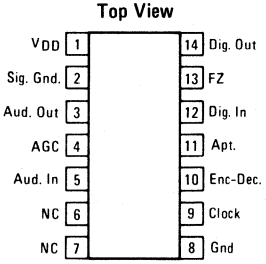
The HC-55516 has internal time constants optimized for 16K bits/sec data rate and is usable down to 9K bits/sec. The HC-55532 is optimized for 32K bits/sec and is usable beyond 64K bits/sec. Both units are available in 14 pin D.I.P. (HC1) in two temperature ranges; -55°C to +125°C (-2 or-8) and -40°C to +85°C (-9).

PINOUT

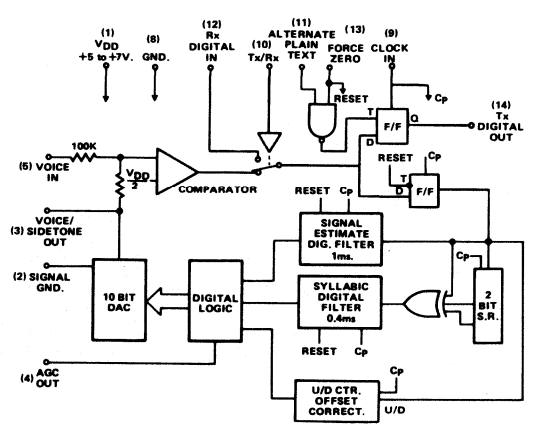
Package Code 4Q

14 PIN D.I.P.

Top View



FUNCTIONAL DIAGRAM



PIN # 14-LEAD F.P. & D.I.P.	SYMBOL	ACTIVE* LEVEL	DESCRIPTION
1	V_{DD}		Positive supply voltage.
2	Sig. Gnd.		Ground connection to D/A ladders and comparator; i.e. audio ground.
3	Aud. Out		Recovered audio out. May be used as side tone at the transmitter. Presents approximately 100 kilohm source. Zero signal reference is $V_{DD}/2$.
4	AGC		A logic "Low" level will appear at this output when the recovered signal excursion reaches one-half of full scale value.
5	Aud. In		Audio input. Should be externally AC coupled. Presents approximately 100 kilohms in series with $V_{DD}/2$.
6,7			No internal connection is made to these pins.
8	Gnd.		Logic ground. Negative supply voltage.
9	Clock		Receiver clock must be phased with digital input such that data must be present at the positive clock transition.
10	Encode (Decode)	Low (High)	A single CVSD can provide half-duplex operation. The encode and decode functions are selected by the logic level applied to this input. A low level selects the encode mode, a high level, the decode mode.
11	APT.	Low	Activating this input causes an "alternate plain text" (quieting pattern) to be transmitted without affecting the internal operation of the CVSD.
12	Dig. In		Input for the received digital data.
13	FZ	Low	Activating this input forces the transmitted output, the internal logic, and the recovered audio output into the "quieting" condition.
14	Dig. Out		Output for transmitted digital data.

*Note: No active input should be left in a "floating condition".

ABSOLUTE MAXIMUM RATINGS

Voltage At Any Pin	-3.0V to V_{DD} +0.3V	Operating Temperature (-9)	-40°C to +85°C
Maximum V_{DD} Voltage	+7.0V	(-2)	-55°C to +125°C
		(-8)	-55°C to +125°C
		Storage Temperature	-65°C to +150°C

ELECTRICAL CHARACTERISTICS @ T_A = 25°C

Test Conditions V_{DD} = 6.0V, Bit Rate = 16Kb/s, (HC-55516)
Bit Rate = 32Kb/s, (HC-55532)

PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
Clock Bit Rate		16/32	64	Kb/s	(1)
Clock Duty Cycle	30		70	%	
Supply Voltage	+5.0		+7.0	V	
Supply Current		1.0		mA	
Digital "1" Input		4.5		V	(2)
Digital "0" Input		1.5		V	(2)
Digital "1" Output		5.5		V	(3)
Digital "0" Output		0.5		V	(3)
Audio Input Voltage		0.5	1.4	Vrms	(4)
Audio Output Voltage		0.5	1.4	Vrms	(5)
Audio Input Impedance		100		KΩ	(6)
Audio Output Impedance		100		KΩ	(7)
Transfer Gain	-0.5		+0.5	dB	(8)
Syllabic Time Constant		4.0		mS	(9)
L.P. Filter Time Constant (55516) (55532)		0.94 0.47		mS mS	(9)
Step Size Ratio (55516) (55532)		24 18		dB dB	(10)
Resolution (55516) (55532)		0.1 0.2		% %	(11)
Min. Step Size (55516) (55532)		0.2 0.4		% %	(12)
Slope Overload		Fig. 1			(13)
Signal/Noise Ratio			Tab. 1		(14)
Quieting Pattern Amplitude (55516) (55532)		12 24		mV P-P mV P-P	(15)
AGC Threshold		0.5		F.S.	(16)
Clamping Threshold		0.75		F.S.	(17)

1. There is one NRZ (Non-Return Zero) data bit per clock period. Clock must be phased with digital data such that data must be present at the positive clock transition.

2. Logic inputs are CMOS compatible at supply voltage and are diode protected. Digital data input is NRZ at clock rate.

3. Logic outputs are CMOS compatible at supply voltage and withstand short-circuits to V_{DD} or ground. Digital data output is NRZ and changes with negative clock transitions.

4. Recommended voice input range for best voice performance.

5. May be used for side-tone in encode mode.

6. Should be externally AC coupled. Presents 100 Kilohms in series with $V_{DD}/2$.

7. Presents 100 Kilohms in series with recovered audio voltage. Zero-signal references is $V_{DD}/2$.

8. Unloaded, for linear signals.

9. Note that filter time constants are inversely proportional to clock rate.

10. Step size compression ratio of the syllabic filter is defined as the ratio of the filter output, with an equal 1-0 bit density input to the filter, to its minimum output.

11. Minimum quantization voltage level expressed as a percentage of supply voltage.

12. The minimum step size between levels is twice the resolution.

13. For large signal amplitudes or high frequencies, the encoder may become slope-overloaded. Figure 1 shows the frequency response at various signal levels,measured with a 3kHz low-pass filter having a 130dB/octave roll-off to -50dB. See Table II.

14. Table I shows the SNR under various conditions, using the output filter described in 13 (above) at a bit rate of 16Kb/s. See Table II.

15. The "quieting" pattern or idle-channel audio output steps at one-half the bit rate, changing state on negative clock transitions.

16. A logic "0" will appear at the AGC output pin when the recovered signal reaches one-half of full-scale value (positive or negative).

17. The recovered signal will be clamped, and the computation will be inhibited, when the recovered signal reaches three-quarters of full-scale value, and will unclamp when it falls below this value (positive or negative).

TABLE I

INPUT FREQUENCY Hz	INPUT AMPLITUDE mV RMS	OUTPUT SNR dB MIN.
300	1400	20
300	45	15
1000	500	14
1000	16	9

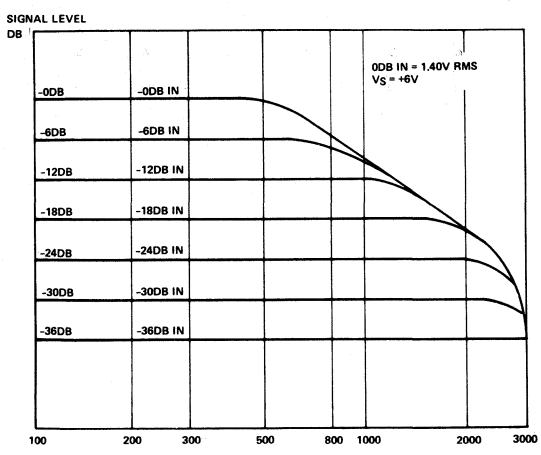


Figure 1 — Transfer Function on CVSD at 16KB

TABLE II

INPUT FILTER FREQUENCY RESPONSE		OUTPUT FILTER FREQUENCY RESPONSE	
FREQUENCY	RELATIVE OUTPUT	FREQUENCY	RELATIVE OUTPUT
100Hz	0±0.5dB	100Hz to 1500Hz	0±1.5dB
200Hz	0±0.1dB	1500Hz to 3000Hz	0±2.5dB
1000Hz	0±0.1dB	3800Hz to 100KHz	Less Than -45dB
3000Hz	-3±0.5dB		
9000Hz	-20±2.0dB		

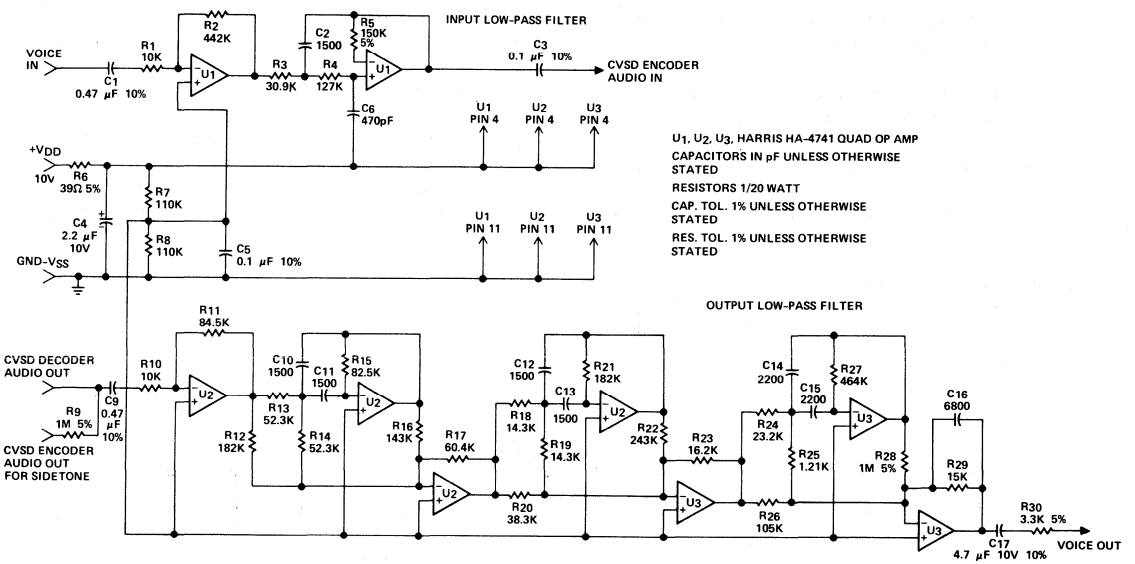


Figure 2 – Suggested Input/Output Audio Filters for SNR Measurement

NOTE: An output filter similar to the input filter section above will generally suffice for good voice intelligibility.

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HD-0165

Keyboard Encoder

FEATURES

- STROBE OUTPUT
- KEY ROLLOVER OUTPUT
- EXPANDABLE: 2 PACKAGES REQUIRED FOR FULL TELETYPEWRITER, EIGHT-BIT ENCODING
- SINGLE +5.0V SUPPLY REQUIRED
- DTL/TTL OUTPUTS
- MONOLITHIC RELIABILITY

APPLICATIONS

- MICROPROCESSOR DATA ENTRY (16 KEY TO HEX CODE)
- BCD DATA ENTRY
- TYPEWRITER TYPE KEYBOARDS
- CONTROL PANELS

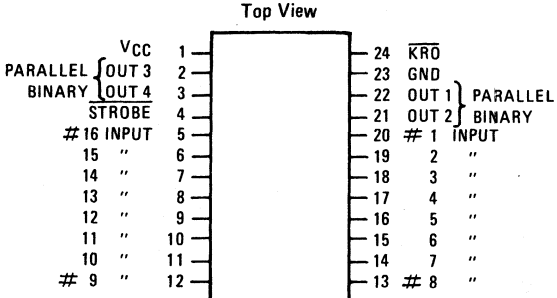
DESCRIPTION

The HD-0165 Keyboard Encoder is a 16 line to four-bit parallel encoder intended for use with manual data entry devices such as calculator or typewriter keyboards. In addition to the encoding function, there is a Strobe output and a Key Rollover output which energizes whenever two or more inputs are energized simultaneously. Any four-bit code can be implemented by proper wiring of the input lines. Inputs are normally wired through the key switches to the +5.0V power supply. Full typewriter keyboard encoding up to eight bits can be accomplished with two Encoder circuits by the use of double pole key switches or single pole switches with two isolation diodes per key. Outputs will interface with all popular DTL and TTL logic families. The circuit is packaged in a hermetic 24-pin dual-in-line package and operates over the temperature range of 0°C to +75°C.

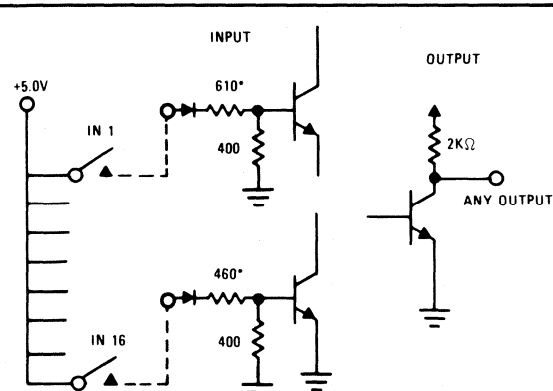
PINOUT

Package Code 4K

Top View



EQUIVALENT CIRCUITS



* EQUIVALENT RESISTORS FOR OTHER INPUTS ARE BETWEEN THESE TWO VALUES

5

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+7.0V	Output Current	30mA
Input Voltage	+5.5V	Storage Temperature	-65^{o} to $+150^{o}C$
Output Voltage	+5.5V	Operating Temperature (Case)	$0^{o}C$ to $+75^{o}C$

ELECTRICAL CHARACTERISTICS

Test Conditions: $V_{CC} = +5.0V \pm 5\%$
$T_{Case} = 0^{o}C$ to $+75^{o}C$
Unless otherwise specified

	PARAMETER	SYM.	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS
D.C.	Input Current "1"	I_{IH}			17	mA	$V_{IN} = +5.0V$
D.C.	Output Voltage "0"	V_{OL}		+0.2	+0.4	V	$V_{IH} = +4.5V$ $I_{OL} = 10mA$
D.C.	Output Voltage				+0.4		$V_{IH} = +3.5V$ $I_{OL} = 3.2mA$
D.C.	Output Voltage "1"	V_{OH}	+2.4	+4.0			V_{IL} = Open Circuit, $I_{OH} = -240\mu A$
D.C.	Power Supply Current Operating	I_{CC}			52	mA	One Input at +5.25V
D.C.	Power Supply Current Maximum	I_{CCM}			88	mA	All Inputs at +5.25V
A.C.	Skew Time (Note 1)	T_{SK}		80	200	ns	$T_{Case} = 25^{o}C$, $V_{CC} = V_{IN} = +5.0V$, $C_L < 50pF$

NOTE: (1) Skew time is the maximum time differential between propagation delay times of any outputs including $\overline{\text{strobe}}$ and $\overline{K_{RO}}$.

TRUTH TABLE

INPUTS 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	OUTPUTS 1	2	3	4	$\overline{St.}$	$\overline{K_{RO}}$
L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H
H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	L	H
L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	L	H
L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	H	H	L	H
L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	L	H
L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	H	H	L	H	L	H
L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	H	L	H	L	H
L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	H	L	L	H	L	H
L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	H	L	H
L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	H	H	H	L	L	H
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L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	H	L	L	H
L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	H	H	L	L	L	H
L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	H	L	L	L	H
L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	H	L	L	L	L	H
L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	H
ANY TWO OR MORE HIGH																X	X	X	X	L	L

INPUTS: L = Open Circuit or < +1.0V H = > +4.5V Current Source
OUTPUTS: L = < +0.4V H = > +2.4V X = Erroneous Data

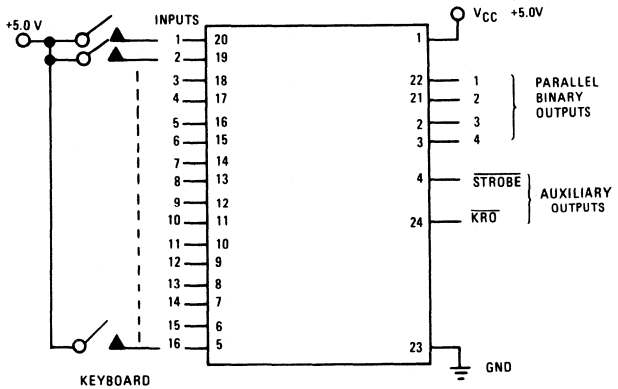


Figure 1. GENERAL CONFIGURATION FOR ENCODING TWO TO SIXTEEN KEYS

The Truth Table is used to determine wiring from the key switches to Encoder inputs to produce desired output codes.

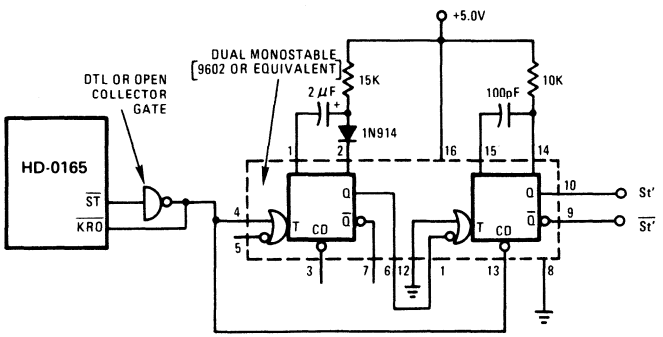
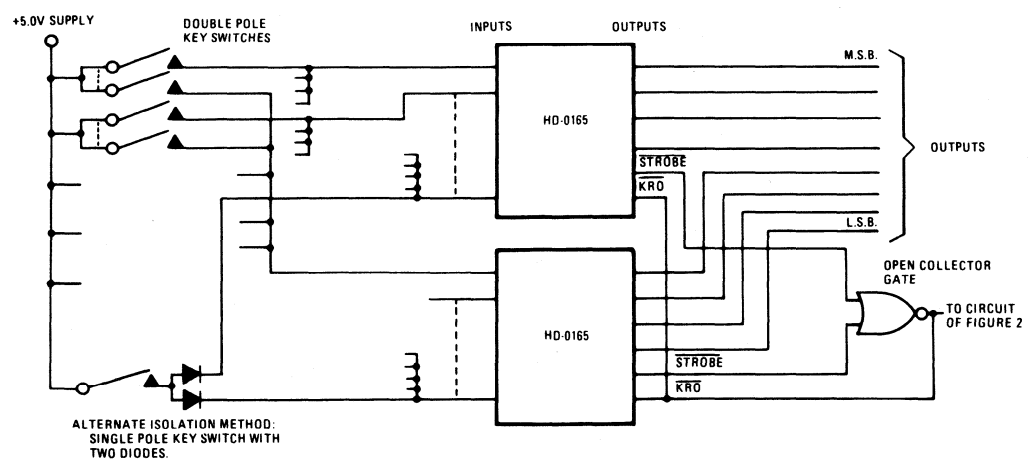


Figure 2. SWITCH BOUNCE ELIMINATION

This circuit generates a delayed Strobe pulse (St'). Delay time is determined by first monostable and should be about 10ms. Pulse width is determined by second monostable and should be set according to system requirements. Effect of switch bounce or arcing on make or break is positively eliminated and proper encoding will take place under two key rollover conditions.



NOTE: *Reduce Encoder fanout to two TTL loads maximum.*

Figure 3. ENCODING UP TO 256 KEYS

Use upper Encoder to produce the four most significant output bits; the lower to produce the least significant bits. Use Truth Table and required output codes to determine wiring from each key to the two Encoders.

SHIFT and CONTROL functions can be implemented by logic gates in series with the output lines.

Analog Application Notes

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APPLICATION NOTE 502

HA-909 OPERATIONAL AMPLIFIERS PERFORMANCE TAILORING

BY DON JONES

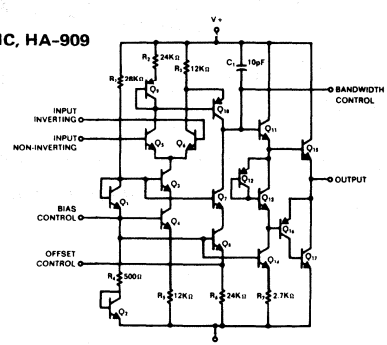
INTRODUCTION

In most applications, the HA-909 operational amplifier family will approach the theoretical "ideal" op amp requiring only connections to the power supplies and to feedback components determined from classical analog computer theory. This results from the exceptionally wide bandwidth of the HA-909 combined with internally compensated 6 dB per octave frequency rolloff and high impedance, low drift, low noise input characteristics.

Nevertheless, in the unlimited number of possible operational amplifier applications, there are those in which certain performance factors may need to be optimized. These performance factors include offset, power dissipation, bandwidth, large signal bandwidth, slew rate, transient response, and stability with reactive loads. The Harris HA-909 combines a design which minimizes the necessity for added external components with the availability of internal circuit points which allow the altering of performance characteristics.

The schematic of the HA-909 family is shown in Figure 1. The circuit nodes connected to the device pins on the HA-909 for performance tailoring are the Offset Control, the Bandwidth Control, and the Bias Control. The HA2-909, an 8-lead metal can version, has only the Bandwidth Control available.

FIGURE 1.
SCHEMATIC, HA-909



OFFSET ADJUSTMENT

In many applications, the guaranteed offset voltage of the HA-909 family is sufficiently small that no connection to the offset control pin is required. In some high precision or high gain DC amplifier applications, it may be desired to set the room temperature offset voltage to zero. Figure 2 shows the proper connection of a single 200K ohm potentiometer to accomplish this. Selected fixed resistors in a voltage divider circuit could also be used; the upper leg between the bias control pin and the offset control pin could be a fixed value of about 120K ohms and the lower leg between the offset control pin and -V could be a value usually between 50K and 100K ohms selected to yield zero offset.

Figure 3 shows offset voltage change with temperature for one unit with and without room temperature offset zeroing. These curves should not be regarded as "typical" since offset can be of either polarity and the temperature slope can be in either direction. In general, room temperature zeroing of offset voltage results in lower temperature coefficients of offset voltage.

FIGURE 2.
OFFSET ADJUSTMENT, HA-909

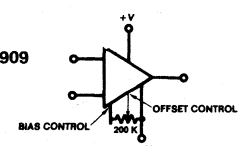
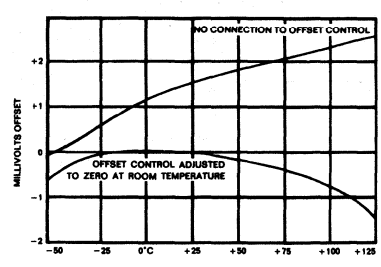


FIGURE 3.
OFFSET VOLTAGE vs. TEMPERATURE



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BANDWIDTH ADJUSTMENT

A unique feature of the HA-909 family of operational amplifiers is wide bandwidth (typically 7 MHz) combined with internal compensation for 6 dB per octave rolloff. This assures stable operation at any gain with resistive loads, plus superior transient response and full power bandwidth.

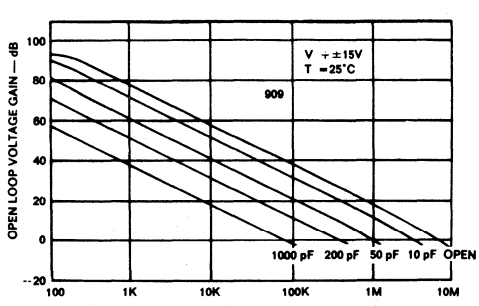
In certain instances, such as when driving reactive loads or when the amplifier is part of a servo loop, it may be desirable for stability to reduce the bandwidth while maintaining the 6 dB per octave rolloff characteristic. Also, in certain systems, it may be desirable to attenuate frequencies above a certain value or to limit transient response.

Connection of a capacitor from the bandwidth control pin to ground will move the first break point on the open loop frequency response curve to a lower frequency while retaining the 6 dB per octave rolloff (Figure 4).

The effective built in capacitance is about 10 pF, so the new bandwidth with external capacitance connected is approximately $Bw = Bwo \times \frac{10}{C+10}$; where Bwo is the bandwidth without external capacitance and C is the external capacitance in pF. Slew rate and full power bandwidth will be reduced by the same factor as the bandwidth.

The Bandwidth Control pin may also be used to limit the output swing by connecting diodes at this point to reference voltages. This pin is a high impedance point which carries the same voltage swing as the output pin offset by about +1.5 volts.

FIGURE 4.
OPEN LOOP FREQUENCY RESPONSE



FREQUENCY RESPONSE VS. CAPACITANCE FROM BANDWIDTH CONTROL PIN TO GROUND.

BIAS CONTROL ADJUSTMENT

Bias Control refers to control of internal device quiescent currents and should not be confused with the Input Bias Current parameter.

Referring to the HA-909 schematic in Figure 1, the current in all stages of the amplifier is determined by the resistor-diode string consisting of R1, Q1, R4, and Q2. The impedance at the collector of Q10 which drives the rolloff capacitor, C1, is directly proportional to the current through R4 and Q2. This current is approximately 1.0 mA at supply voltage of ±15 volts; 0.65 mA at ±10 volts; or 1.35 mA at ±20 volts. As a result, the bandwidth and slew rate measured with supplies of ±20 volts are nearly double the values measured at ±10 volts. It is possible to control bandwidth, slew rate, and to some extent open loop gain by adding or subtracting current through R4 and Q2 by connecting a resistor from the supply voltage to the Bias Control pin.

Adding bias control current by connecting a resistor between the positive supply and the Bias Control pin may be desirable to achieve maximum bandwidth or slew rate, particularly when supply voltages less than ±15 volts must be utilized. Reducing bias control current by connecting a resistor between the negative supply and the bias control pin has much the same effect as adding capacitance to the Bandwidth Control pin but may be desirable to minimize power supply current.

Figure 5 shows the change in D. C. open loop gain with supply voltage and external bias control current normalized to the gain measured at ±15 volt supplies and the Bias Control pin open.

FIGURE 5.
OPEN LOOP GAIN WITH BIAS CURRENT

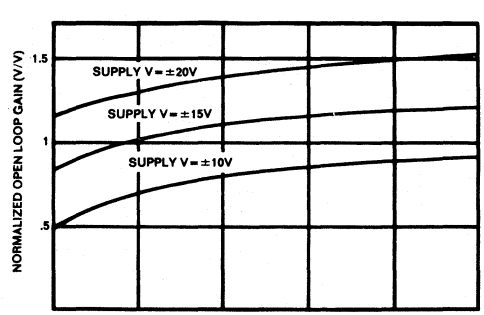


FIGURE 6.
OTHER PARAMETER CHANGES WITH BIAS CURRENT

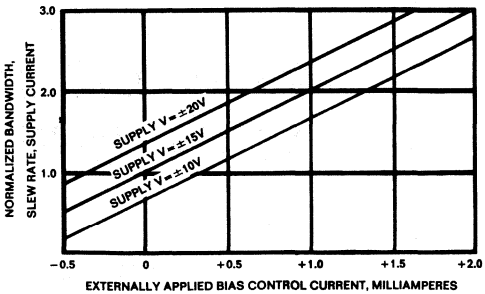
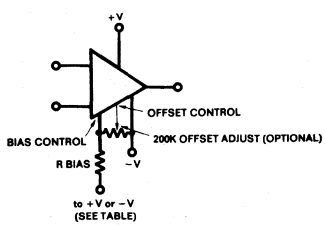


Figure 6 refers to changes in slew rate, bandwidth, large signal bandwidth for a fixed output level, and power supply current with respect to changes in supply voltage and external bias control current. These curves are normalized with respect to the parameters measured at ±15 volt supplies and the Bias Control pin open. It can be seen that these parameters can be increased to those normal at a higher supply voltage by adding bias control current; 0.35 mA added at ±10 volts brings the performance up to the normal 15 volt level and 0.35 mA added at ±15 volts brings the performance up to the normal 20 volt level.

Obviously the maximum output voltage swing cannot be increased by adding bias control current, but actually tends to decrease by about 1 volt at 2 mA bias control current. Bias control currents from 2 to 5 mA increase the parameters even more but instability at unity gain may result from reduced phase margin.

Figure 7 shows the typical external resistance required for various bias control currents at different supply voltage levels.

FIGURE 7.



BIAS RESISTOR SELECTION

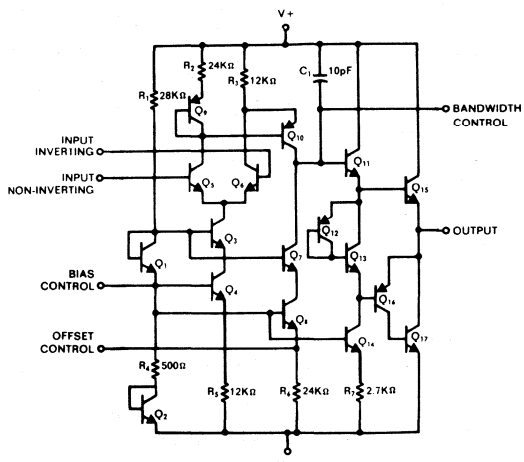
External Bias Current mA	Connect R Bias to:	R Bias In Ohms At Supply Voltage: ±10V	±15V	±20V
−0.5	−V	1.7K	2K	2.4K
+0.5	+V	39K	57K	77K
+1.0	+V	18K	28K	38K
+1.5	+V	12K	21K	27K
+2.0	+V	9K	14K	19K

CONCLUSION

For most applications, no connections are required at the Offset, Bandwidth, or Bias Control pins; they are simply terminated at an isolated solder pad on the PC Card.

The versatility provided by these control points allows the HA-909 to be used in many special applications so that a single op amp type can be used for virtually all op amp requirements in a system.

HA-909 SCHEMATIC



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APPLICATION NOTE 505

A HIGH IMPEDANCE HYSTERESIS CIRCUIT

BY G. G. MILER

A hysteresis amplifier is often needed for Schmitt triggers, analog simulation, differential comparators, and for servomechanisms. Frequently the hysteresis amplifiers used in these circuits are required to have a high input impedance and a low input current to avoid disturbing the input signal. The threshold voltages should be independent of the signal source impedances.

The input current introduces an error in the thresholds, which is equal to the product of the input current and the source resistance. The hysteresis circuit uses positive feedback from the output to the noninverting input of the operational amplifier. Coupling between the output and the source through the input resistance of the operational amplifier can cause multiple triggering unless the differential input resistance of the operational amplifier is large compared with the source resistance. An input impedance of 100 megohms and a bias current of 2 nanoamperes is obtainable with modern high impedance operational amplifiers.

It is frequently necessary to limit the output swing to some convenient levels, such as standard logic levels. The output voltage of current limited devices can be clamped; however, this will create an unnecessary amount of power dissipation.

The output voltage of the circuit can also be limited by using a series resistor between the operational amplifier and a clamp. In this case, the output of the operational amplifier is allowed to swing through its full range. However, this will limit the available output current and will require additional switching time for the output to slew through its full range. On the HA-2520 or HA-2620 the output voltage can be limited by placing a clamp at the bandwidth control point. The bandwidth control point is a high impedance point, which is at the same voltage as the output.

Figure 1 shows a simple hysteresis circuit in which the output voltage is clamped at the bandwidth control point. Let the thresholds, E_T, be defined by:

$$(1) \quad E_T = E_{10} \pm \frac{\Delta E_1}{2}$$

Where E_{10} is the input threshold offset voltage. The output voltage limits are E_0, defined by:

$$(2) \quad E_0 = E_{00} \pm \frac{\Delta E_0}{2}$$

Where E_{00} is the output offset. The total threshold offset, E_{TO} is defined as:

$$(3) \quad E_{TO} = E_{00} - E_{10}$$

The voltage at the noninverting input, E_1, is given by:

$$(4) \quad E_+ = \frac{R_1}{R_1 + R_2} E_0$$

The threshold of the hysteresis circuit occurs when E_- is equal to E_+. It can be shown that:

$$(5) \quad \Delta E_+ = \frac{R_1}{R_1 + R_2} \Delta E_0$$

Since ΔE_I is equal to ΔE_+ it is obvious that R_1 can be found by:

$$(6) \quad R_1 = \frac{\Delta E_I}{\Delta E_0} (R_1 + R_2)$$

$R_1 + R_2$ is chosen to be some convenient resistance.

The next step is to calculate the reference voltage, E_R. R_1 and R_2 form a voltage divider between E_R and E_0. Therefore, the reference voltage can be calculated by:

$$(7) \quad E_R = E_{00} - E_{TO}\left(\frac{R_1 + R_2}{R_2}\right)$$

As an example, let the output swing be between -0.5 and 5.5 volts. The output is diode clamped to these levels as shown in Figure 2. Let the threshold be at ±1.5 volts and let $R_1 + R_2$ equal 4.4K.

$$(8) \quad R_1 = \frac{\Delta E_I}{\Delta E_O} (R_1 + R_2) =$$

$$3.0 \times 4.4K = 2.2K$$

Therefore:

$$(9) \quad R_2 = (R_1 + R_2) - R_1 =$$

$$4.4K - 2.2K = 2.2K$$

The output offset is 2.5 volts and the input offset is zero. Therefore, the total offset voltage is 2.5 volts.

$$(10) \quad E_R = E_{OO} - E_{TO}\left(\frac{R_1 + R_2}{R_2}\right) =$$

$$2.5 - 2.5\left(\frac{4.4K}{2.2K}\right) = 2.5 \text{ volts}$$

An HA-2620 is used because is has an extremely high input impedance. An HA-2520 could also be used if faster switching times are desired.

The hysteresis circuit triggers approximately 70 millivolts early because the output voltage begins to drop when the input is within 75 millivolts of the threshold. The maximum current through the diode clamps is only several hundred microamps and remains constant if the differential input voltage is greater than 100 millivolts. Therefore, output voltage remains constant within a few millivolts unless the input is near the threshold. The threshold voltages and the output voltages vary by only a few millivolts from one device to the next. The circuit functions properly with a variation in the threshold voltage of less than ten millivolts when the source resistance is 10 megohms.

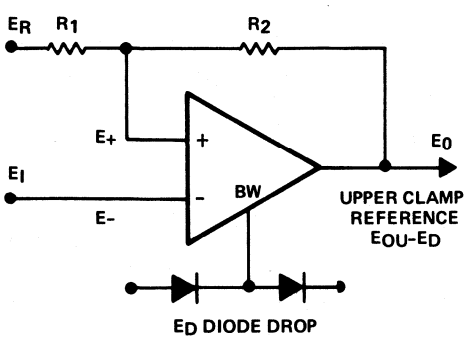

Figure 1

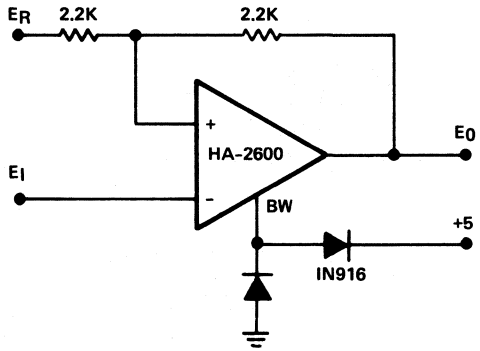

Figure 2

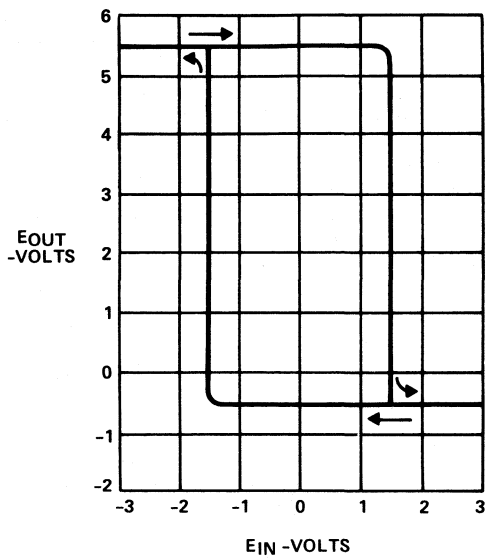

Figure 3. Output Voltage vs. Input Voltage for HA-2620 Hysteresis Amplifier

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APPLICATION NOTE 508

TEST PROCEDURES FOR OPERATIONAL AMPLIFIERS

BY G. G. MILER

The offset voltage of the amplifier under test (A.U.T.) is measured as follows:

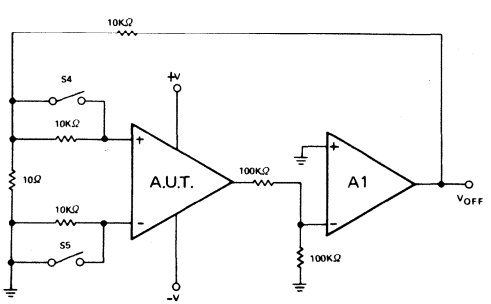
1. Set + and -V to the desired supply voltage and close S4 and S5.
2. Measure the voltage at V_{OFF}.

The offset voltage is equal to (V_{OFF}) (10^{-3}). The feedback amplifier, A1, drives the input of the A.U.T. so that the output is at ground reference, V_{OFF} is driven to 1000 times the voltage necessary to compensate for the offset voltage.

The bias current is measured as follows:

1. Measure the offset voltage, V_{OFF1}, as above.
2. Open S4 and measure V_{OFF2}.
3. The plus input current is equal to ($V_{OFF2} - V_{OFF1}$) x 10^{-7}.
4. Close S4 and open S5 and measure V_{OFF4}.
5. The minus input current is equal to ($V_{OFF4} - V_{OFF1}$) x 10^{-7}.

TEST CIRCUIT FOR MEASUREMENT OF OFFSET VOLTAGE, BIAS CURRENT, AND OFFSET CURRENT 10KΩ

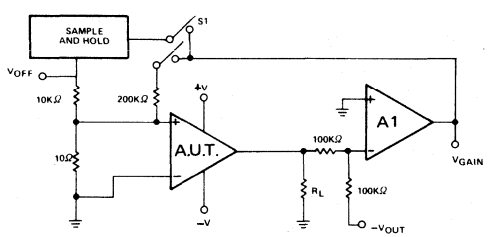


The bias current is equal to the average of the plus and minus input currents.

The input offset current is measured as follows:

1. Measure the offset voltage, V_{OFF1}, as above.
2. Open S4 and S5 and measure V_{OFF2}.
3. The offset current is equal to ($V_{OFF2} - V_{OFF1}$) x 10^{-7}.

TEST CIRCUIT FOR MEASURING OPEN LOOP VOLTAGE GAIN



The open loop voltage gain is measured as follows:

1. Set the +V and -V supply voltages to the desired value and set $-V_{OUT}$ to ground.
2. Close S1 so that the sample and hold will null the offset voltage.
3. S1 can be opened when the circuit stabilizes. The sample and hold will maintain the voltage which nulls the offset voltage.
4. Set $-V_{OUT}$ to the desired output voltage, $-V_4$ and measure V_{GAIN4}.
5. Set $-V_{OUT}$ to another output voltage, $-V5$ and measure V_{GAIN5}.

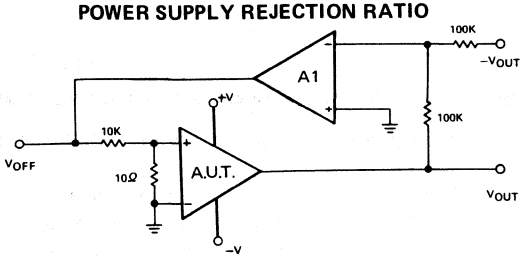
6

6. The gain is equal to

$$\left[\frac{V4 - V5}{V_{GAIN4} - V_{GAIN5}}\right] \times 20{,}000.$$

$-V_{OUT}$ can be first set to zero and then to −10 volts. This gives the gain in the plus direction. The gain in the minus direction can be determined by using zero and +10 volts. The average gain can be determined by using output voltages of −10 and +10 volts.

TEST CIRCUITS FOR MEASUREMENT OF COMMON MODE REJECTION RATIO AND POWER SUPPLY REJECTION RATIO



Common Mode Rejection Ratio:

1. Set +V to +20 VDC, -V to -10 VDC, V_{OUT} +5 VDC by applying -5 VDC to $-V_{OUT}$.
2. Measure V_{OFF2}.
3. Set +V to +10 VDC, -V to -20 VDC, V_{OUT} to -5 VDC by applying +5 VDC to $-V_{OUT}$.
4. Measure $|V_{OFF2} - V_{OFF4}| < 1.0$ VDC.

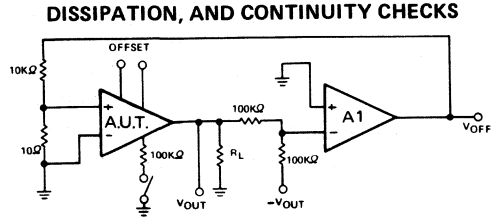
The +1.0 volt limit corresponds to a rejection ratio of 80 dB.

Power Supply Rejection Ratio:

1. Set +V to +20 VDC, -V to 15 VDC, V_{OUT} to ground by grounding $-V_{OUT}$.
2. Measure V_{OFF2}.
3. Set +V to +10 VDC.
4. Measure $|V_{OFF2} - V_{OFF4}| < 1.0$ VDC.
5. Set +V to +15 VDC, -V to -10 VDC.
6. Measure V_{OFF6}.
7. Set -V to -20 VDC.
8. Measure $|V_{OFF6} - V_{OFF8}| < 1.0$ VDC.

The ±1.0 volt limit corresponds to a rejection ratio of 80 dB.

TEST CIRCUITS FOR MEASURING OUTPUT VOLTAGE/CURRENT, POWER DISSIPATION, AND CONTINUITY CHECKS

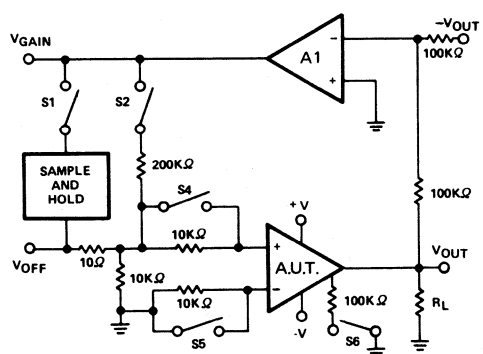


The output voltage/current is measured by connecting a load resistor, R_L, to the output of the A.U.T. The value of R_L is chosen to yield an output current which is the minimum acceptable output current at the desired output voltage. The amplifier under test is programed to a voltage greater than the desired output voltage by applying an equal but opposite polarity voltage to $=V_{OUT}$. The output voltage, V_{OUT}, is measured to see if it reaches the desired output voltage. This test is performed driving the output positive and driving the output negative.

The power dissipation is measured by driving the output voltage to zero by grounding $-V_{OUT}$ and measuring the current in one of the power supply leads.

The continuity of the bandwidth control point is checked by applying −5V to $-V_{OUT}$ and grounding the bandwidth control point through a 100K resistor. V_{OUT} should be less than one volt. There is a known relationship between the voltage at the bandwidth control point and the output voltage, V_{OUT}. This relationship depends on the device type. The continuity of the offset control points is determined by measuring the voltage at these points. These voltages will be slightly less than the positive supply voltage for the HA-2600 and the HA-2500.

SIMPLIFIED SCHEMATIC OF THE COMPLETE D.C. TEST CIRCUIT FOR OPERATIONAL AMPLIFIERS



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APPLICATION NOTE 509

A SIMPLE COMPARATOR USING THE HA-2620

BY G. G. MILER

The input current and impedance of a comparator circuit frequently loads the source and reference signals enough to cause significant errors. This problem is frequently eliminated by using a high impedance operational amplifier between the signal and the comparator. Figure 1 shows a simple circuit in which the operational amplifier is used as a comparator which is capable of driving approximately ten logic gates. The input impedance of the HA-2620 is typically 500 MΩ. The input current is typically 1 nA. The minimum output current of 15 mA is obtainable with an output swing of up to ±10 volts.

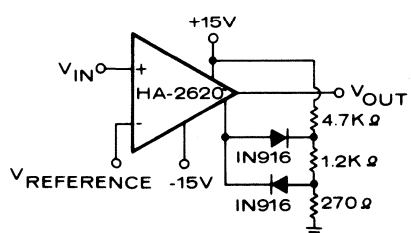

FIGURE 1 - HIGH IMPEDANCE COMPARATOR

The bandwidth control point is a very high impedance point having the same voltage as the amplifier output. The output swing can be conveniently limited by clamping the swing of the bandwidth control point. The maximum current through the clamp diodes is approximately 300 μA. The switching time is dependent on the output voltage swing and the stray capacitance at the bandwidth control point.

Figure 2 shows the waveforms for the comparator. The stray capacitance at the bandwidth control point can be reduced considerably below that of the breadboard circuit; this would improve the switching time. The switching time begins to increase more rapidly as the overdrive is reduced below 10 mV and is approximately 1μs for an overdrive of 5 mV. Dependable switching can be obtained with an overdrive as small as 1 mV. However, the switching time increases to almost 12 μs.

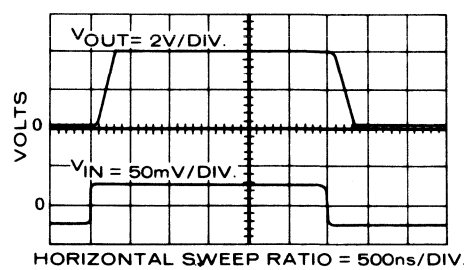

FIGURE 2 - WAVEFORMS FOR HA-2620 COMPARATOR

A common mode range of ±11 volts and a differential input range of ±12 volts makes the HA-2620 a very versatile comparator. The HA-2620 can sink or supply a minimum of 15 mA. The ability to externally clamp the output to any desired range makes the HA-2620 a very flexible comparator which is capable of driving unusual loads.

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APPLICATION NOTE 510

A SIMPLE SQUARE-TRIANGLE WAVEFORM GENERATOR

BY G. G. MILER

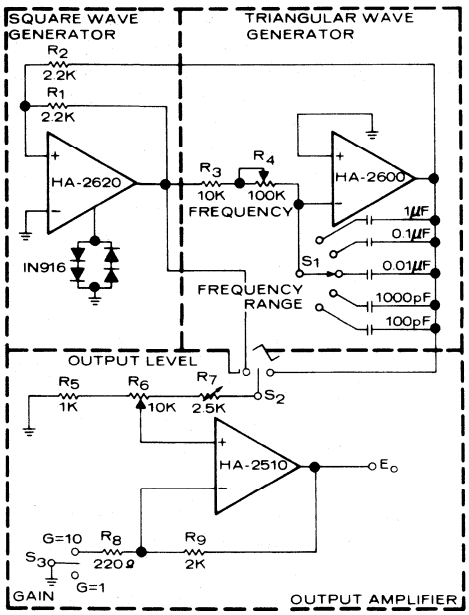

FIGURE 1

Figure 1 shows a very simple function generator which uses only three operational amplifiers. The amplitude of the square and triangular waveforms is variable from 0.2 to 20 volts peak-to-peak. The frequency range is from 2.5Hz to 250kHz. The rise time of the square wave is less than 100 nanoseconds. The slope of the triangular waveform is very linear. Very little change in frequency, amplitude, or waveform is observed with changes in supply voltages between 10 and 20 volts.

The square wave generator consists of a simple hysteresis circuit which is triggered by the triangular wave generator. The output voltage of the square wave generator is clamped to the desired level by diodes connected to the bandwidth control point. The circuit shown gives an output of two volts peak-to-peak. The ratio of the amplitude of the square wave to the triangular wave is equal to the ratio of R_1 to R_2. An HA-2620 is chosen for the comparator because it has very low input currents, high slew rate and wide bandwidth.

The triangular wave generator consists of an integrator which integrates the output of the square wave generator. The frequency of the function generator is controlled by the ramp rate of the triangular wave and the threshold levels of the hysteresis circuit. S_1 selects the integrating capacitor which changes the frequency range in decade steps. R_4 is the variable frequency control. The frequency of the function generator, f, is given by:

$$f = \frac{1}{4(R_3 + R_4)\,C}\left(\frac{R_1}{R_2}\right)$$

Better high frequency operation can be obtained by reducing the value of R_3 and R_4. Very long periods can be obtained by increasing the value of R_3, R_4 and the integrating capacitor. The HA-2600 is chosen because it produces the most accurate integration, having a typical input bias current of 1nA. The HA-2620 can be used for the integrator. It may be necessary to add some external compensation to prevent ringing if an HA-2620 is used.

The output amplifier consists of a simple non-inverting amplifier using a HA-2510. The HA-2510 is chosen for its high slew rate of 50 volts per microsecond. S_3 selects a gain of one or ten. The variable output attenuator, R_6, sets the input level to the amplifier. R_7 serves as an output level calibration control. The maximum output current should be limited to 20mA. The load impedance should not be less than 600 Ω for a gain of ten and 50Ω for unity gain.

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APPLICATION NOTE 511

HI-1080 DIGITAL TO ANALOG CONVERTER APPLICATIONS

BY DON JONES

GENERAL USES

D to A converters are useful in any system where both digital and analog signals are present. Some of the more common applications include:

1. Data processing output interface; driver for displays, plotters, etc.
2. Programmable power supply or function generator in automatic test equipment.
3. Tool interface in numerical controlled machining.
4. Interface for automatic process control to control temperature, flow rates, etc.
5. Digital communications: digital to audio interface.
6. Feedback network in A to D converters.

TERMINOLOGY

A definition of some of the terms and parameters encountered in D to A conversion will be helpful to those being introduced to the field.

Resolution: An indication of the number of possible analog output levels, usually expressed as the number of input bits that the converter will handle. For example, an eight (8) bit binary weighted converter will have $2^8 = 256$ possible output levels (including zero). This should not be confused with accuracy, which is sometimes also expressed as a number of bits.

Accuracy: A measure of the deviation of the analog output level from its predicted value under any input combination. This can be expressed as a percentage of full scale, a number of bits (N bits accuracy = $\frac{1}{2}^N$ possible error,) or a fraction of the least significant bit (if a converter with M bits resolution has 1/2 L.S.B. accuracy the possible error is $\frac{1}{2} \times \frac{1}{2^M}$). Accuracy may be of the same, higher, or lower order of magnitude as the resolution. The importance of accuracy vs. resolution depends on the application. Possible errors in individual bit weights which may be cumulative with combinations of bits; errors in the summation of individual bit weights and changes in these due to temperature variations.

Least Significant Bit (L.S.B.): The digital input bit carrying the lowest numerical weight; or the analog level shift associated with this bit, which is the smallest possible analog step.

Most Significant Bit (M.S.B.): The digital input bit carrying the highest numerical weight; or the analog level shift associated with this bit. In a binary weighted converter the M.S.B. creates a half of full scale level shift.

Settling Time: The total time measured from a digital input change to the time the analog output reaches its new value within a specified error band. It should be noted that the transition from one level to another is not always smooth; spikes and ringing may occur.

THE HI-1080 MONOLITHIC D TO A CONVERTER

The Harris Semiconductor HI-1080 is the first monolithic integrated circuit D to A converter complete with the thin film resistor ladder network on the same chip as the switching devices. Along with the advantages of small size and monolithic reliability, this allows higher speed and faster settling. Also it has the advantage over separate switches and ladder networks in that overall performance is guaranteed and there is no need to add the possible errors of separate components.

The functional diagram of the HI-1080 is shown in Figure 1. An external reference supply, usually 5 volts, is connected between the +REF and the -REF pins. The output levels will be directly proportional to the differential reference voltage. Variations of the other +5 volt and the -15 volt power supplies have negligible effect on the analog output. Either the +REF or the -REF pin may be grounded, so reference supplies of either polarity may be accomodated. The smaller value resistors between +REF and T_1 or between T_2 and T_3 may be externally shorted out, or an external trimmer substituted, for fine adjustment of the full scale output level. The positive side of the reference supply may be connected to T_2 or T_3 for a 10 volt nominal output swing, which is useful in bipolar operation.

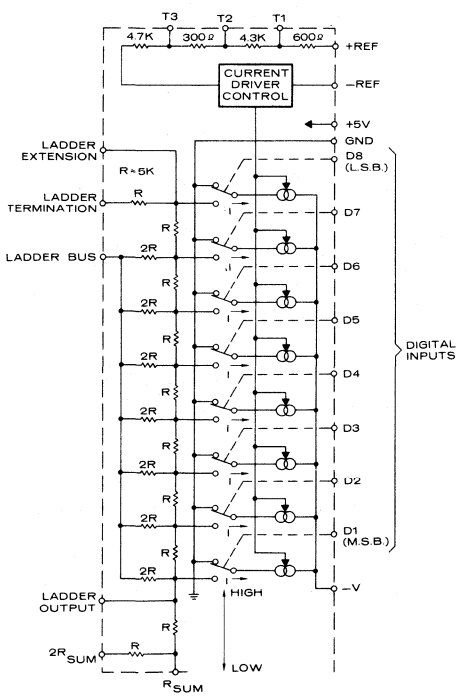


Figure 1. Functional Diagram HI-1080

The reference level is conditioned through the current driver control where the output current of each of the eight current drivers is determined.

The use of current sources to drive the ladder network has several advantages over voltage sources. Within the constant current range of the sources, the current, and hence the differential ladder output voltage, will remain constant regardless of variations in the negative supply voltage and the voltage of the ladder return bus. The ladder bus may be returned to a voltage other than ground if desired for offset or bipolar outputs without affecting its output. The digital and analog grounds can be effectively separated for noise free operation. Also switching of a current source rather than a voltage source generally is faster, creates less ringing at the output, and produces smaller power supply transients.

The digital inputs effectively switch the current source outputs either to the ladder network or to ground. The inputs are fully compatible with any standard 5 volt DTL or TTL logic circuits. A "high" input (> +2 volts) switches the current source to ground; a "low" input (<+0.8 volts) switches the current source to the ladder, creating a more negative output voltage. This polarity convention should be kept in mind when designing with the HI-1080.

The ladder network is constructed from high stability metal film resistors deposited on the same silicon chip. Identical material is used for the resistors in the reference supply network and in the current source circuitry to achieve good temperature stability. The "R – 2R" ladder network is used rather than a weighted resistor network because identical resistors will match better in value and temperature coefficient. Extra resistors are provided at the R Sum and 2R Sum terminals which are very useful for feedback or summing with external amplifiers or comparators, since these resistors will track almost perfectly with the ladder source resistance. Provision is made at the other end of the ladder for cascading converters for higher resolution.

A block diagram is shown in Figure 2 and schematics of the block in Figures 3 – 5.

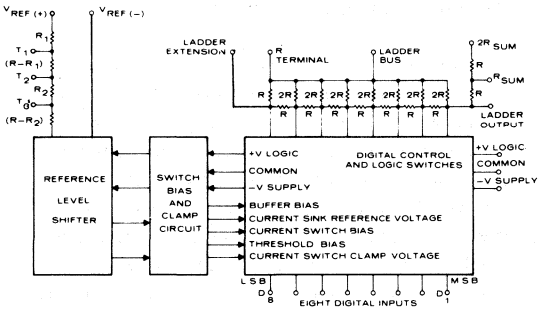


Figure 2. 8 Bit D/A Converter Block Diagram

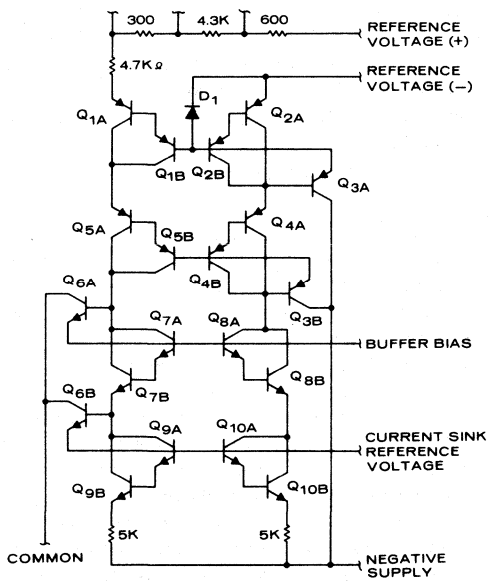


Figure 3. D/A Converter Reference Level Shifter

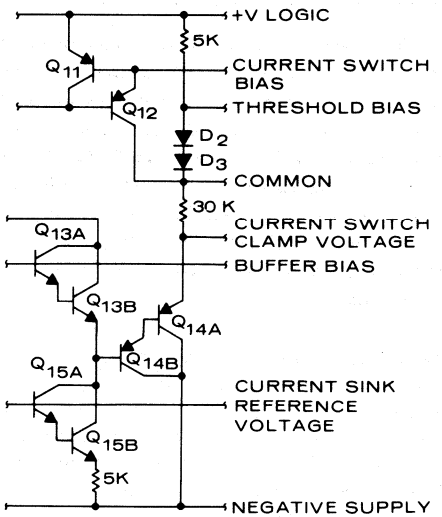


Figure 4. D/A Converter Current Switch Bias & Clamp Circuit

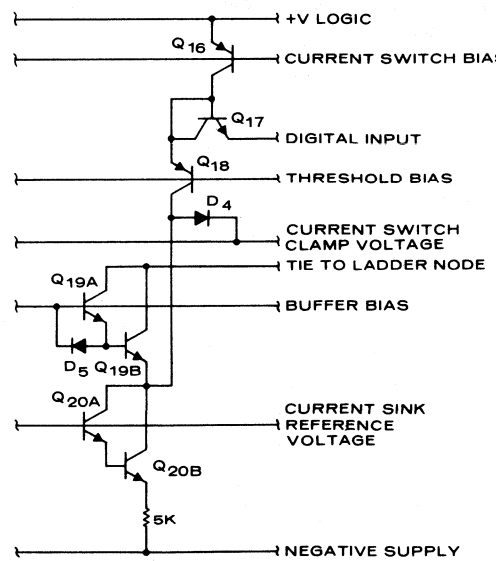
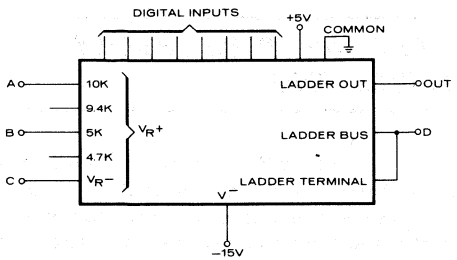


Figure 5. D/A Converter Ladder Current Switch

OPERATING MODES

Some of the possible operating modes of the HI-1080 are illustrated in Figure 6. Since both the reference supply terminals and the ladder bus terminal can be connected to any voltage within ±5 volts with respect to power supply ground, a number of output polarity modes can be achieved. In all cases the ladder output will become more negative with respect to the ladder bus as a digital input is changed from the high to the low state.



MODE	OUTPUT RANGE INPUTS: ALL HIGH TO ALL LOW	CONNECTIONS			
		A	B	C	D
UNIPOLAR ZERO REFERENCE	0 TO − [V_R+ − 1 L.S.B.]	V_R+	N.C.	GND	GND
UNIPOLAR ZERO F.S.	+ / V_R+/ TO [0 + 1 L.S.B.]	V_R+	N.C.	GND	V_R+
BIPOLAR	/V_R+/ TO [−V_R+ 1 L.S.B.]	N.C.	V_R+	GND	V_R+

Figure 6. D/A Converter Operation Modes

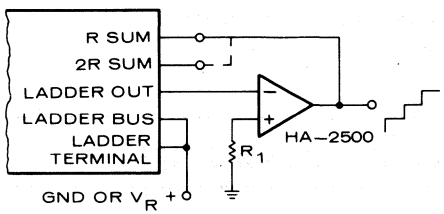
In the unipolar – zero reference mode, the ladder bus is grounded. Using negative logic convention (high = 0, low = 1), the output will increase in the negative direction with increasing input binary number. Either side of the reference supply may be grounded.

In the unipolar – zero full scale mode, the ladder bus is connected to the positive reference voltage, so the output will be always positive with respect to the reference ground. Now, using positive logic convention (low = 0, high = 1), the output will increase in the positive direction with increasing binary number. It may be necessary to connect V_R+ to a lower tap in series with a potentiometer to adjust the zero level.

The bipolar mode connection is similar to the previous mode except the V_R+ is connected to T_2 (or T_3 through a pot), so that the full scale excursion is now 10 volts. With all inputs low, the output will be most negative (about -4.96V). With only the M.S.B. high, the output will be zero volts. With all inputs high, the output will be at V_R+.

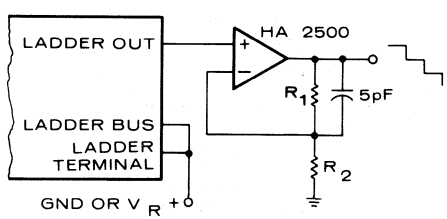
AMPLIFIER CONNECTIONS

Figure 7 illustrates connections from the converter to an operational amplifier. The inverting connection uses the summing registers provided on the chip for amplifier feedback. Since the ladder impedance is nominally 5K ohms, connection of the output to R Sum will result in a gain of -1. Connection to 2_R Sum will result in a gain of -2. Any of the operating modes discussed previously may be used.



FULL SCALE OUTPUT	OUTPUT FEEDBACK CONNECTED TO :	R_1
+4.98V	R_{SUM}	2.5K
+9.96V	$2R_{SUM}$	3.3K

INVERTING OUTPUT
(MORE POSITIVE WITH INCREASING
COMPLEMENT OF INPUT NUMBER)



OUTPUT RANGE: SAME AS SHOWN
ON 'OPERATING MODE' CHART

MULTIPLIED BY $\frac{R2}{R1 + R2}$

NON-INVERTING OUTPUT
(MORE NEGATIVE WITH INCREASING
COMPLEMENT OF INPUT NUMBER)

Figure 7. Buffer Amplifier Connection

6

For a noninverting output the operational amplifier is wired in the conventional manner. The R Sum or 2R Sum resistor could be used to sum an external analog signal of opposite polarity at the amplifier input.

The Harris Semiconductor HA-2500 operational amplifier is recommended for high speed applications since its slew rate of 25 volts per microsecond is sufficient to follow the converter output steps very closely. For more moderate speed applications, the Harris Semiconductor HA-2600 operational amplifier is recommended for better offset drift while retaining a minimum slew rate of 4 volts per microsecond. Booster stages may be added to the amplifier outputs to drive any required load.

CASCADED D TO A CONVERTERS

Two HI-1080 units may be cascaded to achieve resolutions from 9 to 15 bits, using the ladder extension terminals, as illustrated in Figure 8. Note that input D8 of the higher significant bit unit is not used. This is necessary in order to join the two ladders correctly.

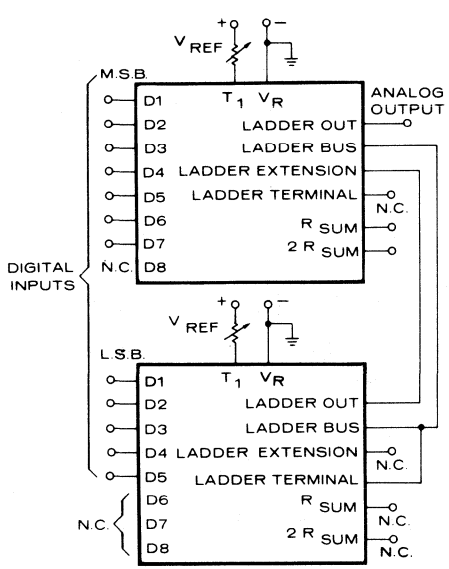


Figure 8. Cascaded Units for 12 Bit Resolution

A person might ask, "Why would anyone want a 12 bit converter with only 8-1/2 bit accuracy?" The answer is that most applications require accuracy expressed as a percentage of actual output rather than as a percentage of full scale output. One feature of the R – 2R ladder network is that errors in terms of millivolt deviation from the predicted output tend to become smaller as the lesser significant bits only are exercised. So for the 12 bit converter shown, with outputs between 1.25 and 5 volts the errors may be on the order of ±10 millivolts; but for outputs between 0 and 20 millivolts the errors will tend to be less than 0.7 millivolts.

A TO D CONVERTER; UP-DOWN COUNTER TYPE

A high speed D to A converter can be used as the heart of several very useful types of A to D converters. The up-down counter, or servo type converter is most efficient in monitoring one analog signal continuously, rather than monitoring multiplexed analog signals.

The converter works basically by balancing the input analog signal with the D to A output, adjusting the D to A by running a digital counter up or down as required to balance the signal. When the two analog signals balance, the counter state represents the digital equivalent of the input signal.

In the example shown in Figure 9, the two analog signals are fed differentially into an op-amp. For a positive input signal, the D to A could be run in the positive output mode, or in the negative output mode by summing the two signals at the inverting amplifier input. The amplifier gain should be set at 2 or greater to allow less critical thresholds for the comparators.

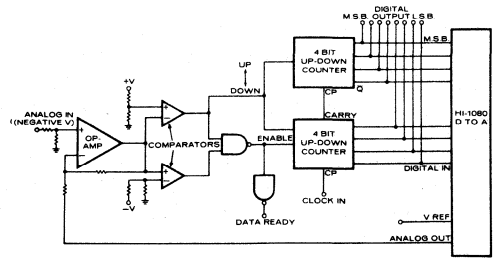


Figure 9. "Up-Down Counter" Type A to D Converter

The two comparator thresholds are set up by voltage dividers to correspond to unbalances of approximately ±1/2 L.S.B. When the analog signals are balanced within this range, the comparator outputs are both high, which stops the counters and gives a Data Ready signal to indicate that the digital outputs are correct.

If the analog signals are unbalanced by more than ±1/2 L.S.B., the counter is enabled and driven in the up or down direction depending on the polarity of the unbalance.

If the D to A converter is operated in the negative output mode, the digital outputs will follow negative logic convention.

If the analog input signal varies by less than 1 L.S.B. per clock period, the converter will continuously track the signal.

The Data Ready signal could be useful in adaptive systems for most efficient data transfer, since that signal changes state only when there is a significant change in the analog input. When monitoring a slowly varying input, it would be necessary to read-out the digital output only after a change has taken place. The Data Ready signal could trigger a flip-flop to flag this condition and the flip-flop would be reset after read-out.

The main disadvantage of the up-down counter converter is the time required to initially acquire a signal, which in an 8 bit system, could be up to 256 clock periods. The input signal usually must be filtered so that its rate of change does not exceed the tracking rate of the converter.

A TO D CONVERTER, SUCCESSIVE APPROXIMATION TYPE

Suppose you were asked to guess a secret number between 0 and 15 by asking the least number of questions answerable by yes or no. One of the most efficient ways might work as follows:

"Is it 8 or greater?"

"Yes"

"Is it 12 or greater?"

"No"

"Is it 10 or greater?"

"Yes"

"Is it 11?"

"No"

If you had jotted down a "1" for each "yes" and a "0" for each "no", you would have 1010, which of course is the binary notation for ten. So it is possible to find one number out of 16 with 4 questions. Likewise 8 questions would be required to find a number between 0 and 255. Obviously this technique is usually much quicker than saying, "Is it zero?", "Is it one?", etc., or guessing numbers at random.

The successive approximation converter shown in Figure 10 uses the same technique to find which proportional number between 0 and 255 best approximates the input analog voltage.

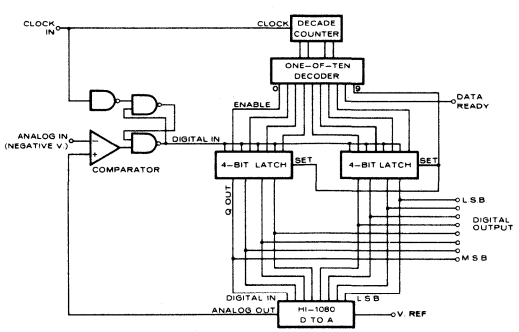


Figure 10. Successive Approximation Type A to D Converter

This is accomplished in 8 clock cycles – two additional cycles are used in this design to hold the data and to clear the registers, but this could be done during the eighth cycle, if necessary. The measurement starts with all zeros programmed into the D to A and the decade counter set to zero. The decoder enables the first of eight latches and the clock pulse sets a flip-flop composed of two cross-coupled gates setting a "1" in the first latch, so the D to A has a 10,000,000 input. The D to A consequently produces a half-scale output which goes to one side of the comparator. The comparator now effectly asks the question "Is the input greater than half-scale?". If the answer is "yes", the comparator output is high and the flip-flop remains set. If the answer is "no" the comparator resets the flip-flop during the second half cycle of the clock, resetting the first latch to zero.

On the second clock cycle the decoder enables the second latch while the last state of the first latch remains stored in it and remains as the D to A, M.S.B. input. In a similar manner, the state of the second M.S.B. is decided and the decoder moves on to the third. After the eighth clock cycle the conversion is complete, which is signaled by the Data Ready line on the ninth cycle. At the tenth cycle all latches are reset to be ready for the next conversion.

In practice, the delay of the clock pulse through the counter and decoder should be less than the delay through the three gates for proper timing.

Polarities shown are correct for the D to A connected in the negative output mode, and the digital output will be correct in negative logic. A positive analog input can be handled by summing with the D to A output at one comparator input, or by operating the D to A in the positive output mode and shifting the digital polarities as necessary.

It is necessary in any successive approximation converter for the analog input to remain constant during the conversion.

In multiplexed systems this is usually accomplished with a sample-and-hold circuit in the analog line.

It can be seen that the successive approximation type will give the correct output in eight clock cycles while the up-down counter type could take up to 255 cycles to acquire a signal. Once acquired, the up-down counter can indicate a change in a slowly varying signal within one clock cycle, while the successive approximation type must step through another eight cycles. The choice really depends on the type of signals to be monitored.

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APPLICATION NOTE 512

COUNTER TYPE A TO D CONVERTER

BY DON JONES

INTRODUCTION

This paper describes circuit details for a full temperature range eight-bit A to D converter employing a unidirectional digital counter and a D to A converter. As shown in the simplified diagram in Figure 1, circuit operation is quite simple. A multiple stage counter circuit is driven from a clock and the counter output drives a D to A converter producing a staircase voltage ramp. When the D to A output voltage equals the analog input voltage, the comparator changes state, and at that instant, the counter state represents the digital equivalent of the analog input.

The heart of this circuit is the HI-1080 Eight-Bit D to A Converter, which is a monolithic integrated circuit containing both the current switches and the R-2R ladder network. This features good speed and accuracy over $-55^{o}C$ to $+125^{o}C$ temperature range. The HI-1080 D to A converter is also very effective in up-down counter and successive approximation type A to D converters, which are described in other application notes.

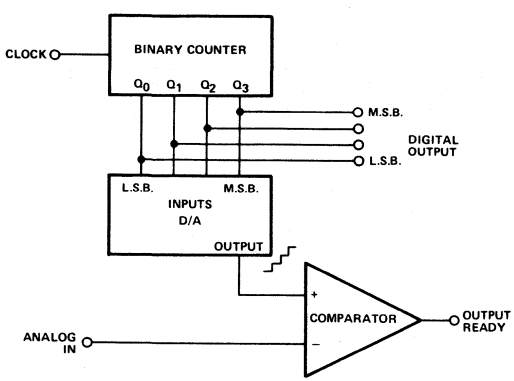

Figure 1. Simplified Diagram, Counter Type A/D

COUNTER vs. SUCCESSIVE APPROXIMATION TYPE CONVERTERS

The most popular A to D converter employing a D to A circuit is the successive approximation type. This type is useful for high speed conversion, since it requires only N clock cycles for an N-bit conversion, while the counter type requires up to 2^N cycles. One disadvantage, where many conversions per second are not needed, is that a sample-and-hold circuit is nearly always required in the analog signal path. The sample-and-hold circuit is an additional error source which is difficult to control over a wide temperature range. The counter type converter does not require a sample-and-hold circuit, since its output is a parallel digital number taken at the instant that the D to A and input signals are equal, although filtering of the input signal may be desirable in some applications. The counter type converter illustrated here can perform 1,000 conversions per second, which is adequate for many applications.

CIRCUIT DETAILS

The complete circuit schematic is shown in Figure 2 and typical waveforms are illustrated in Figure 3. The digital circuits shown are 9300 types, but comparable circuits from other TTL families will work equally well if any functional differences are taken into account.

Since the D to A converter normally has a negative output level, a positive input signal is compared by resistive summation at one comparator input, using the summing resistor internal to the D to A which closely matches the D to A equivalent output resistance.

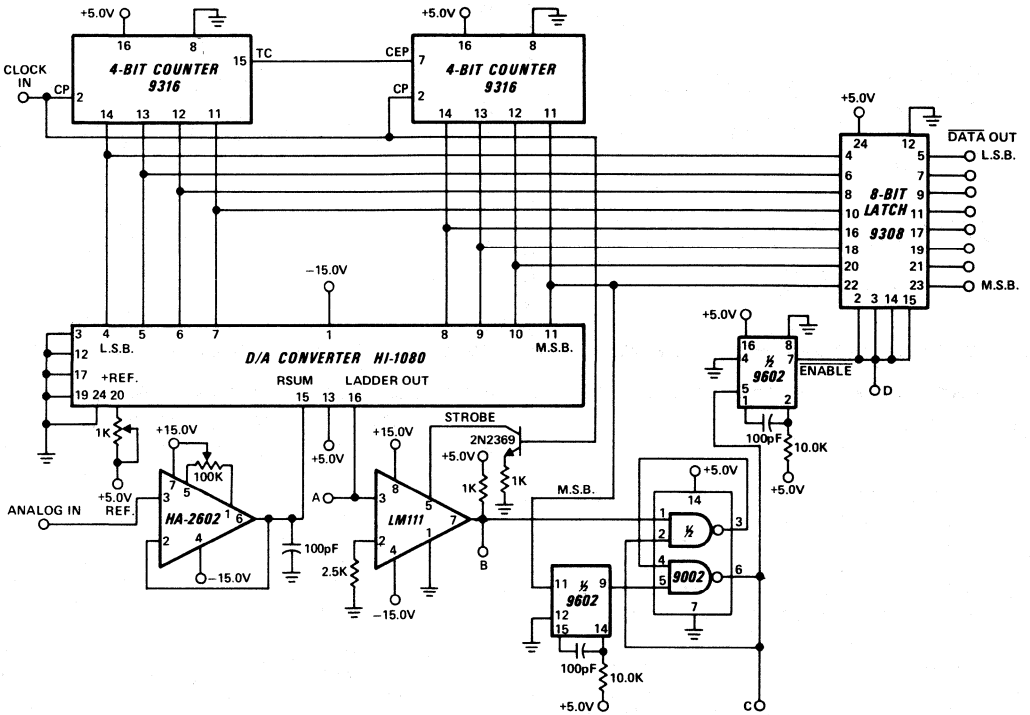

Figure 2. Complete A/D Schematic

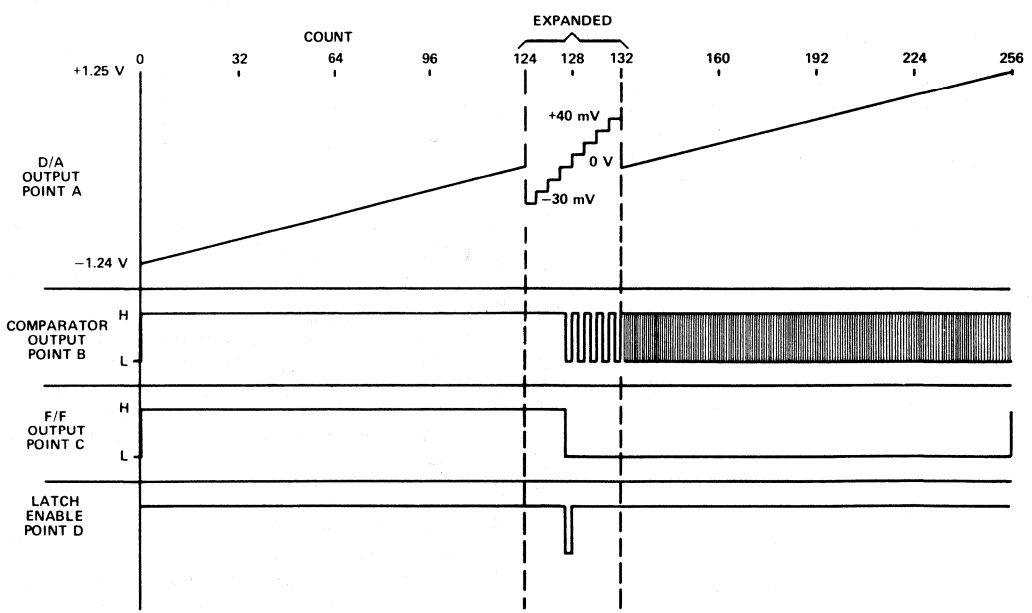

Figure 3. Waveforms with +2.50 Volts Analog Input

The comparator is strobed with the clock to prevent any D to A switching spikes from prematurely triggering the comparator. The strobing necessitates the use of the set-reset flip-flop formed by the cross-coupled gates so that the latch receives only one enable pulse per conversion cycle.

Note that the data output from the latch is the complement of the digital value, due to the polarity conventions of the D to A.

CIRCUIT ADJUSTMENT

For 0 to +5 volt input range the input op-amp is first zeroed in the conventional manner. Then +2.500 volts is applied to the input, and the pot between the reference supply and the D to A is adjusted so that the M.S.B. just trips in at this level. The full scale input will then be 1 L.S.B. below +5.000 volts which is +4.980 volts.

For 0 to +10 volts input range, connect the op-amp output to the 2R sum terminal on the D to A.

For 0 to −5 volt range, connect the op-amp output to the negative input of the comparator through a 5K ohm resistor.

For −5 volt to +5 volt bipolar operation, connect the ladder bus terminal on the D to A to the +5 volt reference, and connect the reference through the potentiometer to the T3 terminal of the D to A.

Virtually any other input range is possible by changing the op-amp gain or polarity, or adjusting the reference potentiometer. Zero shift may be accomplished by offsetting the ladder bus, or summing voltages at the op-amp or comparator inputs.

CIRCUIT PERFORMANCE

Accuracy is affected primarily by the D to A accuracy, and to a lesser degree by offsets in the input op-amp and the comparator. This circuit proved to be accurate within +½ L.S.B. at room temperature, and ±1 L.S.B. from −55°C to +125°C. This accuracy was maintained at clock rates up to 330 KHz. Clock rates up to 1 MHz could be used with about 1 additional L.S.B. of inaccuracy.

CIRCUIT VARIATIONS

Using the illustrated circuit as a starting point, many modifications to the digital circuitry are possible to suit the application.

For convert-on-command operation, the circuitry beyond the comparator, including the latch could be eliminated and the comparator output used to gate off the clock signal. The counters will hold their value until a command to convert again is issued by resetting the counters to zero.

For continuous conversion, a reduction in average (but not maximum) conversion time can be made by resetting the counters immediately after data is entered in the latches.

Another possible improvement in conversion time can be acheived by running the clock at a variable rate - fast while the D to A output is far from the input level and slower when the comparator is about ready to trip. One possibility is to use a VCO as the clock, controlled in frequency by an op-amp with inputs wired across the comparator inputs. Another possibility would be to use a fixed 5 MHz clock and insert a ÷16 counter in series with the clock line when the D to A and input voltages are nearly equal. This could be controlled by a second comparator with the trip point offset from that of the main comparator.

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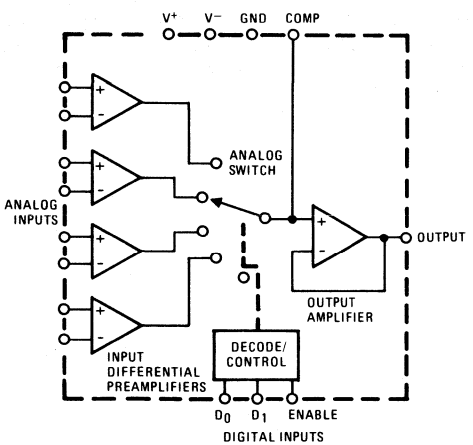
APPLICATION NOTE 514

THE HA-2400 PRAM FOUR CHANNEL OPERATIONAL AMPLIFIER

BY DON JONES

INTRODUCTION

Harris Semiconductor has announced a new linear device, the HA-2400/HA-2405 Four Channel Operational Amplifier. This combines the functions of an analog switch and a high performance operational amplifier, and makes practical a large number of new linear circuit applications.



A functional diagram of the HA-2400 is shown above. There are four preamplifier sections, one of which is selected through the DTL/TTL compatible inputs and connected to the output amplifier. The selected analog input terminals and the output terminal form a high performance operational amplifier.

In actuality, the circuit consists of four conventional op-amp input circuits connected in parallel to a conventional op-amp output circuit. The decode/control circuitry furnishes operating current only to the selected input section.

CIRCUIT CONNECTIONS

These inputs control the selection of the amplifier input channels in accordance with the truth table below:

D_0	D_1	ENABLE	CHANNEL 1	CHANNEL 2	CHANNEL 3	CHANNEL 4
L	L	H	ON	OFF	OFF	OFF
H	L	H	OFF	ON	OFF	OFF
L	H	H	OFF	OFF	ON	OFF
H	H	H	OFF	OFF	OFF	ON
L or H	L or H	L	OFF	OFF	OFF	OFF

0V ≤ L ≤ +0.8V +2.0V ≥ H ≥ +5.0V

The digital inputs can be driven with any DTL or TTL circuit which uses a standard +5.0V supply.

COMPENSATION

Frequency compensation for closed loop stability is recommended for closed loop gains less than 10. This is accomplished by connection of a single external capacitor from Pin 12 to A.C. ground (the V+ supply is recommended). The following table shows the minimum suggested compensation for various closed loop gains, with the resultant bandwidth and slew rate. Obviously, when the four channels are connected with different feedback networks, the channel with the lowest closed loop gain will govern the required compensation.

GAIN, VOLTS/VOLT		C_{COMP}	BANDWIDTH (TYPICAL)	SLEW RATE (TYPICAL)
NON-INVERTING	INVERTING	pF	(-3dB), MHz	VOLTS/μs
1	-	15	8.0	15
2	1	7	8.0	20
3	2	4	8.0	22
5	4	3	6.0	25
8	7	2	5.0	30
>10	>9	0	40÷GAIN	50

Compensation capacitors of greater value can be used to obtain lower bandwidth, greater

phase margin, and reduced overshoot, at the expense of proportionately reduced slew rate.

External lead-lag networks could also be used to optimize bandwidth and/or slew rate at a particular gain.

APPLICATIONS

Any circuit function which can be constructed using a conventional operational amplifier can also be constructed using any channel of the HA-2400. Similar or different networks can be wired from the output to each channel input pair. The device can therefore be used to select and condition different input signals, or to select between different op-amp functions to be performed on a single input signal.

To wire a particular op-amp function to a channel, simply connect the appropriate network between the two inputs for that channel and the common output in the same manner as in wiring a conventional op-amp. It is often possible to design with fewer external components than would be required in wiring four separate op-amps (see Application Numbers 2 and 3 on the following pages). It should be remembered that the networks for unselected channels may still constitute a load at the amplifier output and the signal input, as if the unselected input terminals were disconnected from the network.

If offset adjustment is required, it can generally be accomplished by resistive summation at either of the inputs for each channel (see Application Number 8).

The analog input terminals of the OFF channels draw the same bias current as the ON inputs. The maximum differential input voltage of these terminals must be observed and their voltage levels must never exceed the supply voltages.

When the Enable input is held low, all four input channels are disconnected from the output. When this occurs, the output voltage will generally slowly drift towards the negative supply. If a zero volt output condition is required, one channel should be wired as a voltage follower with its positive input grounded.

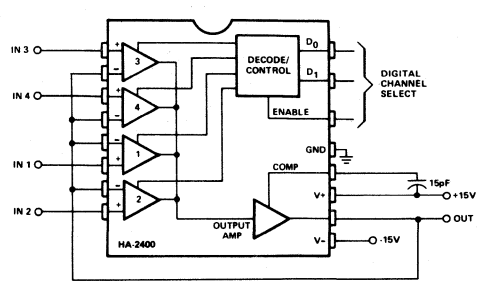
The amplifier output impedance remains low, even when the inputs are disabled; so it is not generally practical to wire the outputs of two or more devices directly together. The compensation pins of two devices, however, could be wired together to produce a switch with one output and more than four input channels.

The voltage at the compensation pin is about 0.7V more positive than the output signal, but has a very high source impedance. Maximum current from this pin is about 300μA, which makes it a convenient point for limiting the output swing through clamping diodes and divider networks (see Application Number 13).

Even if the application only requires a single channel to be switched on and off, it is often more economical to use the HA-2400, rather than a separate analog switch and high performance op-amp. Unused analog channel inputs should be grounded. Unused digital inputs may be wired to ground for a permanent "low" input, or either left open or wired to +5.0V for a permanent "high" input.

Illustrated on the following pages are a few of the thousands of possible applications for the Four Channel Operational Amplifier. These will give the reader a general impression of how the units can be connected; and probably will help generate many other ideas for applications. Also included are some "challenges" for the reader to modify the illustrated designs to perform different functions.

APPLICATION NO. 1



ANALOG MULTIPLEXER WITH BUFFERED INPUT AND OUTPUT

This circuit is used for analog signal selection or time division multiplexing. As shown, the feedback signal places the selected amplifier channel in a voltage follower (non-inverting unity gain) configuration, and provides very high input impedance and low output impedance. The single package replaces four input buffer amplifiers, four analog switches with decoding, and one output buffer amplifier.

For low level input signals, gain can be added to one or more channels by connecting the (—) inputs to a voltage divider between output and ground. Bandwidth is approximately 8 MHz, and the output will slew from one level to another at about 15.0V per microsecond.

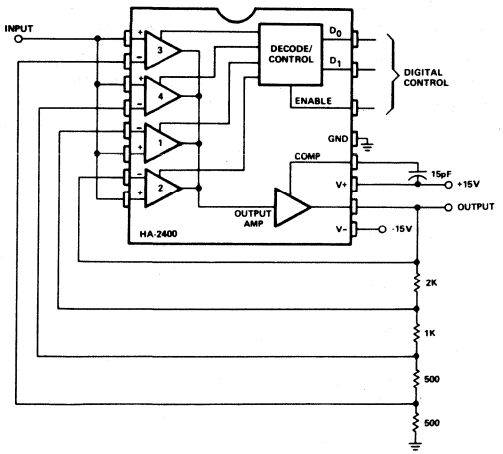
Expansion to multiplex 5 to 12 channels can be accomplished by connecting the compensation pins of two or three devices together, and using the output of only one of the devices. The Enable input on the unselected devices must be low.

Expansion to 16 or more channels is accomplished in a straightforward manner by connecting outputs of 4 four-channel multiplexers to the inputs of another four-channel multiplexer.

Differential signals can be handled by two identical multiplexers addressed in parallel.

Inverting amplifier configurations can also be used, but the feedback resistors may cause crosstalk from the output to unselected inputs.

APPLICATION NO. 2



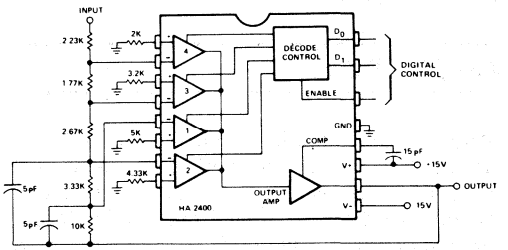
AMPLIFIER, NON-INVERTING PROGRAMMABLE GAIN

This is a non-inverting amplifier configuration with feedback resistors chosen to produce a gain of 0, 1, 2, 4, or 8 depending on the Digital Control inputs.

Comparators at the output could be used for automatic gain selection for auto-ranging meters, etc.

CHALLENGE: Design a circuit using only two HA-2400's which can be programmed to any of 16 different gains.

APPLICATION NO. 3

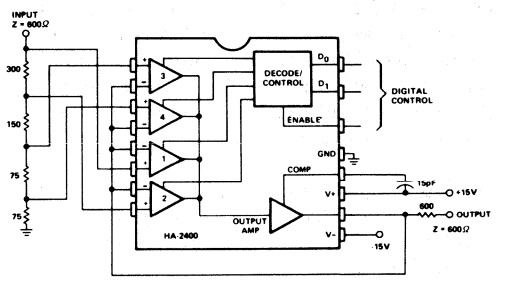


AMPLIFIER, INVERTING PROGRAMMABLE GAIN

The circuit above can be programmed for a gain of 0, —1, —2, —4 or —8.

This could also have been accomplished with one input resistor and one feedback resistor per channel in the conventional manner, but this would require eight resistors rather than five.

APPLICATION NO. 4

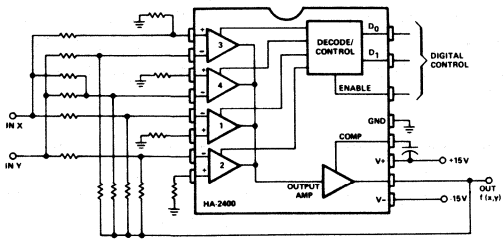


ATTENUATOR PROGRAMMABLE

This circuit performs the function of dividing the input signal by a selected constant (1, 2, 4, 8, or ∞ as illustrated). To multiply by a selected constant, see circuit No. 2. While T, π, or L sections could be used in the input attenuator, this is not necessary since the amplifier loading is negligible and a constant input impedance is maintained. The circuit is thus much simpler and more accurate than the usual method of constructing a constant impedance ladder and switching sections in and out with analog switches.

Two identical circuits may be used to attenuate a balanced line.

APPLICATION NO. 5

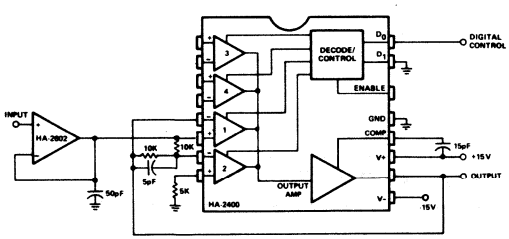


ADDER/SUBTRACTOR PROGRAMMABLE FUNCTION

The circuit shown above can be programmed to give the output functions $-K_1X$, $-K_2Y$, $-(K_3X + K_4Y)$, or $K_5X - K_6Y$. Obviously, many other functions of one or more variables can be constructed, including combinations with analog multiplier or logarithmic modules.

This device opens up many new design approaches in digitally controlled analog computation or signal manipulation.

APPLICATION NO. 6

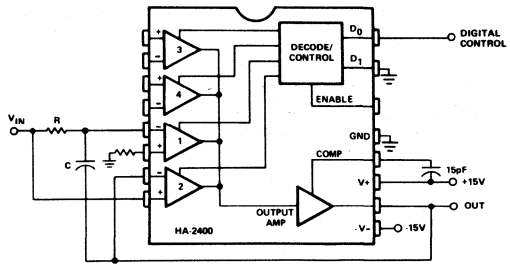


PHASE SELECTOR/PHASE DETECTOR/ SYNCHRONOUS RECTIFIER/BALANCED MODULATOR

This circuit passes the input signal at unity gain, either unchanged, or inverted depending on the Digital Control input. A buffered input is shown, since low source impedance is essential. Gain can be added by modifications to the feedback networks. Signals up to 100 kHz can be handled with 20.0V peak-to-peak output. The circuit becomes a phase detector by driving the Digital Control input with a reference phase at the same frequency as the input signal, the average D.C. output being proportional to the phase difference, with zero volts at $\pm 90^{o}$. By connecting the output to a comparator, which in turn drives the Digital Control, a synchronous full-wave rectifier is formed.

With a low frequency input signal and a high frequency digital control signal, a balanced (surpressed carrier) modulator is formed.

APPLICATION NO. 7

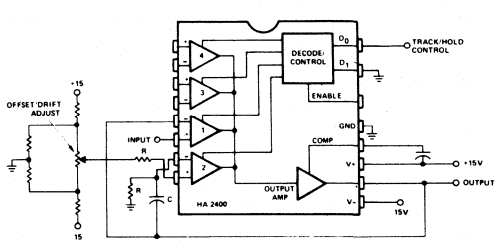


INTEGRATOR/RAMP GENERATOR WITH INITIAL CONDITION RESET

It is difficult in practice to set the initial conditions accurately in an integrator. This usually requires wiring contacts of a mechanical relay across the capacitor - - leakage currents of solid state switches produce integration inaccuracy. The scheme shown above eliminates these reliability and accuracy problems.

Channel 1 is wired as a conventional integrator, Channel 2 as a voltage follower. When Channel 2 is switched on, the output will follow V_{IN}, and C will discharge to maintain zero volts across it. When Channel 1 is then switched on the output will initially be at the instantaneous value of V_{IN}, and then will commence integrating towards the opposite polarity. This circuit is particularly suitable for timing ramp generation using a fixed D.C. input. Many variations are possible, such as programmable time constant integrators.

APPLICATION NO. 8



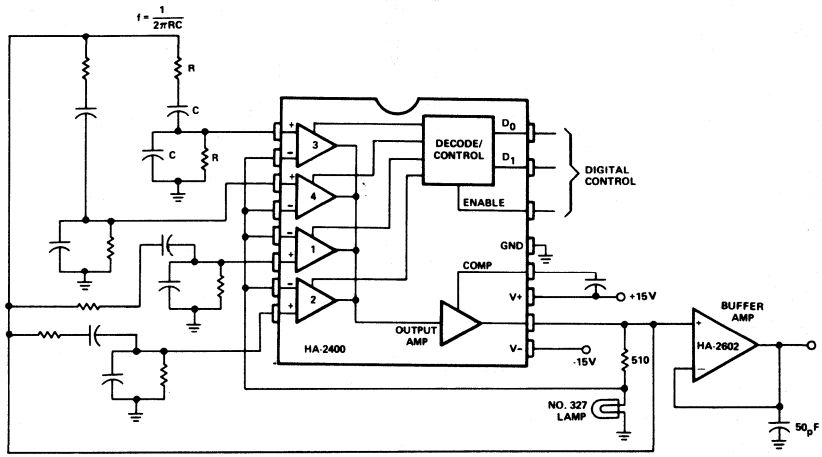
TRACK AND HOLD/SAMPLE AND HOLD

Channel 1 is wired as a voltage follower and

is turned on during the track/sample time. If the product of R x C is sufficiently short compared to the period of maximum output frequency, or sample time, C will charge to the output level. Channel 2 is an integrator with zero input signal. When Channel 2 is then turned on, the output will remain at the voltage across C.

An even simpler circuit can be made by wiring one channel as an amplifier, choosing the compensation capacitor to yield the minimum required bandwidth or slew rate. When the Enable input is pulled low, the output will tend to remain at its last level, because of the charge remaining on the compensating capacitor.

APPLICATION NO. 9

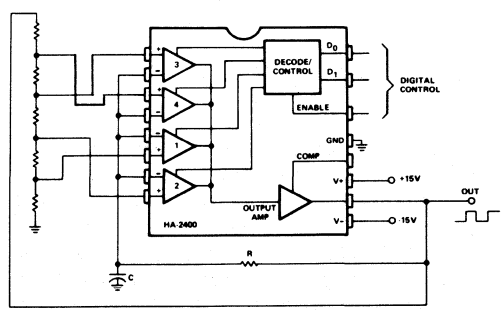


SINE WAVE OSCILLATOR PROGRAMMABLE FREQUENCY

Any oscillator which can be constructed using an op-amp, such as the twin-T, phase shift, crystal controlled types, etc. can be made programmable by using the HA-2400. Illustrated above is a Wien Bridge type, which is very popular for signal generators, since it is easily tunable over a wide frequency range, and has a very low distortion sine wave output. The frequency determining networks can be designed from about 10Hz to greater than 1MHz. Output level is about 6.0V RMS. By substituting a programmable attenuator (Circuit No. 4) for the Buffer Amplifier, a very versatile sine wave source for automatic testing, etc. can be constructed.

CHALLENGE: A high Q, narrow band filter can be made by feeding back greater than 1/3 of the output to the negative input. Design a circuit using the HA-2400 and an RC network which can be programmed either to generate or to detect an audio tone of the same frequency. Such a circuit would be quite useful for data communications.

APPLICATION NO. 10



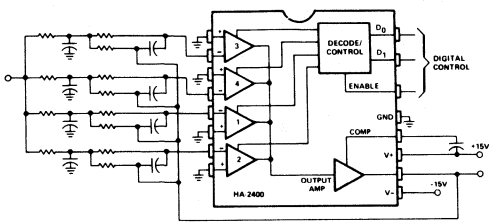
MULTIVIBRATOR, FREE RUNNING, PROGRAMMABLE FREQUENCY

This is the simplest of any programmable oscillator circuit, since only one stable timing capacitor is required. The output square wave is about 25.0V peak-to-peak and has

rise and fall times of about 0.5 μs. If a programmable attenuator circuit (No. 4) is placed between the output and the divider network, 16 frequencies can be produced with two HA-2400's and still only one timing capacitor.

A precision programmable square-triangle generator can also be constructed by adapting circuit described in Harris Application Note 507 to the HA-2400.

APPLICATION NO. 11



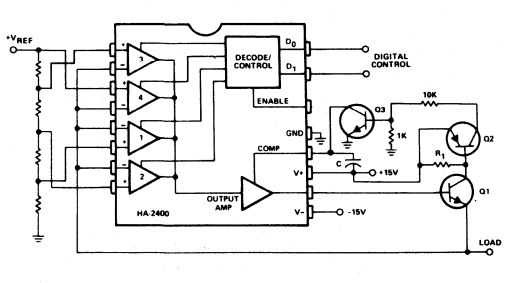
ACTIVE FILTER PROGRAMMABLE

Shown above is a second order low pass filter with programmable cutoff frequency. This circuit should be driven from a low source impedance since there are paths from the output to the input through the unselected networks.

Virtually any filter function which can be constructed with a conventional op-amp can be made programmable with the HA-2400.

A useful variation would be to wire one channel as a unity gain amplifier, so that one could select the unfiltered signal, or the same signal filtered in various manners. These could be cascaded to provide a wide variety of programmable filter functions.

APPLICATION NO. 12

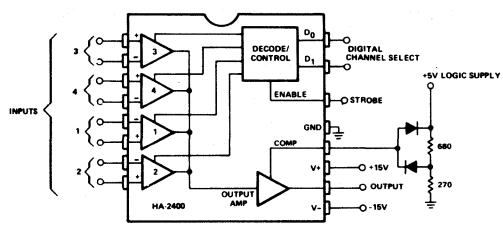


POWER SUPPLY PROGRAMMABLE

Many systems require one or more relatively low current voltage sources which can be programmed to a few predetermined levels. It is no longer necessary to purchase a programmable power supply with far more capability than needed. The circuit shown above produces positive output levels, but could be modified for negative or bipolar outputs. Q1 is the series regulator transistor, selected for the required current and power capability. R1, Q2 and Q3 form an optional short circuit protection circuit, with R1 chosen to drop about 0.7V at the maximum output current. The compensation capacitor, C. should be chosen to keep the overshoot, when switching, to an acceptable level.

CHALLENGE: Design a supply using only two HA-2400's which can be programmed to 16 binary weighted (or 10 BCD weighted) output levels.

APPLICATION NO. 13



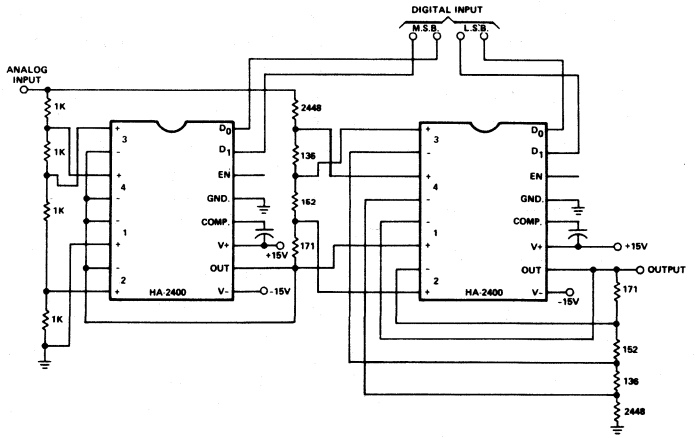
COMPARATOR, FOUR CHANNEL

When operated open loop without compensation, the HA-2400 becomes a comparator with four selectable input channels. The clamping network at the compensation pin limits the output voltage to allow DTL or TTL digital circuits to be driven with a fanout of up to ten loads.

Output rise and fall times will be about 100ns for differential input signals of several hundred millivolts, but will be in the microsecond region for small differential signals.

The circuit can be used to compare several signals against each other or against fixed references; or a single signal can be compared against several references. A "window comparator", which assures that a signal is within a voltage range, can be formed by monitoring the output polarity while rapidly switching between two channels with different reference inputs and the same signal input.

APPLICATION NO. 14



MULTIPLYING D TO A CONVERTER

The circuit above performs the function, $V_{OUT} = V_{IN} \cdot \frac{N}{16}$, where N is the binary number from 0 to 15 formed by the digital input. If the analog input is a fixed D.C. reference, the circuit is a conventional 4-bit D to A. The input could also be a variable or A.C. signal, in which case the output is the product of the analog signal and the digital signal.

The circuit on the left is a programmable attenuator with weights of 0, 1/4, 1/2 or 3/4. The circuit on the right is a non-inverting adder which adds weights to the first output of 0, 1/16, 1/8 or 3/16.

If four quadrant multiplication is required, place the Phase Selector circuit (No. 6) in series with either the analog input or output. The D_0 input of that stage becomes the + or – sign bit of the digital input.

MORE CHALLENGES

One of our favorite college textbooks paused at each climactic point with a statement to the effect that, "Proof of the following theorem is omitted, and is suggested as an exercise for the student."

The following is a list of some additional applications in which we believe the HA-2400 will prove very valuable. The "proofs", at present, remain as exercises for our ingenious readers.

- A to D Converter, Dual Slope Integrating
- Active Filter, State Variable Type with Programmable Frequency and/or Programmable "Q"
- Amplifier with Programmable D.C. Level Shift
- Chopper Amplifiers
- Crossbar Switches
- Current Source, Programmable
- F.M. Stereo Modulator
- F.S.K. Modem
- Function Generators, Programmable
- Gyrator, Programmable
- Monostable Multivibrator, Programmable
- Multiplier, Pulse Averaging
- Peak Detector with Reset
- Resistance Bridge Amplifier/Comparator with Programmable Range
- Sense Amp/Line Receiver with Programmable Threshold
- Spectrum Analyzer, Scanning Type
- Sweep Generator, Programmable
- Switching Regulator
- Touch-Tone™ Generator/Detector (Use Harris HD-0165 Keyboard Encoder I.C.)

FEEDBACK

We believe we have only scratched the surface of possible applications for a multiple channel operational amplifier.

If you have a solution for any of the previous "challenges" or any new application, please let us know. Anything from a one word description to a tested design will be welcome.

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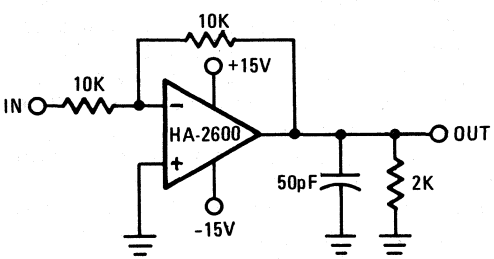
APPLICATION NOTE 515

OPERATIONAL AMPLIFIER STABILITY: INPUT CAPACITANCE CONSIDERATIONS

BY DON JONES

This is the first in a series of notes dealing with stabilization and optimization of A.C. response in operational amplifiers. One of the more common difficulties in applying operational amplifiers will be discussed.

Let's consider the unity gain inverting amplifier circuit shown below:



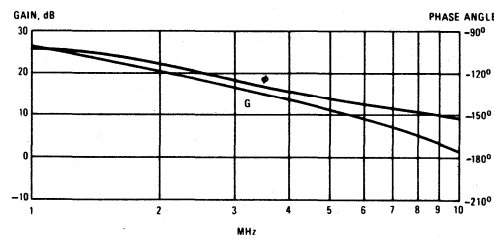
This appears to be a straightforward application with reasonable component values.

But, with the input grounded, the circuit output shows an oscillation at about 5 MHz.

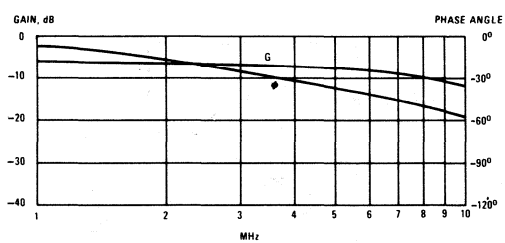
Even more surprising, if the same device is connected as a voltage follower with the same load, it is perfectly stable. Since the inverting amplifier has 6 dB less feedback than the voltage follower, shouldn't it be more stable?

The culprit here is capacitance at the amplifier inverting input. The HA-2600 in the TO-99 can has an input capacitance of about 2 or 3 pF. When soldered on a P.C. card, or inserted in a socket, wiring capacitance might add another 3 to 6 pF. With only 5K effective resistance at this point, 5 to 10 pF seems pretty negligible, doesn't it? But let's find out.

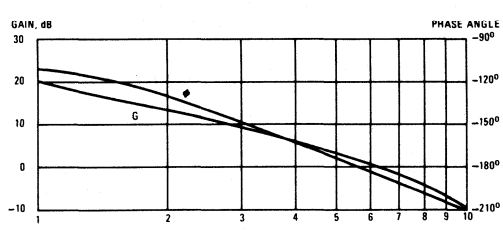
The open loop amplitude and phase response characteristics of the amplifier between 1 and 10 MHz looks like this:



The characteristics of the feedback network alone with 5 pF capacitance to ground looks like this:



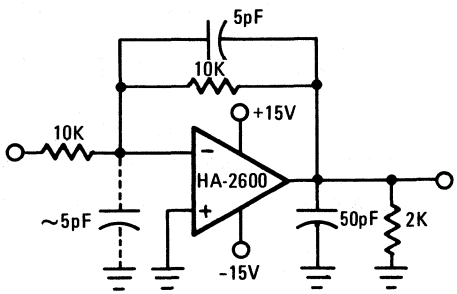
Combining these two graphs by algebraically adding the dB gains together and adding the phase shifts together gives us the open loop response at the summing point:



6

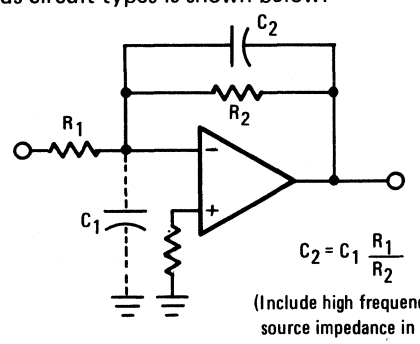
We can see that on the composite response curves, the phase shift crosses 180° at 5.5 MHz, and that there is still about +2 dB of gain at this frequency. Therefore, closing the loop automatically creates an oscillator.

How can we overcome this effect? If we add a capacitor across the feedback resistor, we can cancel the effects of the input capacitance:

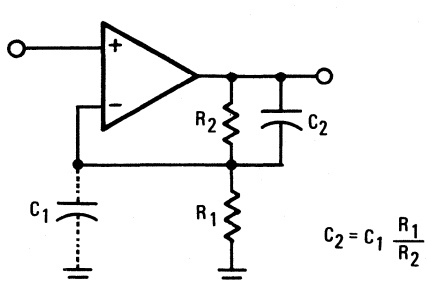


If the feedback capacitance matches the input capacitance, the response curves of the feedback network alone will be a flat -6 dB and 0° across the frequency band. The composite curves will then show a bandwidth of 7.5 MHz and a positive phase margin of 33°. So the circuit will now be quite stable. It's amazing how much difference that small capacitance can make.

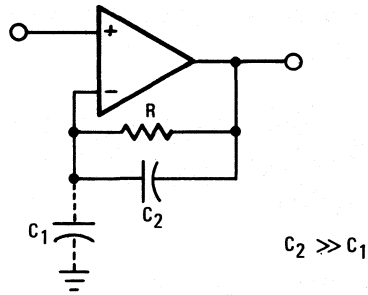
The general scheme for compensation of various circuit types is shown below:



INVERTING AMPLIFIER



NON-INVERTING AMPLIFIER



FOLLOWER WITH FEEDBACK RESISTOR

It's not really necessary to know the exact value of stray capacitance, C_1 - for most layouts, about 5 to 10 pF is a good guess. Unless you are trying to squeeze out the last Hz of frequency response, it doesn't hurt to guess on the high side. At higher gains, where C_2 calculates out to less than 1 or 2 pF, it isn't necessary to use C_2 - but it won't disturb anything if you do use it.

If you are uncertain about whether compensation is necessary, check the pulse response or frequency response of the closed loop stage. Hook a pulse generator to the input, and adjust the amplitude for about a 200 millivolt step at the output - if the output overshoot is less than 40% of the step, the circuit will be stable. Alternately, check the small signal frequency response of the stage - if the high frequency peaking is less than +6 dB, more than the low frequency gain, the circuit is stable. Of course, you can increase the compensation capacitor if you need even smoother response.

The phenomena we have described are not peculiar to any one amplifier type. Wideband amplifiers require a little more care in the design of feedback networks; but the same type oscillations will show up on 741 type amplifiers with higher feedback resistor values.

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APPLICATION NOTE
516

THE HA-2530/2535 WIDEBAND HIGH SLEW INVERTING AMPLIFIER

BY ERNIE THIBODEAUX

INTRODUCTION

The HA-2530/2535 is a monolithic inverting amplifier constructed using the Harris dielectric isolation process. It incorporates both bipolar and MOS devices on the same chip allowing excellent D.C. characteristics not normally achieved in most high performance A.C. amplifiers. The HA-2530/2535 is a continuation of the HA-2500 family of high slew rate amplifiers and represents a factor of 3 improvement in A.C. performance over the HA-2520 op amp. Its superior A.C. performance is achieved by using a two amplifier feedforward scheme on the same chip. Among the many applications best suited for this device are video amplifiers/linedrivers, high speed integrators, signal separators, waveform generators, A/D, D/A and sampled data systems. This application note will briefly discuss the internal circuitry, show how closed-loop frequency response can be predicted and present a few of the above mentioned applications.

INSIDE THE HA-2530/2535

The detailed schematic shown in Figure 1 can be simplified with the functional diagram shown in Figure 2.

Amplifier A_1 is a low frequency, high gain stage providing high accuracy at low frequencies with excellent D.C. input characteristics while A_2 is a high frequency, relatively low gain stage that dominates and controls the overall amplifier response at high frequencies. The overall input bias current is the sum of the bias currents of both amplifiers but A_2's MOSFET input stage adds little to the overall current. The high offset voltage of the MOSFET is of no significant consequence, since this offset is divided by the high open

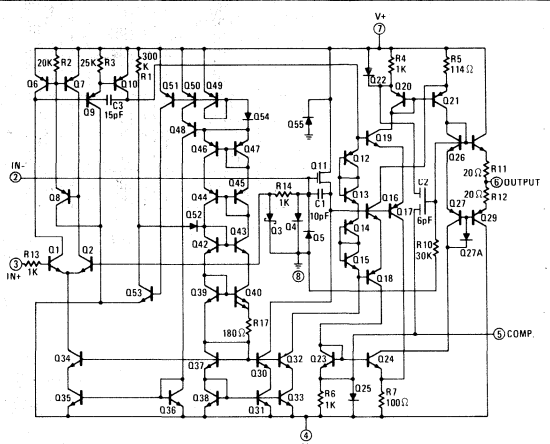


Figure 1

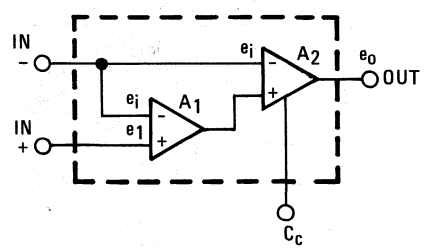


Figure 2

loop gain of A_1. Therefore, the effective D.C. input characteristics of the composite amplifier are that of A_1 alone.

The overall amplifier gain is given by the algebraic sum of the amplifier transfer functions. That is, referring to Figure 2, the open loop equation can be written as:

$$e_o = [(e_1 - e_i)A_1 - e_i]\,A_2 \qquad \text{Equation (1)}$$

6

BODE PREDICTION OF OPEN-LOOP
RESPONSE USING EQ. (5)

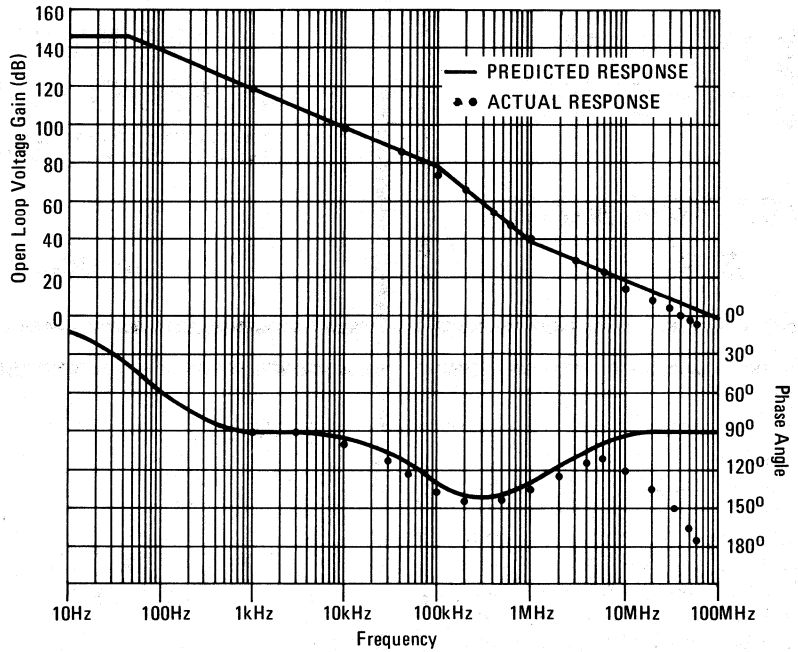


Figure 3

OPEN-LOOP RESPONSE vs.
COMPENSATION CAPACITANCE

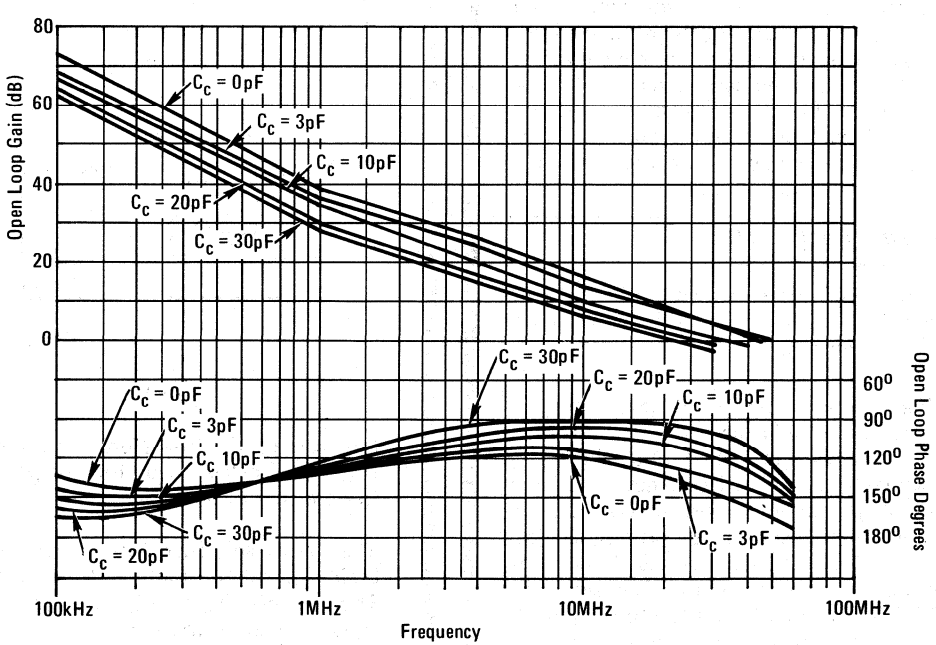


Figure 4

For the inverting configuration $e_1 = 0$ and the total amplifier gain is:

$$A_T = -(A_1A_2 + A_2) \quad \text{Equation (2)}$$

$$\text{Where} \quad A_1(S) = \frac{G_1}{1 + T_1S} \quad \text{Equation (3)}$$

$$A_2(S) = \frac{G_2}{1 + T_2S} \quad \text{Equation (4)}$$

Solving for the overall transfer function results in the following expression:

$$A_T(S) = \frac{G_1G_2[1 + 1/G_1 + (T_1/G_1)S]}{(1 + T_1S)(1 + T_2S)} \quad \text{Equation (5)}$$

Since the D.C. voltage gain (G_1) of amplifier A_1 is typically 20,000 V/V then $1/G_1 << 1$ resulting in:

$$A_T(S) = \frac{G_1G_2\left(1 + \frac{T_1}{G_1}S\right)}{(1 + T_1S)(1 + T_2S)} \quad \text{Equation (6)}$$

The composite transfer function reveals a D.C. gain equal to the product of the D.C. gains of each amplifier (G_1G_2), a pole at the break frequency of each amplifier and a zero at the unity gain frequency of amplifier A_1. The amplifier was designed using the following:

$G_1 = 22K$ Poles: $f_{p1} = 48Hz$
$G_2 = 940$ $f_{p2} = 100kHz$
$f_{z1} = 1MHz$

A comparison of the calculated open-loop response with the actual under no load and no compensation conditions is shown in Figure 3. The two curves compare very closely up to approximately 6MHz where higher order effects dominate, causing the response to deviate from the predicted. The effect of adding compensation capacitance is to lower the pole frequency of A_2 while adding a high frequency zero. Several response curves for different compensation capacitors are shown in Figure 4.

CURVE FITTING THE HA-2530 OPEN LOOP RESPONSE

In many instances a closed-form equation defining completely the characteristics of the HA-2530 beyond it's predictable bandwidth given by Equation 6 would be desirable. This would allow modeling the device on a computer or calculator resulting in the prediction of system performance for various closed-loop configurations. Using a trial and error graphical procedure, a close-fit beyond 6MHz was obtained using several poles and a simple zero as shown below.

$$A_0(S) = \frac{1 + T_6S}{(1 + T_3S)(1 + T_4S)(1 + T_5S)} \quad \text{Equation (7)}$$

Poles: $f_{p3} = 6MHz$ Zero: $f_{z6} = 7MHz$
$f_{p4} = 30MHz$
$f_{p5} = 150MHz$

A comparison of the actual uncompensated ($C_C = 0$) response with that given by Equation 7 above is shown in Figure 5. Combining Equation 6 and 7, the calculated open-loop transfer function from D.C. to 50MHz is obtained.

APPROXIMATION OF HIGH FREQUENCY CHARACTERISTIC USING EQUATION (7)

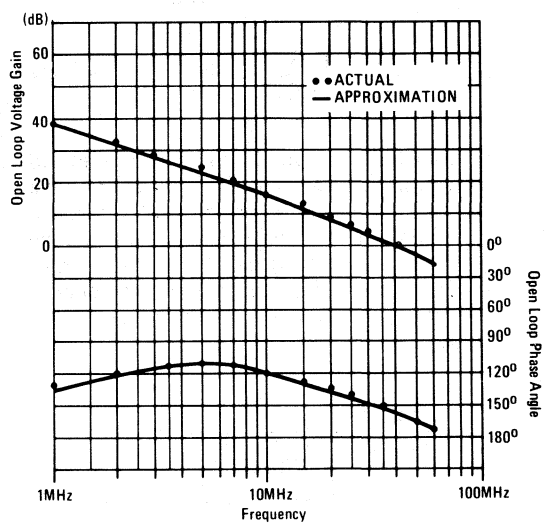


Figure 5

$$A_T'(S) = A_0(S) \cdot A_T(S) = \frac{G_1G_2(1+T_1/G_1S)(1+T_6S)}{(1+T_1S)(1+T_2S)(T+T_3S)(1+T_4S)(1+T_5S)}$$

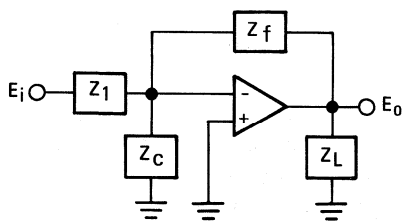
Equation (8)

This equation represents a working transfer function for the typical HA-2530/2535 and may be useful in many synthesis applications.

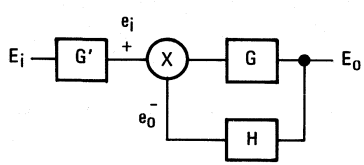
THE INVERTING AMPLIFIER

GENERAL REPRESENTATION

Consider the general inverting configuration below:

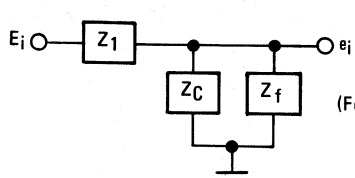


The control system representation of the circuit is:



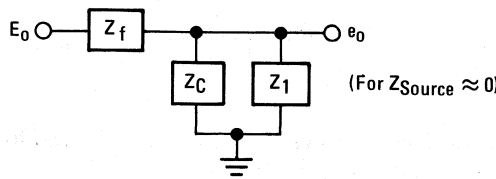
Where: $\frac{E_o}{E_i} = \frac{-G'G}{1+GH}$ **Equation (9)**

The transfer functions G' and H can be solved very simply by assuming the ideal operational amplifier and using the principle of superposition. First, G' is calculated by disconnecting the amplifier summing point from the rest of the circuit and calculating the voltage e_i with ideal voltage source E_i impressed as shown below.



$$G' = \frac{e_i}{E_i} = \frac{Z_cZ_f}{Z_1Z_c + Z_1Z_f + Z_cZ_f}$$ **Equation (10)**

The feedback transfer function is calculated similarly by calculating e_o with E_o impressed.



$$H = \frac{e_o}{E_o} = \frac{Z_cZ_1}{Z_fZ_1 + Z_fZ_c + Z_cZ_1}$$ **Equation (11)**

Writing G' in terms of H we have:

$$G' = (Z_f/Z_1)(H)$$ **Equation (12)**

Finally, the closed-loop transfer function is obtained below by combining Equation 9 and Equation 12.

$$\frac{E_o}{E_i} = \frac{-Z_f}{Z_1}\left[\frac{GH}{1+GH}\right]$$ **Equation (13)**

As will be seen later, the closed-loop equation is in a very convenient form for the graphical evaluation of closed-loop response.

PHASE MARGIN DETERMINATION

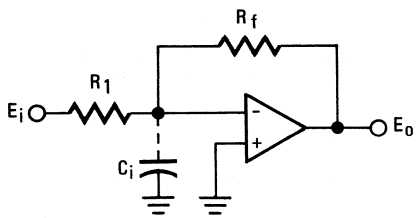
Phase margin for the unity gain inverting amplifier is not evaluated at the 0dB crossing of the open loop gain response as might be expected. By definition phase margin is evaluated when the magnitude of the loop gain |GH| is 1. For the non-inverting amplifier the feedback factor (H) is unity (full feedback) and phase margin is evaluated at |G| = 1 or 0dB. However, for the unity gain inverting amplifier H is 1/2 (equal voltage division caused by input and feedback resistors) so that phase margin is evaluated at |G| = 2 or 6dB.

In general, for the inverting amplifier, the phase margin would be determined at:

$$|G| = \frac{R_1 + R_f}{R_1}$$ **Equation (14)**

EFFECTS OF INPUT CAPACITANCE ON HIGH FREQUENCY STABILITY

The effects of input capacitance (C_i) can probably best be illustrated by evaluating phase margin under this condition. Calculating the feedback factor, H, from the circuit below:



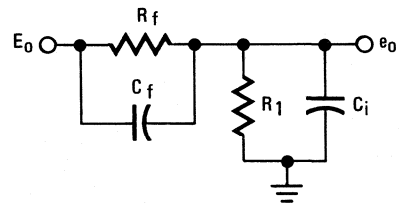
We obtain from Equation 11:

$$H = \frac{R_1/(R_f + R_1)}{1 + S(R_{1f}C_i)}$$

where $R_{1f} = R_1 \,||\, R_f$ **Equation (15)**

Therefore, the input capacitance creates a pole at wp = $1/R_{1f}C_i$ producing additional phase shift about this frequency. This will reduce the phase margin resulting in possible oscillation. For example, if $R_1 = R_f = 2K$ and $C_i = 10pF$, the pole frequency is found to be fp = 16MHz. The loop gain plot $(GH)_i$ in Figure 6 reveals a perfect oscillatory condition at 18MHz; i.e. IGHI = 0dB and ϕ_i (phase margin) = 0. If input capacitance were neglected, our prediction would have erroneously resulted in a phase margin (ϕ_o) of 38°.

The effects of input capacitance can be cancelled by adding a feedback capacitor (C_f) across resistor R_f. Recalculating H from the feedback network below:



We have:

$$H = \frac{[R_1/(R_1 + R_f)](1 + SR_fC_f)}{1 + SR_{1f}(C_i + C_f)}$$ **Equation (16)**

From this equation we see that adding C_f creates a zero that can be adjusted to cancel the denominator pole, resulting in a pure resistive feedback factor.

The condition for this cancellation is:

$$R_fC_f = R_{1f}(C_i + C_f)$$ **Equation (17)**

or

$$C_f = (R_1/R_f)C_i$$ **Equation (18)**

For unity gain, the feedback capacitance should equal the input capacitance. Adding C_f for gains greater than 10 becomes academic, since C_f calculates to be less than 1pF. Although adding C_f alleviates phase shift caused by C_i, it should be noted that it also creates a closed-loop pole at $1/R_fC_f$ that could limit the attainable bandwidth. For example, if the 6dB open-loop bandwidth is 30MHz, $C_i = C_f = 10pF$, and $R_1 = R_f = 2K$, the closed-loop pole occurs at 8MHz causing the frequency response to roll-off prematurely at this frequency. Decreasing the resistor values by a factor of 4 would increase the pole frequency to 32MHz and the attainable bandwidth would only be limited by the open-loop bandwidth and not the external circuit components. However, care must be taken not to make input and feedback resistors too small, since loading problems may result. That is, the input resistor, R_1, represents a load to the

input driving source, since R_1 is connected to the amplifier summing point which is at "virtual" ground. Furthermore, the feedback resistor, R_f, loads the amplifier output for the same reason.

EFFECTS OF INPUT CAPACITANCE ON PHASE MARGIN

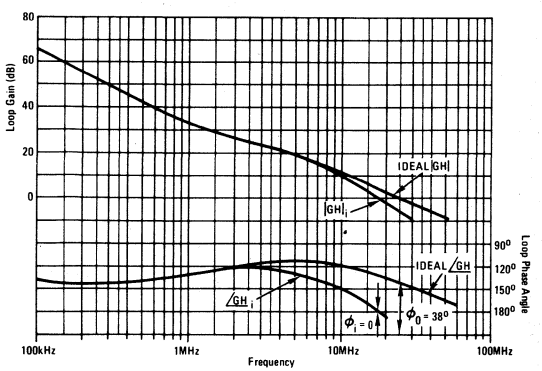


Figure 6

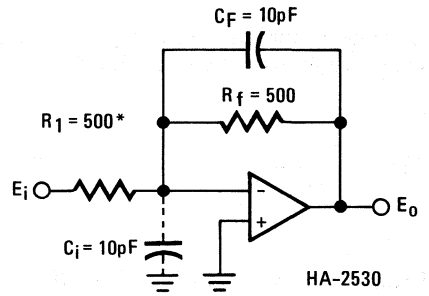
In summary, the effects of input capacitance can be negated by providing a feedback capacitor according to Equation 18. For closed-loop gains greater than 10, no feedback capacitor is required. Finally, trade-offs between maximum bandwidth, circuit component values and stability will have to be made in most cases.

PREDICTION OF CLOSED-LOOP RESPONSE USING A GRAPHICAL PROCEDURE

The closed-loop response of any amplifier can be graphically determined from its open-loop response curve. The generalized closed-loop transfer function is restated and given below:

$$\frac{E_o}{E_i} = -\frac{Z_f}{Z_1}\left[\frac{GH}{1+GH}\right] \qquad \textbf{Equation (19)}$$

The graphical procedure using the Nichols chart (Figure 7) conveniently determines the above function in brackets from the amplifier loop gain (GH) plot. Using the following circuit, let's graphically obtian its closed loop response and compare it with actual experimental results.



*Note: $R_1 = R_f = 500\ \Omega$
Chosen to obtain maximum bandwidth.

The complete procedure is:

(1) Plot both gain and phase of the GH function on semi-log paper (see ideal GH curve Figure 6). The following points were tabulated:

f (MHz)	1	2	4	6	10	15
|GH| (dB)	33	26	21	17	12	6
∠GH	-132°	-120°	-114°	-114°	-120°	-128°
f (MHz)	17	20	25	30	38	42
|GH|(dB)	5	3	0	-2	-5	-7
∠GH	-132°	-137°	-142°	-148°	-155°	-160°

(2) Transfer gain/phase points obtained above at selected frequencies to create a smooth curve on the Nichols chart using the rectangular coordinates.

(3) Obtain directly from the chart gain/phase of the function ($\frac{GH}{1+GH}$) at the selected data points. The following was tabulated:

f (MHz)	1	2	4	6	10	15
$\left\lvert\frac{GH}{1+GH}\right\rvert$ (dB)	0.14	0.22	0.3	0.45	0.7	2
$\angle\frac{GH}{1+GH}$	-1°	-2.5°	-5°	-8°	-15°	-30°
f (MHz)	17	20	25	30	38	42
$\left\lvert\frac{GH}{1+GH}\right\rvert$ (dB)	2.3	3.2	4.0	3.5	0	-2.5
$\angle\frac{GH}{1+GH}$	-35°	-45°	-70°	-75°	-130°	-145°

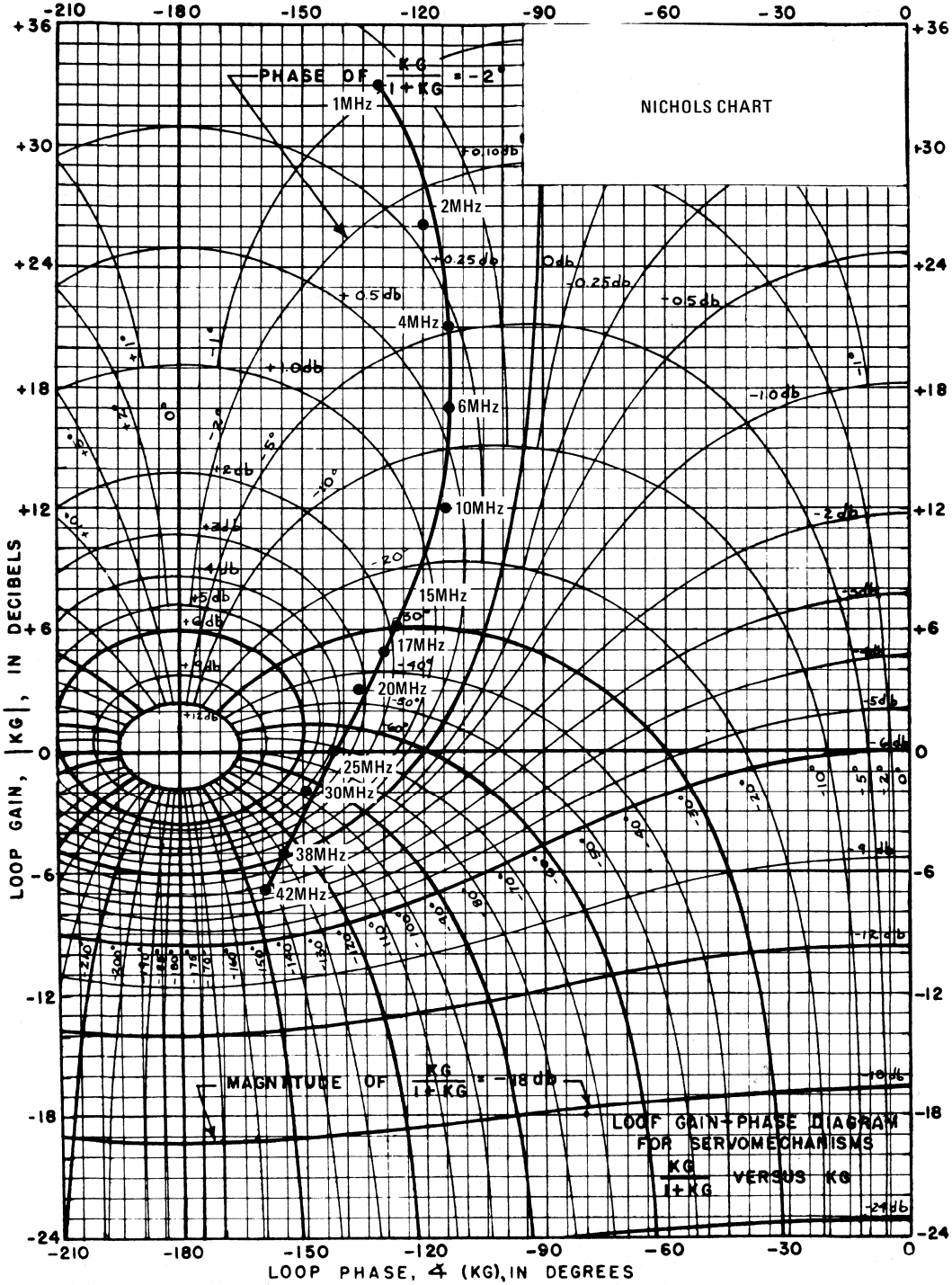

NICHOLS CHART
PHASE OF KG/(1+KG) = -2°
MAGNITUDE OF KG/(1+KG) = -18 db
LOOP GAIN+PHASE DIAGRAM FOR SERVOMECHANISMS
KG/(1+KG) VERSUS KG
1MHz
2MHz
4MHz
6MHz
10MHz
15MHz
17MHz
20MHz
25MHz
30MHz
38MHz
42MHz
+0.25db
+0.5db
+1.0db
+2db
+4db
+5db
+6db
+12db
0db
-0.25db
-0.5db
-1.0db
-2db
-3db
-4db
-5db
-6db
-12db
-18db
-24db
LOOP GAIN, |KG|, IN DECIBELS
LOOP PHASE, ∠ (KG), IN DEGREES
-210 -180 -150 -120 -90 -60 -30 0
+36 +30 +24 +18 +12 +6 0 -6 -12 -18 -24

Figure 7

(4) Transfer these points to semi-log paper and add the pole given by $w = \frac{1}{R_f C_f}$ (or f_p = 32MHz for this case) to obtain the calculated closed-loop response, $(\frac{E_o}{E_i})_{CALC}$ shown in Figure 8.

(5) Obtain Bandwidth, Peaking and closed-loop phase margin from the closed-loop response given in Figure 8.

Comparing the actual closed-loop response with that of our prediction, we see that favorable results were obtained. The performance specifications are:

PREDICTION OF CLOSED LOOP RESPONSE USING NICHOLS CHART

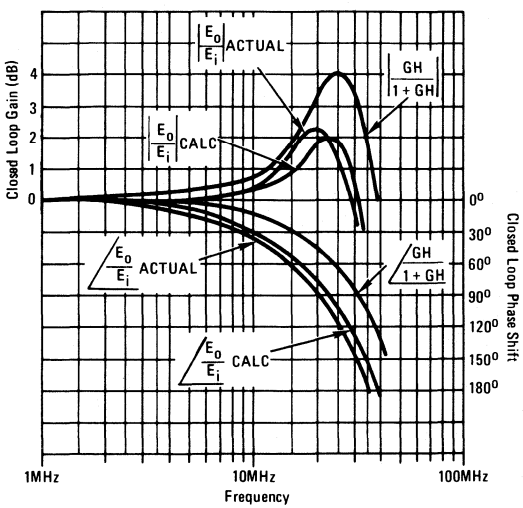


Figure 8

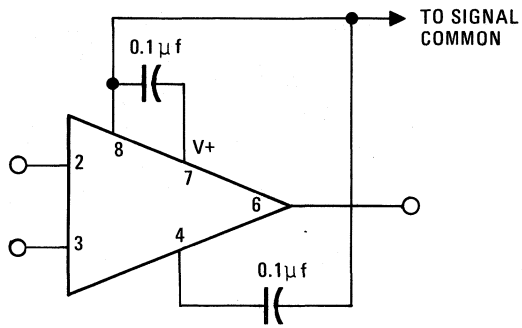
	ACTUAL	PREDICTED
Bandwidth(0dB)	29MHz	31MHz
Closed Loop Phase Margin	39°	42°
Mp (peaking)	2.3dB	2dB

SPECIAL CONSIDERATIONS FOR OPTIMUM PERFORMANCE

INTRODUCTION

Obtaining the best performance from high frequency amplifiers is not always easy. External components, deoupling, stray wiring capacitance and long lead lengths are a few of the culprits that can take a 30MHz amplifier and convert it to a 3MHz amplifier with no effort at all. However, we can avoid these shortcomings if a few simple rules are followed:

(1) Decouple as close to the amplifier pins as possible. In fact, decoupling the HA-2530 as shown below will give best results.



(2) Know your decoupling caps: At RF frequencies decoupling capacitors may look like an inductor and/or resistor. Select a good H.F. ceramic.

(3) Orient components to minimize stray capacitance.

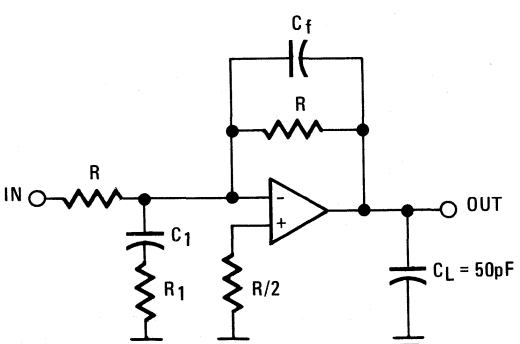
(4) Keep leads short to minimize inductance and prevent ground loop problems.

(5) Keep input and feedback resistor values as small as practical; they react with stray and input capacitance.

(6) Minimize loading capacitance; it affects settling time and stability (see how in next section).

CIRCUIT FOR OPTIMUM SETTLING TIME

Before we investigate settling time, let's take a look at phase margin with a capacitive load of $C_L = 50pF$. The effects of load capacitance can be seen by referring to the uncompensated phase response shown in Figure 9. Note the phase margin reduction from approximately 38° (Figure 3) to only 4°; a marginally stable condition with a long settling time. The load capacitance effectively causes a high frequency pole whose break frequency is $\frac{1}{2\pi R_{OUT} C_L}$, where R_{OUT} is the approximate output resistance of the amplifier. The additional phase shift that C_L adds will give us some hint as to the pole location. That is, at 25MHz, about 34° is added to the unloaded response resulting in a pole frequency of about 40MHz. Using this break frequency, R_{OUT} calculates to be about 80 ohms. This bit of information may prove useful in evaluating closed-loop response against various capacitive loads. At this point, let's see how we can improve phase margin to improve settling time. Consider the circuit below consisting of the pole-zero compensating network ($R_1 - C_1$).



OPEN LOOP RESPONSE USING POLE-ZERO COMPENSATION AND $C_L = 50pf$

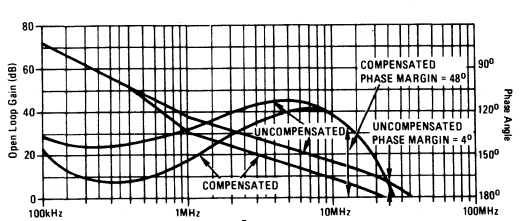


Figure 9

CIRCUIT FOR OPTIMUM SETTLING TIME (continued)

The $R_1 - C_1$ network will increase phase margin by sacrificing a small amount of bandwidth at no expense to slew rate. Slew rate is not affected as long as the voltage divider made up of the input resistor (R) and $R_1 \parallel R$ provides an instantaneous voltage at the summing point that will be sufficient to slew the amplifier. Assuming a single pole response and a bandwidth of 25MHz, this voltage to a first approximation should be greater than 1.8 volts.

The network forces an increase in phase margin by rolling-off the amplifier gain response without affecting phase response at the bandwidth frequency. The pole-zero locations are chosen at frequencies where the loop gain is large enough to buffer the error effects caused by the additional phase shift of the network in this region. Component values are chosen to satisfy the slew condition and neutralize high frequency phase shift caused by the input capacitance according to the relationship.

$$(R_1 \parallel R)C_i = RC_f \qquad \text{Equation (20)}$$

The following values were determined experimentally for optimum settling time and satisfy the conditions mentioned previously.

$R = 2K\Omega$ $\quad C_1 = 250pF$ $\quad C_i = 10pF$
$R_1 = 620\Omega$ $\quad C_f = 3pF$

The pole-zero locations are approximately:

$$\text{Pole: } f_{pl} = \frac{1}{2\pi(R/2 + R_1)C_1} = 400kHz$$

$$\text{Zero: } f_{zl} = \frac{1}{2\pi R_1 C_1} = 1MHz$$

The compensated open-loop response curve shown in Figure 9 shows the effects of the pole-zero additions. Note how its phase response deviates from the uncompensated at frequencies less than 10MHz but coincides

above this frequency allowing a phase margin of 48° to be achieved. From experimental data using a 10V pulse, a typical settling time to 0.1% of 550ns was achieved. Settling times to 0.1% for various compensation capacitors without the pole-zero network are shown in the table below.

	C_C	0pF	3pF	10pF	20pF	30pF
C_L = 0pF	T_S(ns)	500	540	620	760	880
C_L = 50pF	T_S(ns)	Unstable	650	740	840	940

Looking at the table, we see that the best settling time without the pole-zero compensating network is 650ns with C_C = 3pF. This will suffice for most pulse applications but optimum settling is still obtained with the pole-zero network.

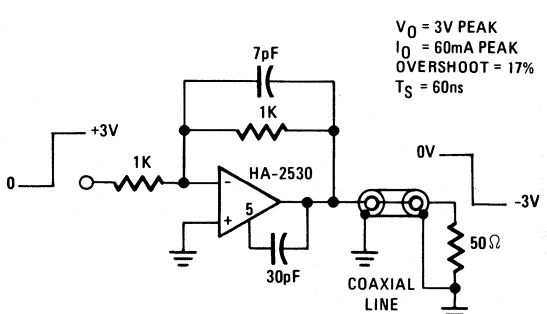
APPLICATIONS

INTRODUCTION

In all the applications to be discussed the HA-2530 is used as an inverting amplifier. Usage as a non-inverting amplifier can be used but the common mode range is limited to about ±0.5V because the inverting input is diode-clamped to signal ground. Usable bandwidth in this mode is only about 100kHz.

APPLICATION 1
FAST SETTLING COAXIAL DRIVER

The circuit below is intended for use in line driving systems requiring good settling at high output current levels; such as radar pulse drivers, video sync driver, PAM line driver, etc.

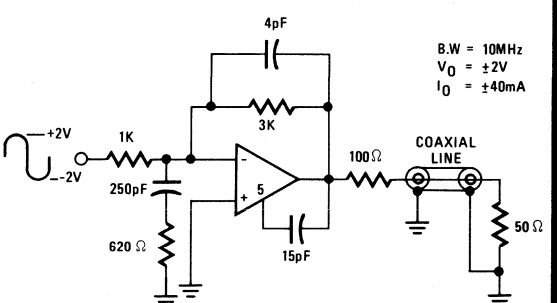


The input voltage source supplies only 3mA at 3 volts into the driver circuit which develops an output current drive of 60mA into a 50 ohm load. At these low voltage levels, the HA-2530 relies chiefly upon its excellent gain bandwidth product resulting in a 5% settling time of 60ns.

Although the HA-2530 is capable of providing high output current, special attention should be given to the input duty cycle so that the maximum power dissipation of the device is not exceeded; especially if operating at high ambient temperatures (consult data sheet for details).

APPLICATION 2
10MHz COAXIAL LINE DRIVER

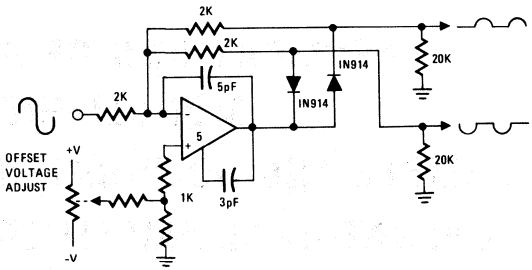
The circuit shown below will find excellent usage in high frequency line driving systems that require wide-power bandwidths at high output current levels.



The bandwidth of the circuit is limited only by the single pole response of the feedback components; namely $f_{-3dB} = \frac{1}{2\pi R_f C_f}$. As such, the response is flat with no peaking and yields minimum distortion.

APPLICATION 3
WIDE RANGE SIGNAL SEPARATOR

The high open-loop gain of the HA-2530 along with its high slew rate will allow a wide variation of input voltages and a wide frequency response as well. The circuit separates the input voltage into its positive and negative components. The diodes steer the positive and negative components to the

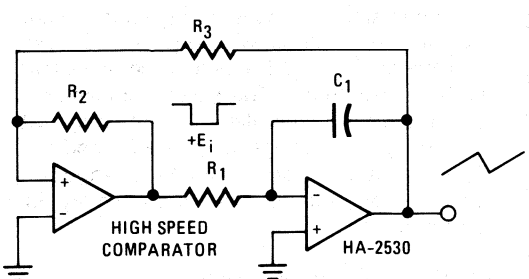


respective outputs. When placed in the feedback loop they virtually act as ideal diodes since the output error voltage is only the forward voltage drop divided by the loop gain of the amplifier. The two outputs can be driven into a differential amplifier to produce an absolute value circuit useful in many multiplier and averaging circuits.

Dynamic ranges between 60dB and 80dB can be obtained depending upon the maximum operating frequency. For example, in the circuit above a dynamic range from 5mV to 10 volts peak was easily obtained for a bandwidth of 100kHz without offset voltage adjustment. For a bandwidth of 1MHz, the range was 100mV to 10 volts peak. Dynamic ranges approaching 60dB at 1MHz can be obtained with proper offset voltage adjustment.

APPLICATION 4
HIGH FREQUENCY TRIANGULAR WAVE GENERATOR

Frequency generation well into the megahertz region can be realized with the HA-2530. Assuming circuit operation is not limited by the comparator's speed, operating frequencies between 1MHz and 5MHz can be achieved with the circuit below.



The integration time constant and circuit gain is set according to:

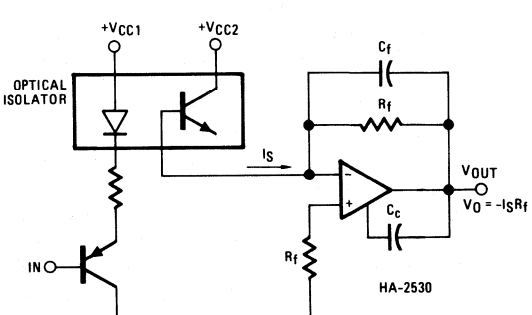
$$(a)\quad f = \frac{1}{4R_1C_1}\left(\frac{R_2}{R_3}\right)$$

$$(b)\quad \frac{E_o}{E_i} = -\frac{R_3}{R_2}$$

For accurate integration, the time constant, $\frac{R_3}{R_2}(R_1C_1)$, should be large compared to the unity gain frequency time constant and the comparator rise time. Also, the integrating capacitor, C_1, should be large in relation to the input capacitance of the amplifier while the resistors should be small to avoid reacting with stray and input capacitances. For larger output swings, another HA-2530 could be cascaded for amplification.

APPLICATION 5
CURRENT-TO-VOLTAGE CONVERTER

FET amplifiers used as current amplifiers offer the greatest resolution of current input because they have very low input bias currents. However, their input offset voltage and drift characteristics are very poor, sometimes adding to gross inaccuracies over temperature. The HA-2530 offers excellent offset voltage and drift characteristics (0.8mV, 5µV/°C) with low bias currents (17nA). The circuit below depicts the HA-2530 used to enhance the speed of an optical isolator interface. Operating the photo-transistor as a diode will increase speed at the expense of decreased current output. In this configuration the maximum current output may vary from 100µA to 400µA depending upon the LED pulse duration. At these current levels the errors of the HA-2530 are negligible and speed is limited only by the gain-bandwidth of the amplifier with attainable rise times of 20ns.



HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

APPLICATION NOTE 517

APPLICATIONS OF A MONOLITHIC SAMPLE-AND-HOLD/GATED OPERATIONAL AMPLIFIER

BY DON JONES

INTRODUCTION

The sample-and-hold or track-and-hold function is very widely used in linear systems. Until recently, this function was available only in modular or hybrid circuits; or perhaps most frequently the circuit was constructed by the user from an analog switch, a capacitor, and a very low bias current operational amplifier.

A high quality sample-and-hold circuit must meet certain requirements:

(1) The holding capacitor must charge up and settle to its final value as quickly as possible.

(2) When holding, the leakage current at the capacitor must be as near zero as possible to minimize voltage drift with time.

(3) Other sources of error must be minimized.

Design of a sample-and-hold, particularly the user built variety, involves a number of compromises in the above requirements. The amplifier or other device feeding the analog switch must have high current capability and be able to drive capacitive loads with stability. The analog switch must have both low ON resistance and extremely low OFF leakage currents. But, leakage currents of most analog switches (except the dielectrically isolated types) run to several hundred nanoamperes at elevated temperatures. The analog switch must have very low coupling between the digital input and analog output, because any spikes generated at the instant of turn-off will change the charge on the capacitor. The output amplifier must have extremely low bias current over the temperature range, and also must have low offset drift and sufficient slew rate; a combination satisfied by only a few available amplifiers.

THE HA-2420/2425

The HA-2420/2425 is the first complete monolithic sample-and-hold integrated circuit. A functional diagram is shown in Figure 1.

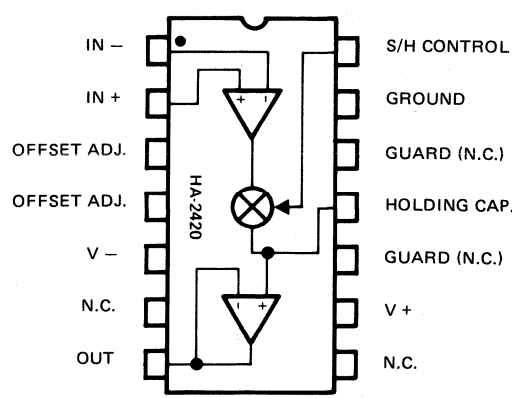


Figure 1 – HA-2420/2425 Functional Diagram

The input amplifier stage is a high performance operational amplifier with excellent slew rate, and the ability to drive high capacitance loads without instability. The switching element is a highly efficient bipolar transistor stage with extremely low leakage in the OFF condition. The output amplifier is a MOSFET input unity gain follower to achieve extremely low bias current.

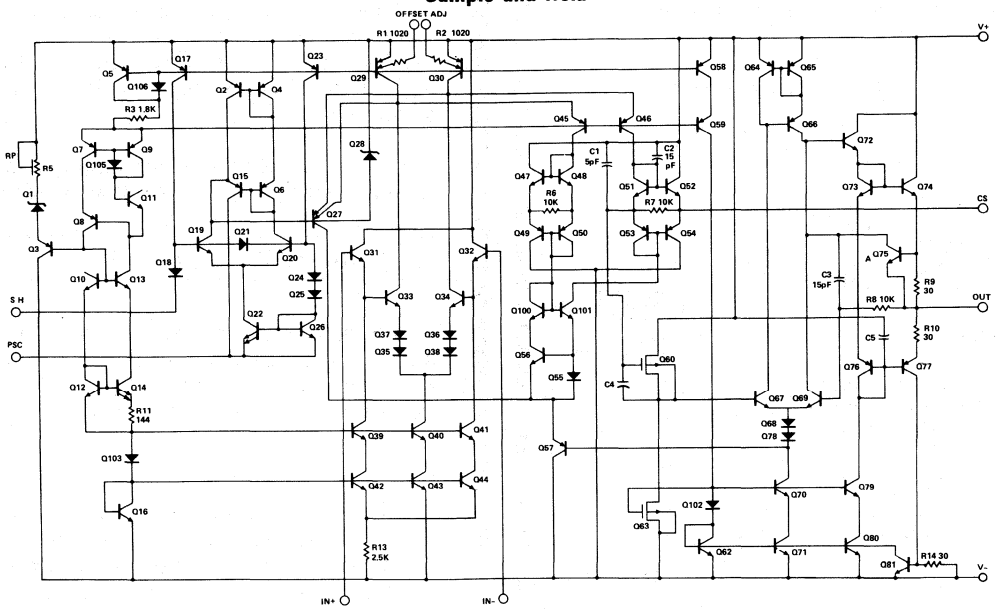
MOSFET inputs are generally not used for D.C. amplifiers because their offset voltage

drift is difficult to control. In this configuration, however, negative feedback is generally applied between the output and inputs of the entire device, and the effect of this offset drift at the inputs is divided by the open loop gain of the input amplifier stage.

The schematic of the HA-2420 is in Figure 2. During sampling (S/H control LOW) the signal path through the input amplifier stage starts at Q31-34, through Q45 and Q46, and then to the holding capacitor terminal through Q51-54. The output follower amplifier has its input at MOSFET Q60.

HA-2420/2425

Sample-and-Hold



NOTE: 1. Unless otherwise specified resistance values are in OHMS, capacitance values are in picofarads.

Figure 2

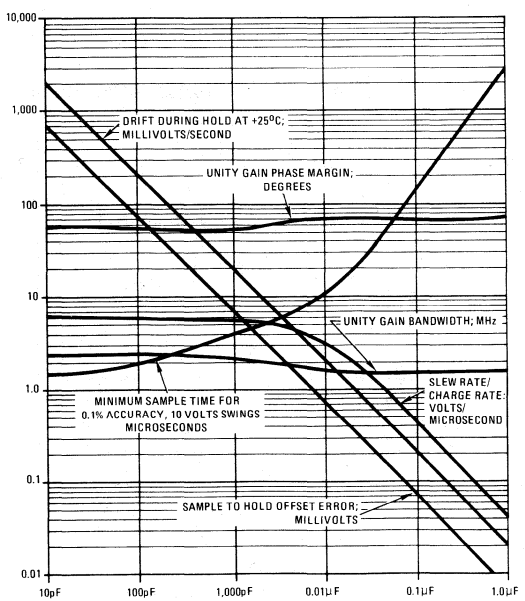


Figure 3 – Holding Capacitor, C_H

TYPICAL SAMPLE-AND-HOLD PERFORMANCE AS A FUNCTION OF HOLDING CAPACITANCE

In the "hold" mode, the S/H control is HIGH, so Q21 conducts, turning on Q27 which diverts the signal away from Q45 and Q46, and passes the signal to V - through Q57. Q57 also forces Q51-54 to ride up and down with the output signal, so there is virtually zero potential between these transistor bases and the voltage on C_H; completely eliminating leakage from C_H back into the input amplifier.

SAMPLE-AND-HOLD APPLICATIONS

A number of basic applications are shown on the following pages. The device is exceptionally versatile, since it can be wired into any of the hundreds of feedback configurations possible with any operational amplifier. In many applications the device will replace both an operational amplifier and a sample-and-hold module.

The larger the value of the timing capacitor, the longer time it will hold the signal without excessive drift; however, it will also reduce the

charging rate/slew rate and the amplifier bandwidth during sampling. So the capacitance value must be optimized for each particular application. The graph in Figure 3 shows these tradeoffs. Drift during holding tends to double for every 10°C rise in ambient temperature. The holding capacitor should have extremely high insulation resistance and low dielectric absorption-polystyrene (below +85°C), Teflon, or mica types are recommended.

Guard Ring Layout (Bottom View)

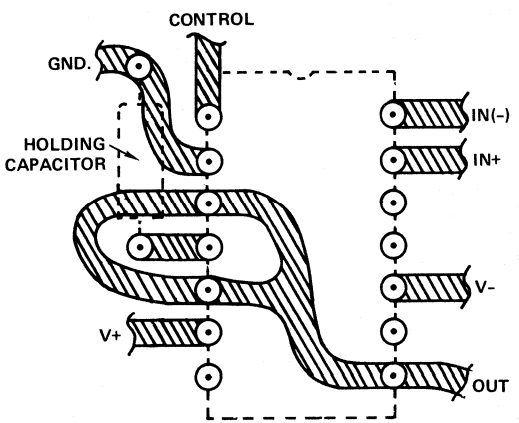


Figure 4

For least drift during holding, leakage paths on the P.C. board and on the device package surface must be minimized. Since the output voltage is nearly equal to the voltage on C_H, the output line may be used as a guard line surrounding the line to C_H. Then, since the potentials are nearly equal, very low leakage currents will flow. The two package pins surrounding the C_H pin are not internally connected, and may be used as guard pins to reduce leakage on the package surface. A suggested P.C. guard ring layout is shown in Figure 4.

GATED OPERATIONAL AMPLIFIER APPLICATIONS

An operational amplifier with a highly efficient analog switch in series with its output is a very useful building block for linear systems. The amplifier can be connected in any of the conventional op amp feedback configurations. With the switch closed, the circuit behaves as a conventional op amp with excellent bandwidth, slew rate, high output current capability, and is able to drive capacitive loads with good stability. With the switch open, the output node is an almost perfect open circuit.

The output buffer amplifier has extremely high input impedance and exceptionally low bias current, but is not particularly well suited for D.C. applications outside an overall feedback loop, since its offset voltage may be quite high.

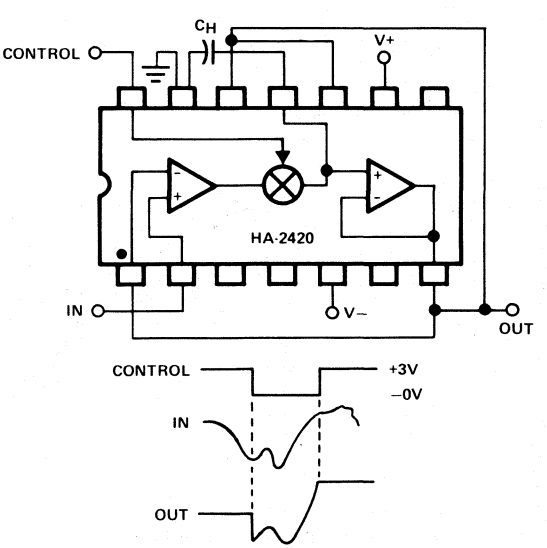
A number of possible gated amplifier applications are suggested in the following section.

APPLICATION NO. 1

Feedback is the same as a conventional op amp voltage follower which yields a unity gain, non-inverting output. This hookup also has a very high input impedance.

The only difference between a track-and-hold and a sample-and-hold is the time period during which the switch is closed. In track-and-hold operation, the switch is closed for a relatively long period during which the output signal may change appreciably; and the output will hold the level present at the instant the switch is opened. In sample-and-hold opera-

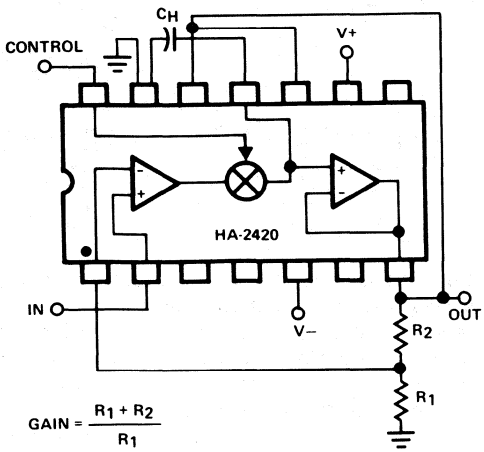
Basic Track-and-Hold/Sample-and-Hold



tion, the switch is closed only for the period of time necessary to fully charge the holding capacitor.

APPLICATION NO. 2

Sample-and-Hold With Gain



This is the standard non-inverting amplifier feedback circuit.

It illustrates one of the many ways in which the HA-2420 may be used to perform both op amp and sampling functions, eliminating the need for a separate scaling amplifier and sample-and-hold module.

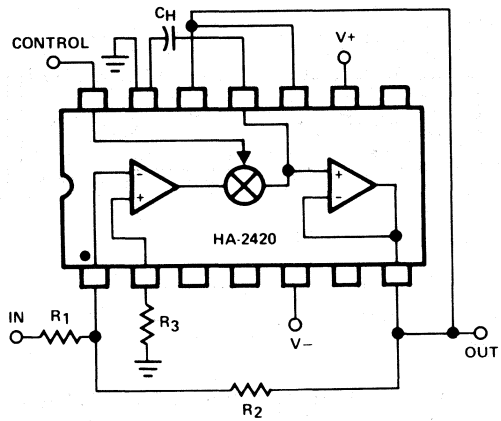
In general, it is usually best design practice to scale the gain such that the largest expected signal will give an output close to + or – 10 volts. Drift current is essentially independent of output level, and less percentage drift will occur in a given time for a larger output signal.

APPLICATION NO. 3

This illustrates another application in which the hookup versatility of the HA-2400 often eliminates the need for a separate operational amplifier and sample-and-hold module. This hookup will have somewhat higher input to output feedthrough during "hold," than the non-inverting connection, since output impedance is the open-loop value during "hold," and feedthrough will be:

$$\frac{Vin\ Ro}{R_1 + R_2 + R_0}$$

Inverting Sample-and-Hold



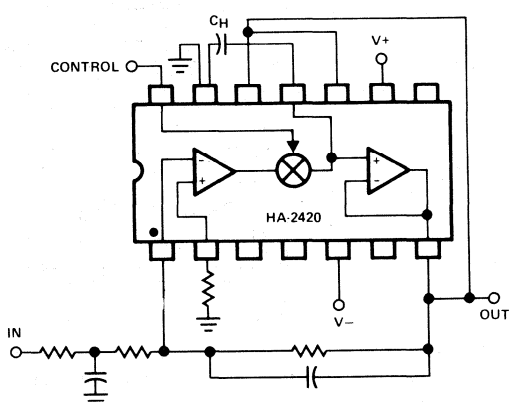
$$GAIN = \frac{R_2}{R_1}$$

$$MAKE \quad R_3 = \frac{R_1 R_2}{R_1 + R_2}$$

APPLICATION NO. 4

It is often required that a signal be filtered prior to sampling. This can be accomplished with only one device. Any of the inverting and non-inverting filters which can be built with op amps can be implemented. However, it is necessary that the sampling switch be closed for sufficient time for the filter to settle when active filter types are connected around the device.

Filtered Sample-and-Hold



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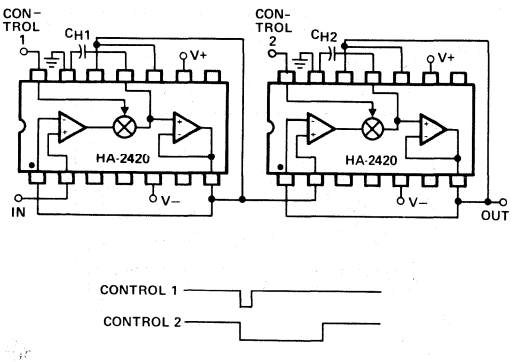
APPLICATION NO. 5

Cascaded Sample-and-Hold

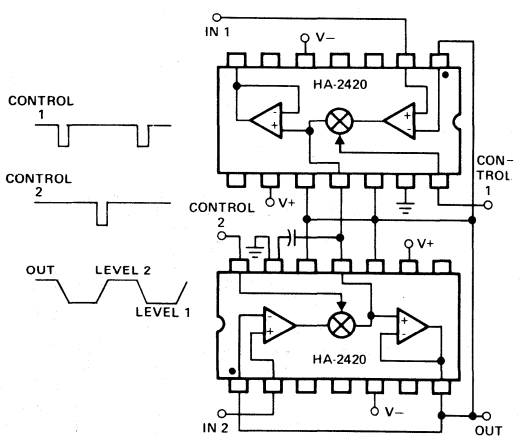


Short sample times require a low value holding capacitor; while long, accurate hold times require a high value holding capacitor. So, achieving a very long hold with a short sample appears to be contradictory. However, it can be accomplished by cascading two S/H circuits, the first with a low value capacitor, the second with a high value. Then the second S/H can sample for as long a time as the first circuit can accurately hold the signal.

APPLICATION NO. 6

Two or more S/H circuits may share a common holding capacitor and output as shown. The only limit to the number of devices to be

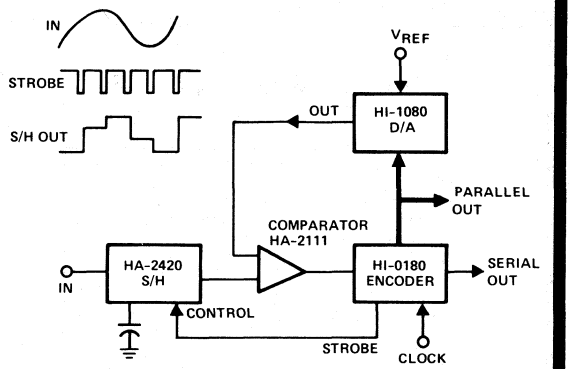
Multiplexed Sample-and-Hold



multiplexed is that the leakage currents of all devices add together, which increases drift during holding.

APPLICATION NO. 7

A/D Converter

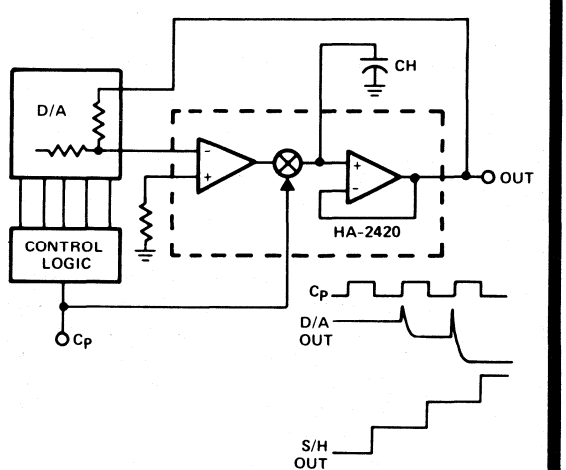


Certain analog to digital converters such as the successive approximation type require that the input signal be a steady D.C. level during the conversion cycle. The HA-2420 is ideal for holding the signal steady during conversion; and also functions as a buffer amplifier for the input signal, adding gain, inversion, etc., if required.

The system illustrated is a complete 8 bit successive approximation converter requiring only four I.C. packages and capable of up to 40,000 conversions per second. Interconnection details are shown on the HI-0180 data sheet.

APPLICATION NO. 8

De-Glitcher



The word "glitch" has been a universal slang expression among electronics people for an unwanted transient condition. In D to A converters, the word has achieved semi-official status for an output transient which momentarily goes in the wrong direction when the digital input address is changed.

In the illustration, the HA-2420 does double duty, serving as a buffer amplifier as well as a glitch remover, delaying the output by ½ clock cycle.

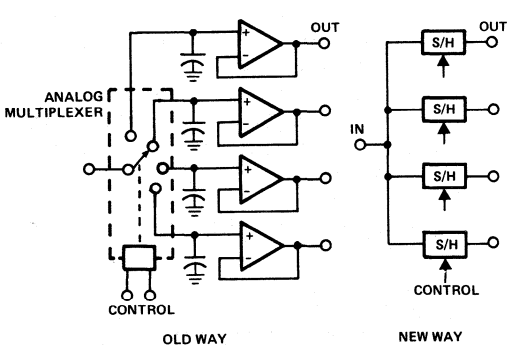
The HA-2420 may be used to remove many other types of "glitches" in a system. If a delayed sample pulse is required, this can be generated using a dual monostable multivibrator I.C.

APPLICATION NO. 9

This circuit reconstructs and separates analog signals which have been time division multiplexed.

The conventional method, shown on the left, has several restrictions, particularly when a short dwell time and a long, accurate hold time is required. The capacitors must charge from a low impedance source through the resistance and current limiting characteristics of the multiplexer. When holding, the high impedance lines are relatively long and subject

De-Multiplexer

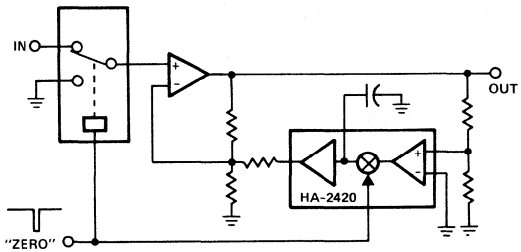


to noise pickup and leakage. When FET input buffer amplifiers are used for low leakage, severe temperature offset errors are often introduced.

Use of the HA-2420 greatly diminishes all of these problems.

APPLICATION NO. 10

Automatic Offset Zeroing



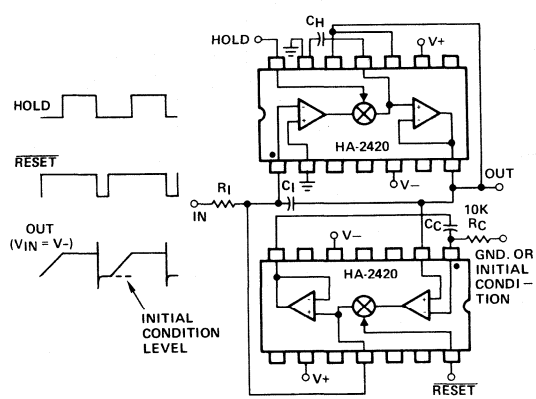
This basic circuit has widespread applications in instrumentation, A/D conversion, DVM's and DPM's to eliminate offset drift errors by periodically rezeroing the system. Basically, the input is periodically grounded, the output offset is then sampled and fed back to cancel the error.

The system illustrated automatically zeros a high gain amplifier. Care in the actual design is necessary to assure that the zeroing loop is dynamically stable. A second sample-and-hold could be added in series with the output to remove the output discontinuity.

Many variations of this scheme are possible to suit the individual system.

APPLICATION NO.11

Integrate-Hold-Reset



This circuit accurately computes the functions,

$$V_o = \int_{T_1}^{T_2} V_{in}\, dt$$

and holds the answer for further processing.

6

Resetting circuits for integrators have always been a practical design problem. The reset circuit must produce an extremely low leakage current across the integrating capacitor, and must produce a very low offset voltage when turned on. The circuit illustrated has excellent results since the leakage at the switch node is exceptionally low. R_C and C_C prevent oscillations during reset and their product should be at least 0.02 times R_I X C_I.

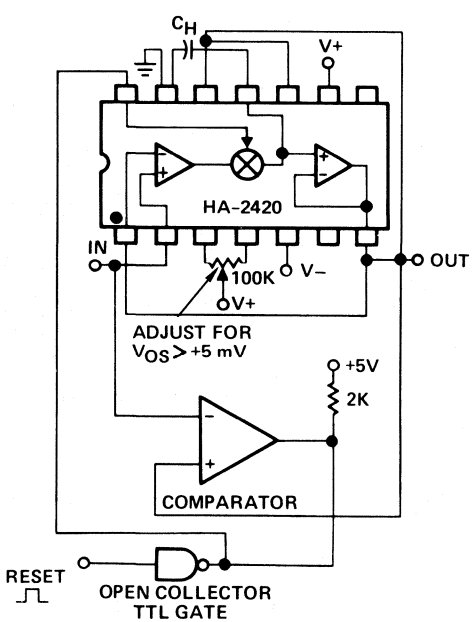
For the simpler integrate and reset function without a hold, substitute an ordinary operational amplifier for the upper device.

APPLICATION NO. 12

This accurate, low drift peak detector circuit combines the basic sample-and-hold connection with a comparator, and will detect 20V p-p signals up to 50kHz.

When the input signal level exceeds the voltage being stored in the S/H, the comparator trips, and a new sample of the input is taken. The S/H offset pot should be adjusted for a slight positive offset, so that the comparator will trip back when the new peak is acquired; otherwise the comparator would remain "on" and the S/H would follow the peak back down.

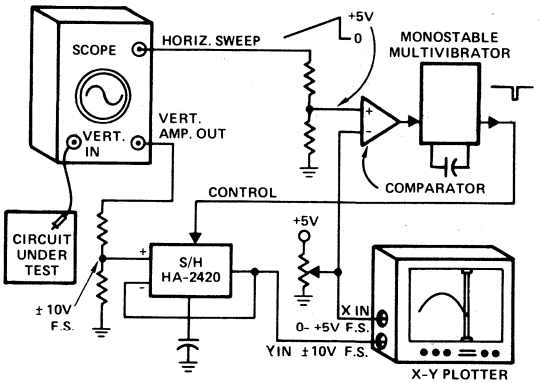
To make a negative peak detector, reverse the comparator inputs, and adjust the S/H for a negative offset.



The reset function, which is difficult to achieve in other peak detector circuits, forces a new sample at the instantaneous input level.

APPLICATION NO. 13

Plot High Speed Waveforms With Sampling Techniques



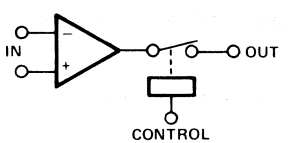
This useful application illustrates how fast repetitive waveforms can be slowed down using sampling techniques. The input signal is much too fast to be tracked directly by the X-Y recorder; but sampling allows the recorder to be driven as slow as necessary.

To operate, the waveform is first synched in on the scope. Then the potentiometer connected to the recorder X input is slowly advanced, and the waveform will be reproduced. The HA-2420 samples for a very short interval once each horizontal sweep of the scope. The sampling instant is determined by the potentiometer at the instant when the horizontal sweep waveform corresponds to the X position of the recorder.

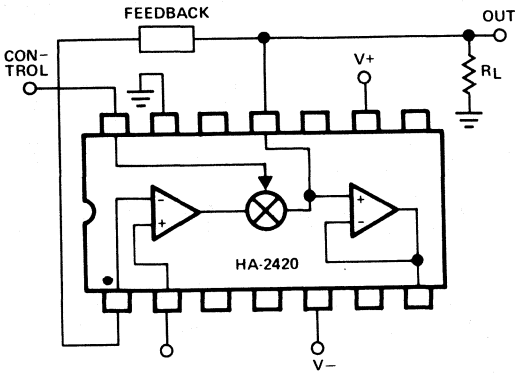
This principle can be applied to many systems for waveform analysis, etc.

APPLICATION NO. 14

Gated Operational Amplifier



EQUIVALENT CIRCUIT



The following are a few of the many applications where an operational amplifier followed by a highly efficient analog switch could be used:

Analog Multiplexer Element
Gated Oscillator
Precision Timing Circuit
Chopper Type Modulator/Demodulator
Crosspoint Switch Element
Reset or Initial Conditions Switch
Gated Comparator
Automatic Calibration Switch
Gated Voltage Regulator

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PRODUCTS DIVISION
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APPLICATION NOTE 518

THE HA-2900 MONOLITHIC CHOPPER STABILIZED AMPLIFIER

BY DON JONES and ROBERT W. WEBB

INTRODUCTION

An operational amplifier should ideally be selected so that, in a given application, performance to the required accuracy is determined only by the external networks. The amplifier should act like a pure, nearly infinite gain block; and not intrude its own personality on the overall circuit performance within the desired accuracy level.

Monolithic integrated circuit operational amplifiers have been quite successful in applications where total input inaccuracies of a few millivolts are acceptable. A new monolithic op amp, the HA-2900, is now available which allows about 100 times improvement in total accuracy.

For about thirty years, the chopper stabilized amplifier has been used when an op amp with the ultimate in DC performance was required. First it was constructed with vacuum tubes and mechanical relay choppers. More recently, it was made with discrete solid state devices in a module or hybrid package. It would be very desirable to achieve the same performance in a monolithic amplifier, with its compactness, higher reliability, and lower cost.

OFFSET VOLTAGE DRIFT

The one parameter which is probably the most troublesome to the monolithic operational amplifier design is offset voltage drift. This is also the most basic parameter for a DC amplifier – with zero volts differential input, the amplifier ought to have zero volts output. Input offset voltage (the small voltage which would be required between the input terminals to make the output actually go to zero volts) can generally be adjusted to a very low value using an external potentiometer or selected fixed resistors. The problem is that this adjustment is good only for the ambient temperature (and instant of time) at which it was made. With a few degrees of change in temperature or after a few months passage of time; the offset voltage may again become significant.

OFFSET CURRENT DRIFT

In many precision op amp specifications, there appears to be a tradeoff between offset voltage drift and offset current drift, each amplifier type being quite good in one category but only average in the other. For precision applications, both drift parameters should be low. For example, a FET input op amp with a quite respectable offset current drift of 10pA/°C, with balanced source resistances of 100K ohms, would have an additional offset voltage drift of 1.0μV/°C created by the offset current drift.

To maintain precision, the maximum practical source resistance will be determined by the offset voltage drift divided by the offset current drift. In the HA-2900, this computes to 130K ohms.

CHOPPER STABILIZATION

Stabilization of offset voltage in an amplifier can be accomplished by adding an auxiliary DC amplifier which may have very limited frequency response but which has very low offset voltage drift. In Figure 1, A1 is the main amplifier, and A2 the auxiliary. If the gain of A2 is large, the effective input offset

voltage of the entire circuit will be nearly that of A2 alone. This is because the input offset voltage of A1 is effectively divided by the gain of A2 in determining its contribution to the offset of the entire circuit. The open loop DC gain of the entire circuit is the product of the gains of A1 and A2.

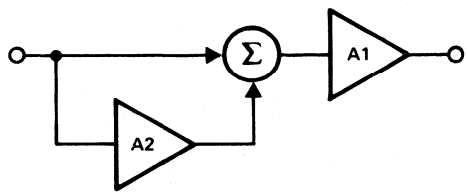


Figure 1

Figure 2 shows a classical chopper amplifier which is often used as an auxiliary DC amplifier. Chopper switch S1 functions as a modulator which changes the incoming DC level to an AC waveform with a proportional amplitude, and phase angle of either 0° or 180° depending on input polarity. The chopped signal is then amplified by an AC coupled amplifier. Ground level of the amplified signal is restored by a second chopper switch, S2, which may be regarded as a synchronous demodulator. Filtering then recreates an amplified replica of the incoming DC or low frequency signal.

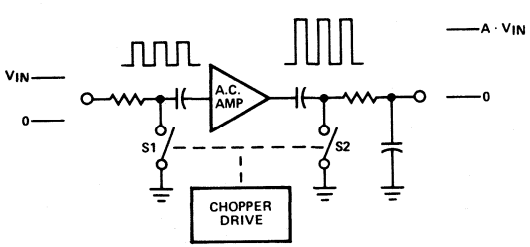


Figure 2

This circuit, properly constructed, will have extremely low offset voltage drift. The amplifier, being AC coupled, does not contribute to the DC offset. The most critical element is S1, since any coupling, DC or AC, of the drive signal to the contacts may introduce an offset error.

A different chopper amplifier concept is illustrated in Figure 3. This is a DC coupled amplifier scheme in which the amplifier periodically disconnects itself from the input signal and adjusts its offset voltage to zero. With S1 and S3 up, the circuit functions as a DC amplifier. When S1, S2, and S3 go down, the amplifier input is grounded and A2 forces the output of A1 to ground. S2, and C1 form a sample-and-hold, so that the correction signal to zero the offset of A1 is stored on C1 after S2 opens. S3, C2, and A3 form a second sample-and-hold, whose function is to store the previous output of A1, while self-zeroing is taking place, thereby removing most of the signal discontinuity.

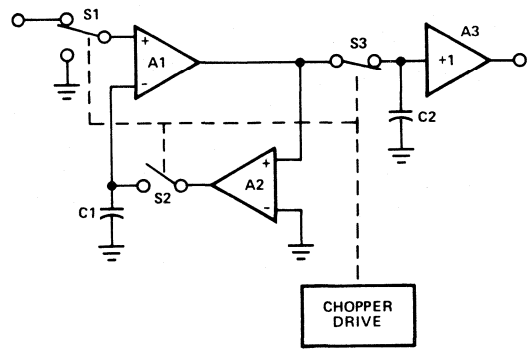


Figure 3

THE HA-2900

In choosing a candidate for monolithic integration, the second scheme (Figure 3) is more attractive, although the block diagram seems more complex. This scheme does not require large value resistors. It requires fewer external capacitors, and these have one end grounded, which allows use of a standard 8 pin can.

There are also performance advantages. The absence of coupling capacitors provides much faster recovery from overdriven conditions – a notorious problem with traditional chopper stabilized amplifiers. The response of the sample-and-hold filter is flat to one half the chopper frequency which greatly reduces settling times. Also, this scheme may be readily modified to provide a stabilized amplifier with full differential inputs; a highly desirable feature.

A diagram of the HA-2900 is shown in Figure 4. A1 is the main amplifier, and A2 is the auxiliary stabilizing amplifier. A3 is the sample-and-hold amplifier in the self-zeroing loop of A2, and A4 is the sample-and-hold amplifier which holds the previous signal during the zeroing interval.

One obvious difference between this diagram and those previously discussed is that the input circuitry is completely symmetrical with respect to the two input lines. This produces a true differential input, in contrast to most stabilized amplifiers which are designed either

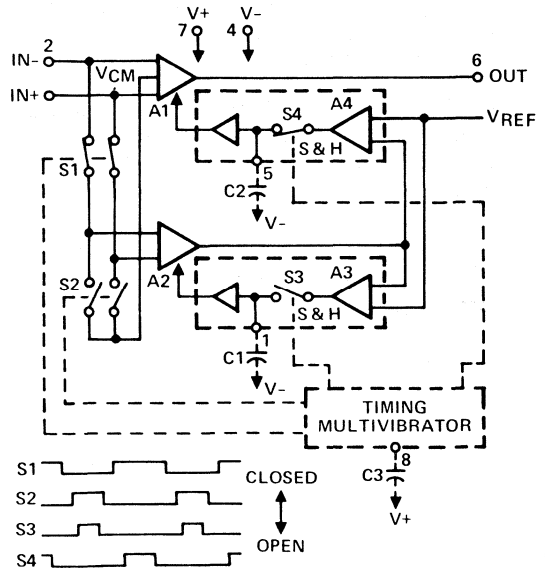


Figure 4

as inverting-only or as non-inverting amplifiers.

During the period in which A2 is stabilizing A1, S1 and S4 are closed while S2 and S3 are open. The DC and low frequency components of the input are amplified by A2 and applied as a correction signal to A1. The effective input offset voltage is nearly that of A2 alone.

To keep the offset voltage of A2 extremely low, it is periodically zeroed. S1 opens and S2 closes, disconnecting A2 from the input terminals and shorting the inputs of A2 together – not at ground level – but to a level equal to the input common mode voltage. This results in an extremely high common mode rejection ratio.

Like most other monolithic op amps, this device does not have a ground terminal; so when S3 closes, the output of A2 is forced to equal an internally generated reference voltage, rather than to ground. Since A4 is referenced to the same voltage, the result is the same. C2 charges to a level which will maintain the offset voltage of A2 at zero. In the meantime, S4 has opened, so that C1 maintains its previous level. The offset of A2 has now been zeroed and A2 then returns to its task of stabilizing A1.

Note that the opening and closing times of S1 through S4 are interleaved. This allows the transient spikes generated when a switch is opened or closed to settle out before other signal paths, which could be affected by these transients, are actuated. The timing multivibrator generates a triangular waveform (Figure 5). Different levels of this triangle are detected by four comparator circuits referenced to different points on a voltage divider to produce the four desired switch driving signals.

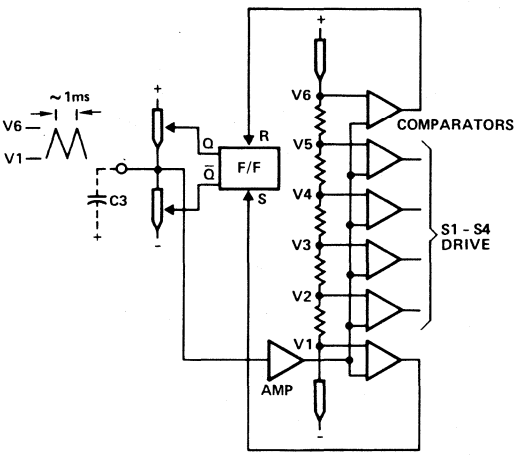
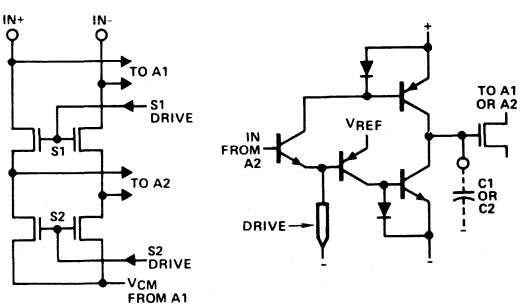


Figure 5

Switches S1 and S2 are each composed of two N-Channel MOSFET's which make excellent no-offset choppers for the low levels and low currents involved. S3 and S4 are complementary bipolar current switches, since appreciable current drive is required and offset voltage is not critical at these points (Figure 6).



A) S1 AND S2

B) SAMPLE-AND-HOLD AMP AND SWITCH (S3 OR S4)

Figure 6

A1 and A2 are each N-Channel MOSFET input amplifiers, which produce the extremely low input currents (Figure 7). Normally, MOSFET's would not be suitable as DC amplifier input stages because of their high offset voltage drift; but chopper stabilization effectively removes that drift; while retaining their high input impedance advantage.

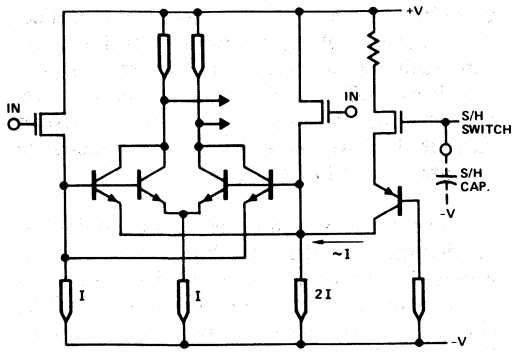


Figure 7

Single ended MOSFET input stages are used in the two sample-and-hold circuits as buffers to sense capacitor voltages. The correction signal from each sample-and-hold circuit alters a current generator which feeds one of the MOSFET sources in the inputs of A1 and A2.

The output stage of A1 is a conventional complementary bipolar follower with short circuit protection.

All of this complex circuitry boils down to the simple functional op amp block shown in Figure 8, packaged with the standard op amp pin-out in the standard TO-99 can. Three external capacitors are required for operation; one for multivibrator timing and two for the sample-and-holds.

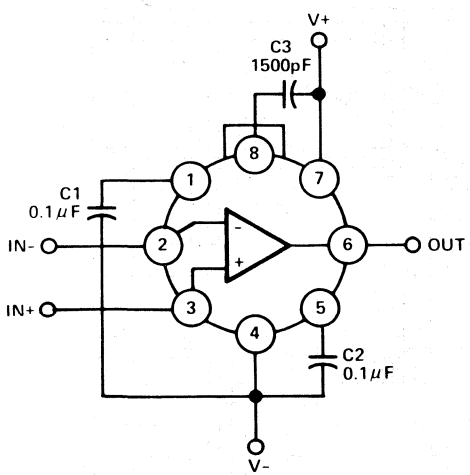


Figure 8

FABRICATION

The HA-2900 is an LSI linear device, containing 252 active elements on a chip measuring .093 X .123 inches.

The chip was designed using the dielectric isolation process, rather than the more conventional junction isolation process, for several reasons. A linear chip can usually be made smaller in dielectric isolation, both because of better packing density and because the high quality active elements can simplify the design – requiring fewer high value resistors and capacitors. The savings in chip area and the consequent higher yields mean that dielectric isolation can be used at little or no cost premium.

The factor which really makes a monolithic chopper stabilized amplifier practical is the high quality NPN, PNP, and FET elements which can be readily fabricated using dielectric isolation. The circuit designer has more freedom in the choice of transistors with desirable parameters, such as high frequency, high gain, vertical PNP transistors; and MOSFET's optimized for chopper service. The superior isolation between elements greatly reduce parasitic capacitance and prevents interaction or latchup due to unwanted four-layer devices. This also allows accurate circuit modeling – essential in a circuit of this complexity.

PERFORMANCE

Significant performance parameters of the HA-2900 are listed in Table 1. In addition to the superior DC parameters, bandwidth and slew rate are also quite respectable. The amplifier is stable, even as a unity gain follower, and exhibits a smooth, fast settling slewing waveform (Figure 9).

OFFSET VOLTAGE DRIFT:	0.2μV/°C
OFFSET CURRENT DRIFT:	1pA/°C
OPEN LOOP GAIN:	5 X 10^8
BANDWIDTH:	3MHz
SLEW RATE:	2.5V/μS
TRUE DIFFERENTIAL INPUTS	

Table I

6

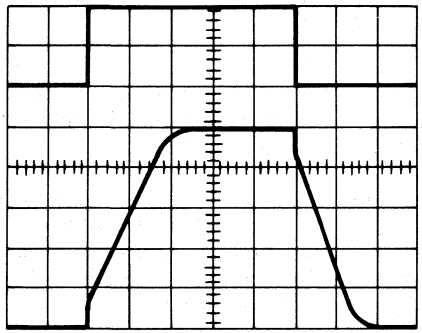


Figure 9

RANDOM NOISE CONSIDERATION

One of the more noticeable characteristics of the HA-2900, particularly when used in high gain circuits, is that the random noise level is 5 to 10 times higher than that seen with conventional bipolar input amplifiers. This is a result of a deliberate design tradeoff — offset current errors vs. noise.

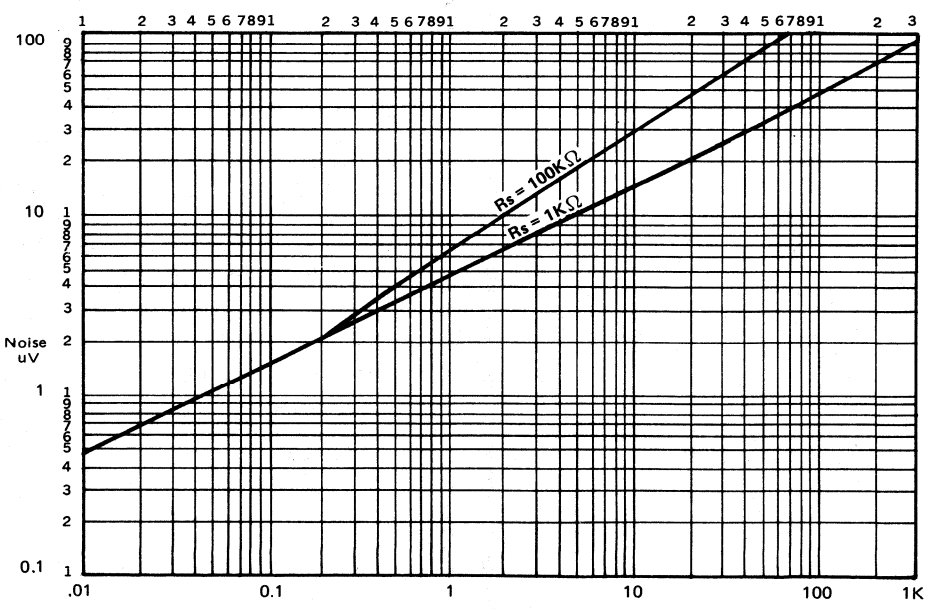
Super gain bipolar input devices or JFET inputs would have lower noise, but have offset current drifts of about 10pA/°C, while the HA-2900 offset current drift is about 1pA/°C. The HA-2900, therefore, may be used with ten times higher input resistors than the other type amplifiers with the same drift errors due to offset current drift. The important applications fact in making this tradeoff is that noise can easily be averaged, allowing recovery of low level D.C. signals at the expense of response time; however, errors due to offset current drift in moderate to high impedance circuits cannot be recovered.

A curve of total equivalent input noise vs. bandwidth for the HA-2900 is shown in Figure 10. As an example of the use of this curve, suppose that we wished to resolve D.C. changes of 10 microvolts with the amplifier illustrated in Figure 11. From the curve, a maximum bandwidth of 0.6 Hz would be required, which could be achieved with C= .0027μF. Response time (10% to 90%) would be about 0.35 ÷ B.W., or about 0.6 seconds.

But suppose we need both fast response and low noise. This can be accomplished by utilizing the best characteristics of two operational amplifiers as illustrated in the applications section.

Synchronous noise generated by the choppers is primarily a common mode current noise, which can be minimized by matching the impedances at the two input terminals. With matched impedances up to 100 K ohms, the synchronous noise seen at the output is well below the random noise level; and the effect of random current noise is not discernable at this impedance level.

HA-2900 EQUIVALENT INPUT NOISE (peak-to-peak) AS A FUNCTION OF CLOSED LOOP BANDWIDTH



WHO NEEDS IT?

There are many applications, such as in precise analog computation and in precision DC instrumentation where the low drift of a chopper stabilized amplifier is obviously required.

There are many other applications where the need for this amplifier vs. the more conventional op amps is less obvious. The designer should ask himself these questions:

1. Are there assemblies which require a technician to adjust a pot or select resistors to zero an amplifier? What are the cost and reliability advantages in using an amplifier which requires no circuit adjustments? Trimmer pots are many times less reliable than a monolithic I.C.

2. Does the system require occasional recalibration because of amplifier drift with time? The chopper stabilized amplifier is actually a closed loop system — offset voltage is continuously monitored and adjusted to near zero.

3. Do assemblies ever have to be reworked because of excessive amplifier drift with temperature? In many amplifiers the drift specification may no longer be valid after zeroing. In many low drift amplifiers, the guaranteed drift specifications are not 100% measured by the manufacturer, so the burden of proof is left to the user.

4. Is the total system performance marginal because of the accumulation of errors? Would the error budget situation improve with the substitution of much more accurate op amps?

5. Is a complex analog-digital system under consideration, simply because of accuracy and drift problems associated with a simpler all analog system?

The decision on whether or not to use a chopper stabilized amplifier in these cases will depend on the analysis of the cost and performance tradeoffs in the individual situation. In any case, the knowledge that a solution is now available, should any of these problems arise, will remove some of the greatest worries of the linear systems designer.

APPLICATIONS

The HA-2900 may be used in virtually any of the hundreds of published operational amplifier applications.

Some care is required in the physical layout of the system to realize the full accuracy potential of an ultra-low drift amplifier. When mounted in a typical breadboard or P.C. card adequate for an ordinary op amp application, drifts on the order of 1μV/°C may be expected. If this is good enough, the designer need go no further. But to reach the ultimate device performance, the designer must take into account external effects. These include thermocouple and electrochemical EMF's generated at junctions of dissimilar metals (solder joints, connectors, internal junctions in resistors and capacitors), leakage across insulating materials, static charges created by moving air, and improper grounding and shielding practices. The main layout procedure is to insure that the networks going to the two amplifier inputs are identical and are at the same temperature.

Figure 11 shows a typical high gain amplifier application. Gain is 1,000; bandwidth is about 2 KHZ. Either input terminal may be grounded for inverting or non-inverting operation or the inputs may be driven differentially. The symmetrical networks at the device inputs are recommended for any of the three operating modes to eliminate chopper noise and yield the best drift characteristics. Total input noise, with C=0, is about 30μVRMS. This noise can be reduced, at the expense of bandwidth by adding capacitors as shown.

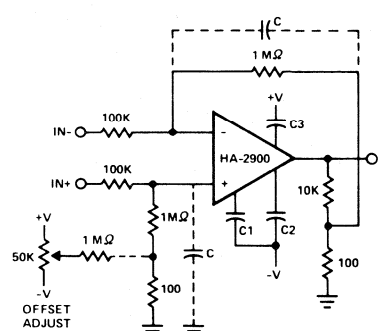


Figure 11

6

A high impedance differential instrumentation amplifier is shown in Figure 12. This well known configuration has excellent common mode rejection of ±10 volts common mode input signals. Protection diodes are included to prevent the device input terminals from exceeding either power supply.

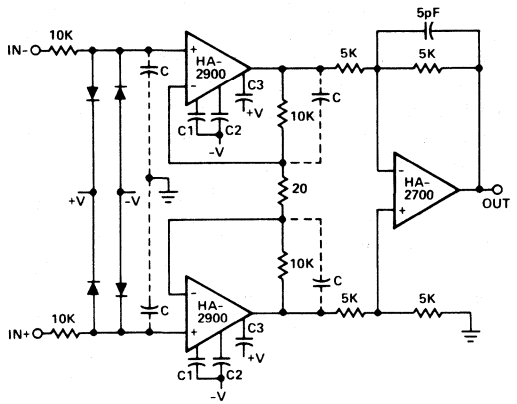


Figure 12

Integrators have been around as long as op amps, and are used in analog computation, active filters, timers, waveform generators, control systems, and A/D converters. An op amp for a precision integrator should have high gain, low offset voltage, low bias current, and wide bandwidth. So it is evident that the HA-2900 should make the best possible integrator (Figure 13). The gain of the HA-2900 allows accurate integration over eight decades of frequency. Dual slope A/D converters can now easily be made with six digit resolution.

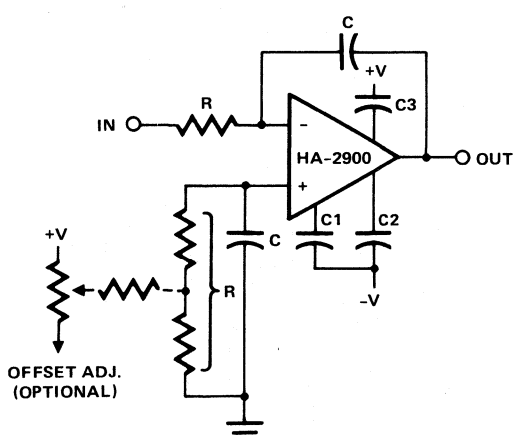


Figure 13

The composite amplifier combines the best performance of two different amplifier types. The exceptionally low drift characteristics of the HA-2900 may be added to another amplifier with wide bandwidth and high slew rate or low noise.

Figure 14 illustrates an excellent combination of characteristics for use wherever inverting amplifier applications are required. Features of the composite amplifier include: slew rate: 300V/μs, gain bandwidth product: 10-500 MHz, D.C. gain: 10^{13}, offset voltage drift: 0.3uV/°C, bias current drift: 50pA/°C, input noise (0-1 KHz): 5uV peak to peak.

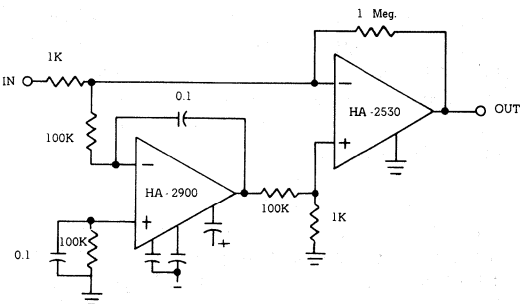


Figure 14

In most composite amplifiers, to avoid excessively long settling times or instabilities, it is preferable to match the 0 db response of the integrator to the open loop low frequency pole of the main amplifier. However, if the main amplifier has all of the characteristics, except for offset voltage drift, necessary to resolve the lowest required input change; it will be possible to operate the integrator at a much lower bandwidth, greatly reducing its noise contribution. The main amplifier must have very high gain, low bias current, low noise, and very small changes in offset voltage with output voltage changes. Then the integrator needs to remove only the essentially D.C. offset voltage of the main amplifier.

Figure 15 illustrates a hookup for non-inverting amplifier applications, which is useful from gains of unity up to several thousand. Gain – bandwidth product is 100 MHz. If the composite amplifier closed loop bandwidth exceeds the unity gain bandwidth of the HA-2900 (2.5MHz), then R and C should be added to suppress response peaks and pulse overshoot. Low frequency flicker noise is about 10μV peak to peak, caused chiefly by the HA-2620.

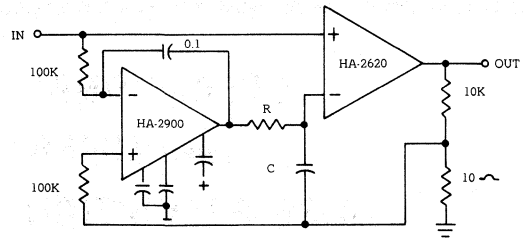


Figure 15

The circuit shown in Figure 16 where the integrator drives one of the offset adjust terminals of the main amplifier may be adapted to many amplifier types. This hookup has the advantages that the composite amplifier retains differential inputs, and may be used in any normal operational amplifier feedback configuration.

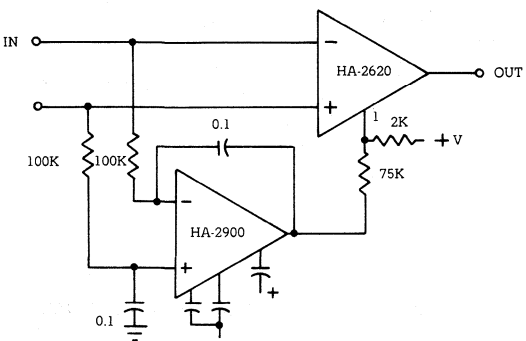


Figure 16

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

APPLICATION NOTE 519

OPERATIONAL AMPLIFIER NOISE PREDICTION

BY RICHARD WHITEHEAD

INTRODUCTION

When working with op amp circuits an engineer is frequently required to predict the total RMS output noise in a given bandwidth for a certain feedback configuration. While op amp noise can be expressed in a number of ways, "spot noise" (RMS input voltage noise or current noise which would pass through 1Hz wide bandpass filters centered at various discrete frequencies), affords a universal method of predicting output noise in any op amp configuration.

THE NOISE MODEL

Figure 1 is a typical noise model depicting the noise voltage and noise current sources that are added together in the form of root mean square to give the total equivalent input voltage noise (RMS), therefore:

$$E_{ni} = \sqrt{e_{ni}^2 + I_{ni}^2 R_g^2 + 4KTR_g}$$ where,

E_{ni} is the total equivalent input voltage noise of the circuit.

e_{ni} is the equivalent input voltage noise of the amplifier.

$I_{ni}^2 R_g^2$ is the voltage noise generated by the current noise.

$4KTR_g$ expresses the thermal noise generated by the external resistors in the circuit where $K = 1.23 \times 10^{-23}$ joules/^oK; $T = 300^oK$ (27^oC) and $R_g = \left(\frac{R_1 R_3}{R_1 + R_3}\right) + R^2$

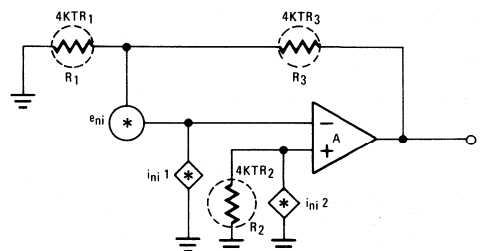


Figure 1

The total RMS output noise (E_{no}) of an amplifier stage with gain = G in the bandwidth between f_1 and f_2 is:

$$E_{no} = G\left(\int_{f1}^{f2} E_{ni}^2 df^{1/2}\right)$$

Note that in the amplifier stage shown, G is the non-inverting gain $\left(G = 1 + \frac{R2}{R1}\right)$ regardless of which input is normally driven.

PROCEDURE FOR COMPUTING

1. Refer to the voltage noise curves for the amplifier to be used. If the R_g value in the application is close to the R_g value in one of the curves, skip directly to step 6, using that curve for values of E_{ni}^2. If not, go to step 2.
2. Enter values of e_{ni}^2 in line (a) of the table below from the curve labeled "$R_g = 0\,\Omega$".
3. From the current noise curves for the

amplifier, obtain the values of i_{ni}^2 for each of the frequencies in the table, and multiply each by R_g^2, entering the products in line (b) of the table.

4. Obtain the value of $4KTR_g$ from Figure 14, and enter it on line (c) of the table. This is constant for all frequencies. The $4KTR_g$ value must be adjusted for temperatures other than normal room temperature.

5. Total each column in the table on line (d). This total is E_{ni}^2.

	10Hz	100Hz	1KHz	10KHz	100KHz
(a) e_{ni}^2					
(b) $I_{ni}^2R_g^2$					
(c) $4KTR_g$					
(d) E_{ni}^2					

6. On linear scale graph paper enter each of the values for E_{ni}^2 vs. frequency. In most cases, sufficient accuracy can be obtained simply by joining the points on the graph with straight line segments.

7. For the bandwidth of interest, calculate the area under the curve by adding the areas of trapezoidal segments. This procedure assumes a perfectly square bandpass condition; to allow for the more normal -6db/octave bandpass skirts, multiply the upper (-3db) frequency by 1.57 to obtain the effective bandwidth of the circuit, before computing the area. The total area obtained is equivalent to the square of the total input noise over the given bandwidth.

8. Take the square root of the area found above and multiply by the gain (G) of the circuit to find the total Output RMS noise.

A TYPICAL EXAMPLE

It is necessary to find the output noise of the circuit shown below between 1KHz and 24KHz.

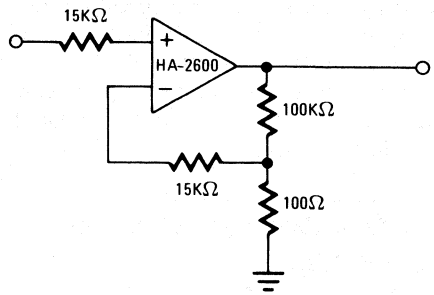
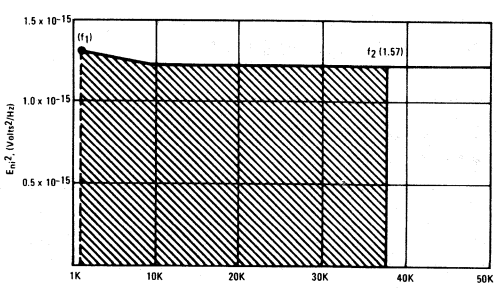


Figure 2
The HA-2600 In a Typical G = 1000 Circuit

Values are selected from Figures 5, 5a and 14 to fill in the table as shown below. An R_g of 30KΩ was selected.

	10Hz	100Hz	1KHz	10KHz	100KHz
(a) e_{ni}^2	3.6×10^{-15}	1.156×10^{-15}	7.84×10^{-16}	7.29×10^{-16}	7.29×10^{-16}
(b) $I_{ni}^2R_g^2$	9.9×10^{-16}	1.89×10^{-16}	3.15×10^{-17}	7.2×10^{-18}	7.2×10^{-18}
(c) $4KTR_g$	4.968×10^{-16}	4.968×10^{-16}	4.968×10^{-16}	4.968×10^{-16}	4.968×10^{-16}
(d) E_{ni}^2	5.09×10^{-15}	1.86×10^{-15}	1.31×10^{-15}	1.23×10^{-15}	1.23×10^{-15}

The totals of the selected values for each frequency is in the form of E_{ni}^2. This should be plotted on linear graph paper as shown below:



HA-2600 Total Equivalent Input Noise Squared

Since a noise figure is needed for the frequency of 1KHz to 24KHz, it is necessary to calculate the effective bandwidth of the circuit. With AV = 60db the upper 3db point is approximately 24KHz. The product of 1.57 (24KHz) is 37.7KHz and is the effective bandwidth of the circuit.

The shaded area under the curve is approximately 45 x 10^{-12} $Volts^2$; the total equivalent input noise is $\sqrt{E_{ni}^2}$ or 6.7 microvolts, and the total output noise for the selected bandwidth is $\sqrt{E_{ni}^2}$ x (closed loop gain) or 6.7 millivolts RMS.

ACTUAL MEASUREMENTS FOR COMPARISON

The circuit shown below was used to actually measure the broadband noise of the HA-2600 for the selected bandwidth:

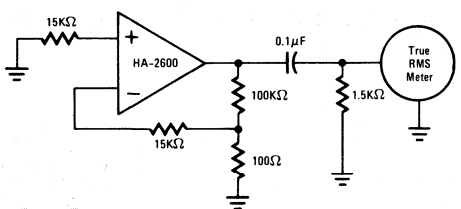


Figure 3
A Typical Test Circuit for Broadband Noise Measurements

The frequencies below the f_1 point of the bandwidth selected are filtered out by the RC network on the output of HA-2600. The measurement of the broadband noise is observed on the true RMS voltmeter. The measured output noise of the circuit is 4.7 millivolts RMS as compared to the calculated value of 6.7 microvolts RMS.

ACQUIRING THE DATA FOR CALCULATIONS

Spot noise values must be generated in order to make the output noise prediction. The effects of "Popcorn" noise have been excluded due to the type of measurement system.

The Quan-Tech Control Unit, model no. 2283 and Filter Unit, model no. 2181 were used to acquire spot noise voltage values expressed in ($V\sqrt{Hz}$). The test system performs measurements from 10Hz by orders of magnitude to 100KHz with an effective bandwidth of 1Hz at each tested frequency.

Several source resistance (R_g) values were used in the measuring system to reveal the effects of R_g on each type of Harris' op amps and to obtain proper voltage noise values essential for current noise calculations.

A DISCUSSION ON "POPCORN" NOISE

"Popcorn" noise was first discovered in early 709 type op amps. Essentially it is an abrupt step-like shift in offset voltage (or current) lasting for several milliseconds and having amplitude from less than one microvolt to several hundred microvolts. Occurance of the "pops" is quite random — an amplifier may exhibit several "pops" per second during one observation period and then remain "popless" for several minutes. Worst case conditions are usually at low temperatures with high values of R_g. Some amplifier designs and some manufacturer's products are notoriously bad in this respect. Although theories of the popcorn mechanism differ, it is known that devices with surface contamination of the semiconductor chip will be particularly bad "poppers". Advertising claims notwithstanding, the authors have never seen any manufacturer's op amp that was completely free of "popcorn". Some peak detector circuits have been developed to screen devices for low amplitude "pops", but 100% assurance is impossible because an infinite test time would be required. Some studies have shown that spot noise measurements at 10Hz and 100Hz, discarding units that are much higher than typical, is an effective screen for potentially high "popcorn" units.

The vast majority of Harris op amps will exhibit less than 3 μV peak-to-peak "popcorn". Screening can be performed, but it should be noted that the confidence level of the screen could be as low as 60%.

REFERENCES

Fitchen, F.C. and Motchenbacker, C.D. Low Noise Electronic Design. New York: John Wiley and Sons, 1973.

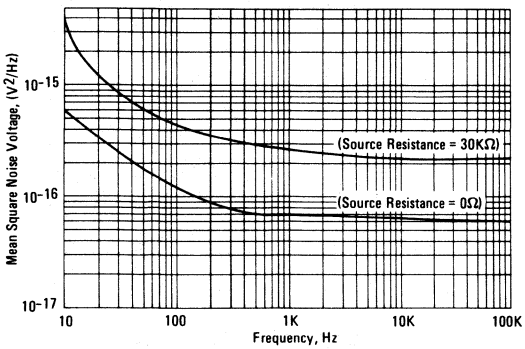
Instruction Manual, Model 2173C Transistor Noise Analyzer Control Unit. Quan-Tech, Division of KMS Industries. Whippany, New Jersey.

TYPICAL SPOT NOISE CURVES

Unless Otherwise Noted:
$V_S = \pm 15V$ $T_A = +25^oC$

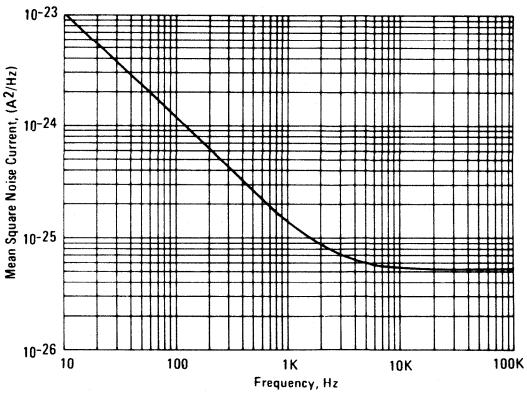
Curve 1

HA-909/911 INPUT NOISE VOLTAGE



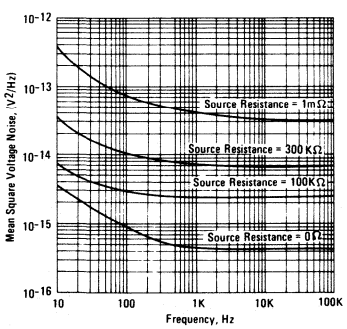
Curve 1A

HA-909/911 INPUT NOISE CURRENT



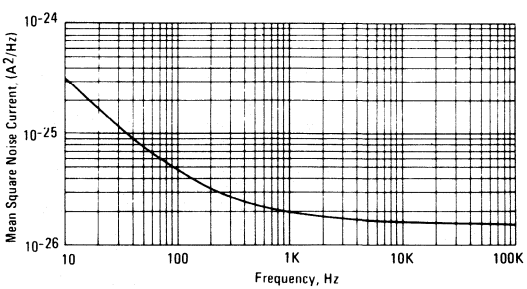
Curve 2

HA-2400 INPUT NOISE VOLTAGE



Curve 2A

HA-2400 INPUT NOISE CURRENT



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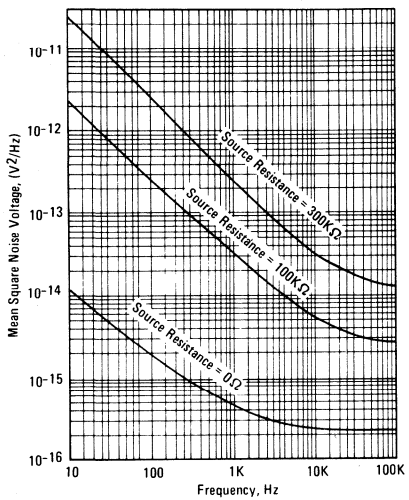
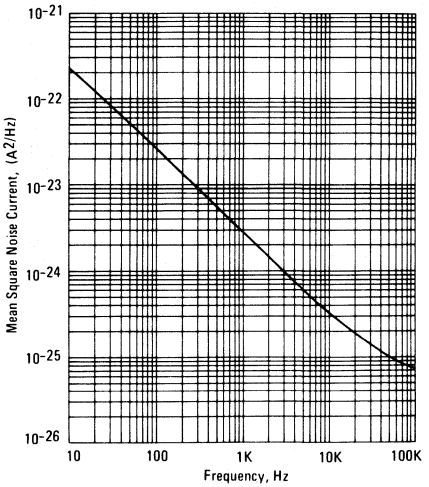
Curve 3

HA-2500/2510/2520 INPUT NOISE VOLTAGE



Curve 3A

HA-2500/2510/2520 INPUT NOISE CURRENT



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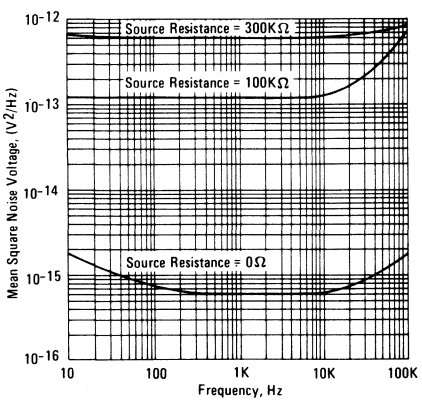
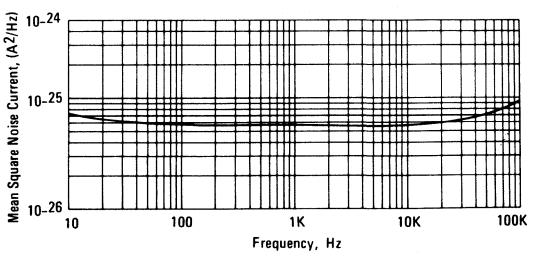
Curve 4

HA-2530/2535 NOISE VOLTAGE



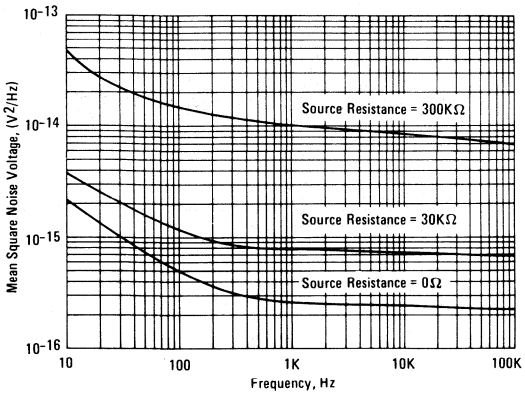
Curve 4A

HA-2530/2535 NOISE CURRENT



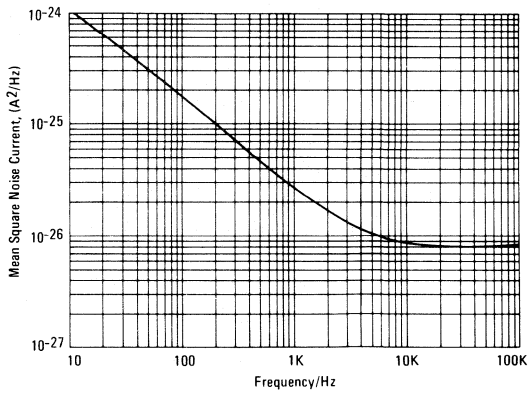
Curve 5

HA-2600/2620 INPUT NOISE VOLTAGE



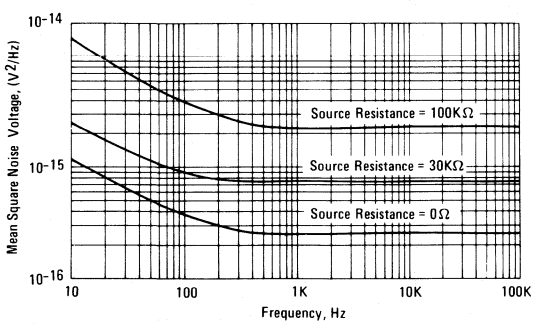
Curve 5A

HA-2600/2620 INPUT NOISE CURRENT



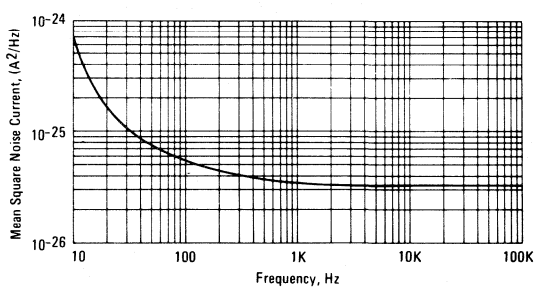
Curve 6

HA-2640/2645 INPUT VOLTAGE NOISE ($V_S = \pm 30V$)



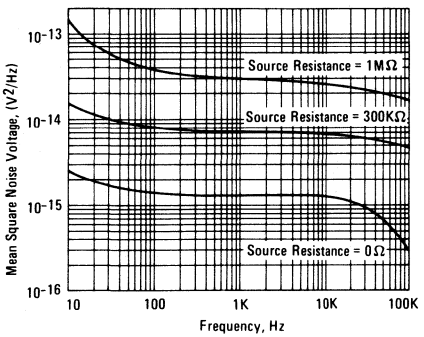
Curve 6A

HA-2640/45 INPUT NOISE CURRENT ($V_S = \pm 30V$)



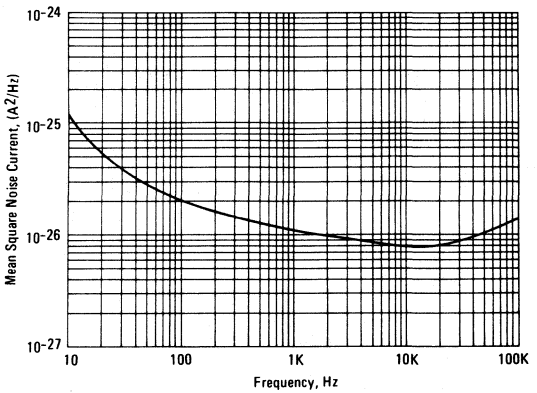
Curve 7

HA-2700 INPUT NOISE VOLTAGE



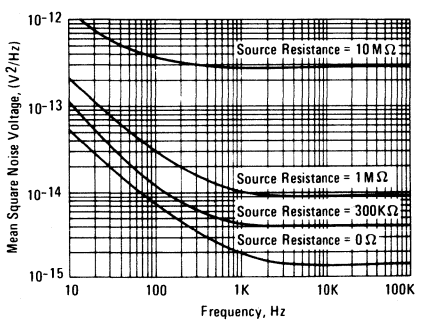
Curve 7A

HA-2700 INPUT NOISE CURRENT



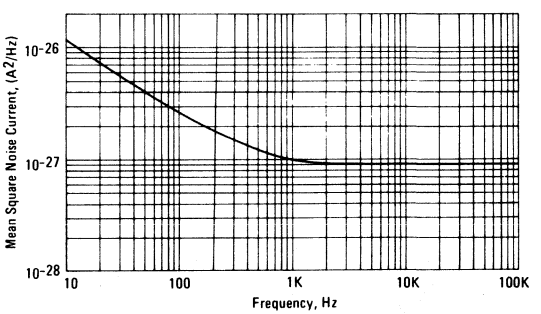
Curve 8

HA-2720/2730 INPUT NOISE VOLTAGE (I_{SET} = 1μA)



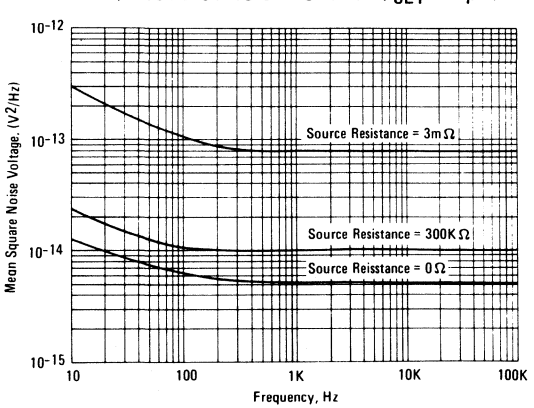
Curve 8A

HA-2720/2730 INPUT NOISE CURRENT (I_{SET} = 1μA)



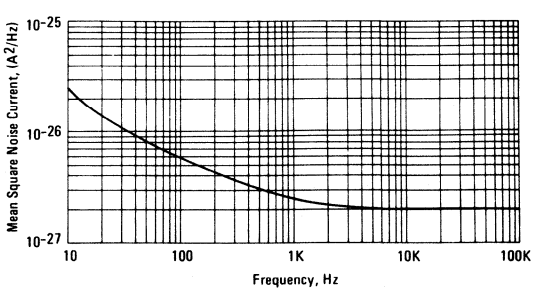
Curve 9

HA-2720/2730 INPUT NOISE VOLTAGE (I_{SET} = 10μA)



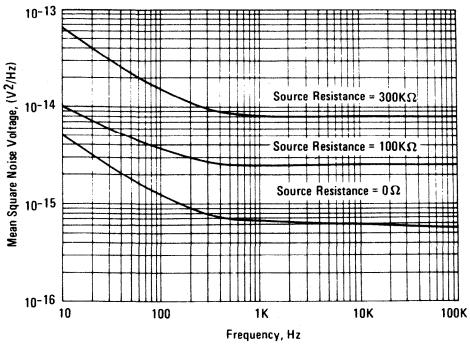
Curve 9A

HA-2720/2730 INPUT NOISE CURRENT (I_{SET} = 10μA)



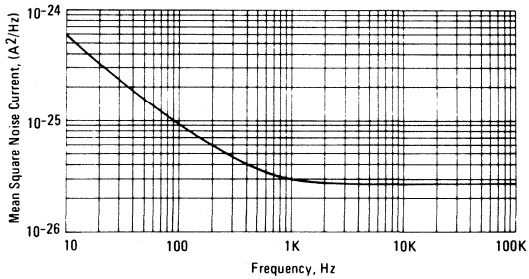
Curve 10

HA-2720/2730 INPUT NOISE VOLTAGE (I_{SET} = 100μA)



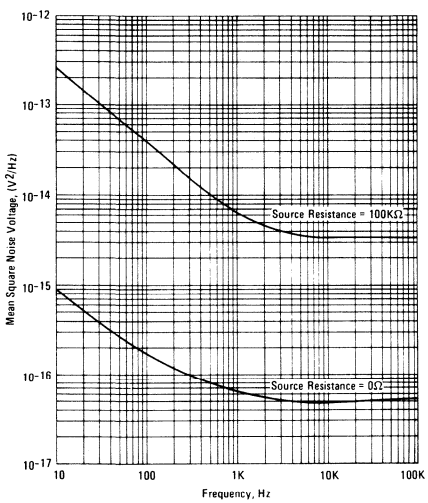
Curve 10A

HA-2720/2730 INPUT NOISE CURRENT (I_{SET} = 100μA)



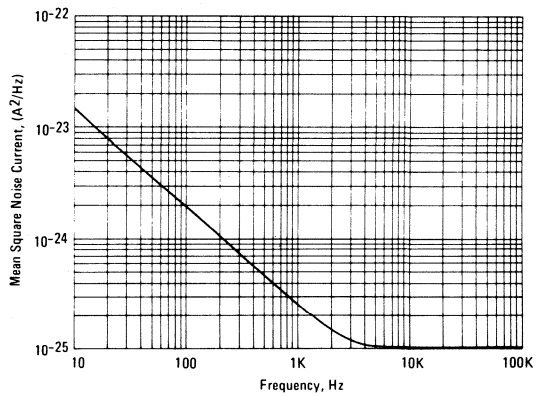
Curve 11

HA-4602/4605 INPUT NOISE VOLTAGE



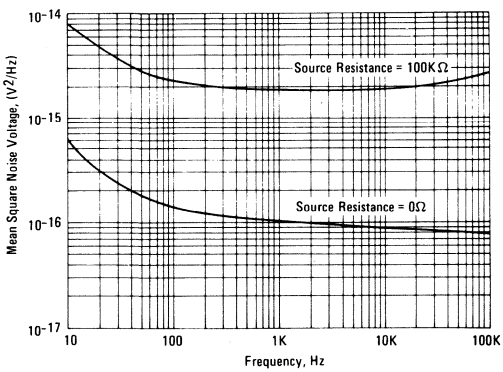
Curve 11A

HA-4602/4605 INPUT NOISE CURRENT



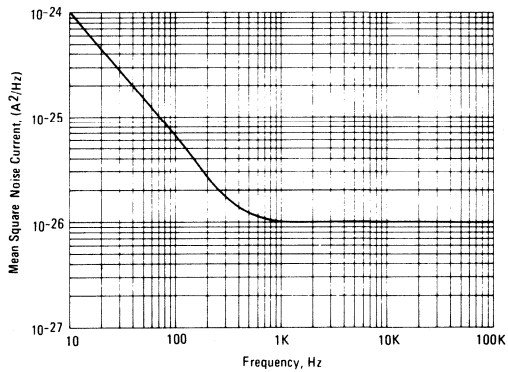
Curve 12

HA-4741 INPUT NOISE VOLTAGE

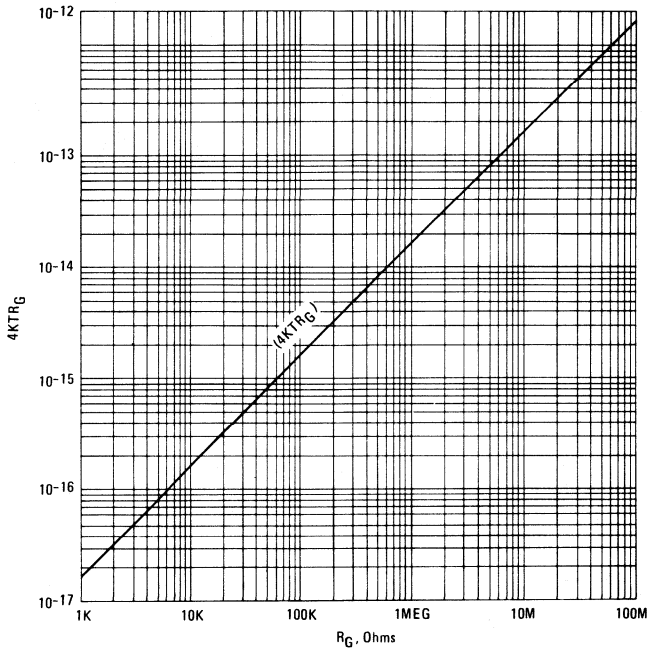


Curve 12A

HA-4741 INPUT NOISE CURRENT



Curve 13


10-12
10-13
10-14
10-15
10-16
10-17
4KTRG
(4KTRG)
1K
10K
100K
1MEG
10M
100M
RG, Ohms

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

APPLICATION NOTE 520

CMOS ANALOG MULTIPLEXERS AND SWITCHES; APPLICATIONS CONSIDERATIONS

BY DON JONES

INTRODUCTION

This paper is a mixed collection of answers to questions most frequently asked about CMOS analog multiplexers and switches. It covers selection criteria, parameter definitions, handling and design precautions, typical applications, and special topics such as transient considerations and R.F. switching. Some other devices which perform analog switching functions in particular applications are also discussed.

As a complement to this paper, the article, "Getting the Most Out of CMOS Devices for Analog Switching Jobs" by Ernie Thibodeaux, Electronics, December 25, 1975 is recommended reading for any analog CMOS user (reprinted in Application Note 521). This discusses the different CMOS processes used by various manufacturers, showing the performance trade-offs and particularly the different failure modes which may be encountered.

CHOOSING THE RIGHT DEVICE

A. MULTIPLEXERS: PROTECTED OR UNPROTECTED?

Harris overvoltage protected multiplexers, HI-506A/507A/508A/509A are designed for failure-proof operation in a common class of applications: any system in which the analog input signal lines originate external to the equipment. This includes most data acquisition, telemetry, and process control systems. Overvoltage protection is necessary because the signal lines are commonly subject to a number of potentially destructive situations.

1. Analog signals may be present while the MUX power supplies are off.
2. The signal lines may receive induced voltage spikes from nearby sources.
3. Static electricity may be introduced on the signal lines by personnel or equipment.
4. Grounding problems are frequent; A.C. power line voltages at high impedance can appear on the signal lines. Signal lines can be accidentally shorted to other voltage sources.

Harris protected type multiplexers will withstand a continuous voltage on any one input of ±20 Volts greater than either supply (this limitation is due only to temperature rise considerations at maximum ambient) and have withstood simulated static discharge conditions of greater than 1000 Volts.

It should be emphasized that only the HI-506A through 509A (and exact equivalents from authorized alternate suppliers) will have this kind of protection necessary for inputs from the outside world. Certain CMOS process improvements, such as "floating body" and "buried layer" do help minimize one failure mode (latchup) but will still fail under excess voltage or current conditions prevalent in this type application.

Conventional CMOS multiplexers can be protected against overvoltage destruction by external resistor-diode networks to limit input current to a safe level, but it is difficult to prevent another phenomenon with overvoltage; normally-off switching elements will tend to switch on, due to parasitic bipolar transistors in the CMOS structure, so the overvoltage spike will appear at the multiplexer output. The Harris internal protection circuits eliminate the problem by automatically shutting off the parasitic transistor during overvoltage conditions.

A simplified equivalent circuit of the Harris internal protection network is shown in Figure 1.

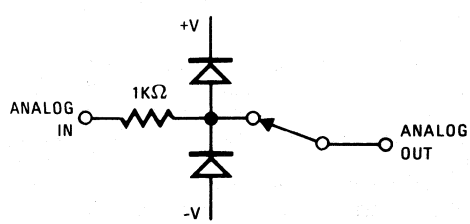


Figure 1

This will help answer the question of what happens when the supplies are turned off, but input signals are present. If the supplies are shorted to ground, then the inputs will have about 1KΩ impedance to ground. If the supplies are open circuit, then the most positive and most negative inputs will act as supplies to the multiplexer.

In normal operating parameters, internally protected multiplexers have one difference from the unprotected versions—ON resistance is necessarily higher because of the added series current limiting resistor. However, to achieve the same degree of protection with conventional devices, the same resistance must be added externally, plus external diodes which would add to the effective leakage currents.

Conventional unprotected multiplexers are suitable for systems where the MUX inputs come from sources within the equipment, such as from op amps powered by the same ±15 Volt supplies. The HI-506/507/1818A/1828A are intended for this type system. They are entirely free of any latch-up tendency, which have plagued some other types, even in these more benign applications. They are also free of the performance compromises which have accompanied some attempts to cure the latch-up problem.

B. WHICH SWITCH TO SWITCH TO?

Harris furnishes a complete line of CMOS analog switches, including replacements for most of the available CMOS and JFET switches. All types feature rugged no-latch-up construction, uniform characteristics over the analog signal range, and excellent high frequency characteristics.

The HI-200 and HI-201 replace the popular, low cost DG200 and DG201 types dual and quad switches.

The HI-1800A is a low leakage dual DPST switch with a versatile addressing scheme, allowing use of a single type for many different switching functions.

The HI-5040 through HI-5051 are low resistance types, offering one to four switches in virtually all combinations. These replace the IH-5040 series with significantly better performance, and with both 75 ohm and 30 ohm switches available in all configurations. These are also plug-in replacements for many of the DG180 and DG190 series of FET hybrid switches, offering the advantage of monolithic construction, but with slightly longer switching times.

The analog switches do not contain overvoltage protection on the analog inputs, although they will withstand inputs 2 or 4 Volts greater than the supplies. External current limiting should be provided if higher overvoltages are anticipated, such as a resistor in series with the analog input of value: R(ohms) $\geq$ (V_{IN} -V_{SUPPLY}) x 50 where V_{IN} is the maximum expected input voltage. All digital inputs do have overvoltage/static charge protection.

DATA SHEET DEFINITIONS

A. ABSOLUTE MAXIMUM RATINGS

As with all semiconductors, these are maximum conditions which may be applied to a device (one at a time) without resulting in permanent damage. The device may, or may not, operate satisfactorily under these conditions—conditions listed under "Electrical Characteristics" are the only ones guaranteed for satisfactory operation.

B. V_S, ANALOG SIGNAL RANGE

The input analog signal range over which reasonably accurate switching will take place. For supply voltages lower than nominal, V_S will be equal to the voltage span between the supplies. Note that other parameters such as R_{ON} and leakage currents are guaranteed over a smaller input range, and would tend to degrade towards the V_S limits. All Harris devices can withstand $+V_S$ applied at an input while $-V_S$ is applied to the output (or vice-versa) without switch breakdown—this is not true for some other manufacturers' devices.

C. R_{ON}, ON RESISTANCE

The effective series on-switch resistance measured from input to output under specified conditions. Note that R_{ON} changes with temperature (highest at high temp.) and to a lesser degree with signal voltage and current.

D. $I_S(OFF)$, $I_D(OFF)$, $I_D(ON)$: LEAKAGE CURRENTS

Currents measured under conditions illustrated on data sheet. Harris prefers to guarantee only worst-case high temperature leakages, because room temperature picoampere levels are virtually impossible to measure repeatably on available automated test equipment. Even under laboratory conditions, fixture and test equipment stray leakages may frequently exceed the device leakage. Leakages tend to double every 10°C temperature rise, so it is reasonable to assume that the +25°C figure is about .001 times the +125°C measurement; however, in some cases there may be ohmic leakages, such as on the package surface, which would make the +25°C reading higher than calculated.

Each of these leakage figures is the algebraic sum of all currents at the point being measured: to each power supply, to ground, and through the switches; so the current direction cannot be predicted. In making an error analysis it should be assumed that all leakages are in the worst-case direction.

In most systems, $I_D(ON)$ has the most effect, creating a voltage offset across the closed switch equal to $I_D(ON) \times R_{ON}$.

E. V_{AL}, V_{AH}; INPUT THRESHOLDS

The lower and upper limits for the digital address input voltage at which the switching action takes place. All other parameters will be valid if all "0" address inputs are less than V_{AL} and all "1" inputs are greater than V_{AH}. Logic compatibility will be discussed in detail later in this paper.

F. I_A, INPUT LEAKAGE CURRENT

Current at a digital input, which may be in either direction. Digital inputs on Harris devices are similar to CMOS logic inputs; connection to MOS gates through resistor-diode protection networks. Unlike some other devices, there is no DC negative resistance region which could create an oscillating condition.

G. T_A, T_{ON}, T_{OFF}; ACCESS TIME

The logic delay time plus output rise time to the 90% point of a full scale analog output swing. After this time the output will continue to rise, approaching the 100% point on an exponential curve determined by $R_{ON} \times C_D(OFF)$.

H. T_{OPEN}, BREAK-BEFORE-MAKE DELAY

The time delay between one switch turning OFF and another switch turning ON; both switches being commanded simultaneously. This prevents a momentary condition of both switches being ON, generally a very minor problem.

I. $C_S(OFF)$, $C_D(OFF$, $C_D(ON)$ INPUT/OUTPUT CAPACITANCE

Capacitance with respect to ground measured at the analog input/output terminals. $C_D(ON)$ is generally the sum of $C_S(OFF)$ and $C_D(OFF)$. $C_D(OFF)$ is usually the most important term as rise time/settling characteristics are determined by $R_{ON} \times C_D(OFF)$, as well as the high frequency transmission characteristics.

J. $C_{DS}(OFF)$, DRAIN TO SOURCE CAPACITANCE

The equivalent capacitance shunting an open switch.

K. OFF ISOLATION

The proportion of a high frequency signal applied to an open switch input appearing at the output: off isolation = 20 log $\frac{V_{IN}}{V_{OUT}}$. This feedthrough is transmitted through $C_{DS}(OFF)$ to a load composed of $C_D(OFF)$ in parallel with the external load. The isolation generally decreases by 6dB/octave with increasing frequency.

L. C_A, DIGITAL INPUT CAPACITANCE

Capacitance to ground measured at digital input. This chiefly affects propagation delays when driven by CMOS logic.

M. P_D, POWER DISSIPATION: I+, I-

Quiescent power dissipation, $P_D = (V+ \times I+) + (V- \times I-)$. This may be specified both operating and standby ("Enable" pin ON/OFF). Note that, as with all CMOS devices, dissipation increases with switching frequency; but that Harris devices exhibit much less of this effect.

CARE AND FEEDING OF MULTIPLEXERS AND SWITCHES

Dielectrically isolated CMOS I.C.'s require no more care in handling and use than any other semiconductor—bipolar or otherwise. However, they are not indestructible, and reasonable common sense care should be taken.

In a laboratory breadboard, power should be shut off before inserting or removing any I.C.. It is especially important that supply lines have decoupling capacitors to ground permanently installed at the I.C. socket pins, as intermittent supply connections can create high voltage spikes through the inductance of a few feet of wire.

Because each of the major manufacturers of CMOS multiplexers and switches uses a radically different process, it is urged that units from all prospective suppliers be equally tested in breadboards and prototypes. It will be interesting to note which types survive best the hazards of a few weeks of breadboard testing.

Particular care of semiconductors during incoming inspection and installation is quite important, because the cost of reworking finished assemblies with even a small percentage of preventable failures can seriously erode profits. All equipment should be periodically inspected for proper grounding. With these devices, it is not usually necessary to shackle personnel to the nearest water pipe, if reasonable attention is paid to clothing and floor coverings; but be alert for periods of unusually high static electricity. If special lines are already set up for handling MOS devices, it wouldn't hurt to use them.

There are a few good rules for P.C. card layout:

1. Each card or removable subassembly should contain decoupling capacitors for each supply line to ground. This not only helps keep noise away from the analog lines, but gives good protection from static electricity damage when loose cards are handled.
2. When digital inputs come through a card connector, the pull-up resistor should be at the CMOS input. This forces current through the connector and prevents possible dry circuit conditions (see following discussion on digital interface).
3. All unused digital inputs must be tied to logic "0" (ground) or logic "1" (logic supply or

device + supply) depending on truth table and action desired. Open inputs tend to oscillate between "0" and "1". It would also be best to ground any unused analog inputs/outputs and any uncommitted device pins.

DIGITAL INTERFACE

A. REFERENCE CONNECTION

HI-5040 through HI-5051 and HI-1800A/1818A/1828A require a connection to the digital logic supply (+5V to +15V).

The HI-200/201/506A/507A have V_{REF} pins which are normally left open when driving from +5 Volt logic (DTL or TTL), but may be connected to higher logic supplies (to +15V) to raise the threshold levels when driving from CMOS or HNIL. The HI-200/201 will have significantly lower power dissipation when V_{REF} is connected to a high level supply.

The HI-506/507/508A/509A do not have V_{REF} terminals, but will operate reliably with any logic supplied from +5 to +15 Volts.

B. DTL/TTL INTERFACE

One major difference found in comparisons of similar devices from different manufacturers is the worst-case digital input high threshold (V_{AH} or V_{IH}). These range anywhere from +2V to +5V; and anything greater than +2.4V is obviously not compatible with worst-case TTL output levels. The fact is that no CMOS input is truly TTL compatible unless an external pull-up resistor is added. TTL output stages were not designed with CMOS loads in mind.

The experienced designer will always add a pull-up resistor from the CMOS input to the +5 Volt supply when driving from TTL/DTL:

1. Interchangeability: allows subsititution of similar devices from several manufacturers.
2. Noise immunity: a TTL output in the "high" condition can be quite high impedance. Even when voltage noise immunity seems satisfactory, the line is quite susceptible to induced noise. The pull-up resistor will reduce the impedance while increasing voltage noise immunity.
3. Compatibility: one manufacturer does guarantee +2.0 Volt minimum V_{AH}. However, this is accomplished with circuitry that is anything but TTL compatible: input current vs. voltage shows an abrupt positive then negative resistance region which is not the kind of load recommended for an emitter follower stage. A pull-up resistor will swamp out the negative resistance. Other CMOS inputs capacitively couple internal switching spikes to the input which could cause double-triggering without the pull-up resistor.
4. Reliability: it shouldn't happen with carefully processed I.C.'s; but any possible long term degradation of CMOS devices usually involves threshold voltage shifts. The pull-up resistor will help maintain operation if input thresholds drift out of spec. On units without adequate input protection, the resistor will also help protect the device when a loose P.C. card is handled. Where the interface goes through a P.C. connector, the resistor will force current through the connector to break down any insulating film which otherwise might build up and cause erratic dry circuit operation.

   A 2K ohm resistor connected from the CMOS input to the +5 Volt supply is adequate for any TTL type output. If power consumption is critical, open collector TTL/DTL should be used, allowing a higher value resistor—the voltage drop across the resistor is computed from the sum of specified "1" level leakage currents at the TTL output and CMOS input.

C. CMOS INTERFACE

The digital input circuitry on all Harris devices is identical to series 4000 and 54C/74C logic inputs, and is compatible with CMOS logic with supplies between +5V and +15V without external pull-up resistors.

D. ELECTROMECHANICAL INTERFACE

When driving inputs from mechanical switches or relays, either a pull-up or pull-down resistor must be connected at the CMOS input to clear the dry circuit and damp out any spikes, as illustrated in Figure 2, (b) and (c).

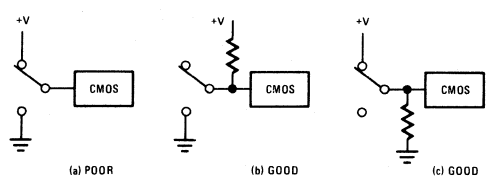


Figure 2

A PRACTICAL MULTIPLEXER APPLICATION

Figure 3 illustrates a practical data acquisition system hookup using an analog multiplexer, a monolithic sample-and-hold and an A/D converter. The HA-2420/2425 sample-and-hold is a particularly good choice for this type application because it eliminates the need for a separate high impedance, high slew rate buffer amplifier. Its acquisition time is consistent with CMOS multiplexer settling times and most available A/D conversion times. Errors, after initial

adjustment, are consistent with up to 12 bit absolute accuracy over a wide temperature range.

A. ACCURACY

D.C. error sources include:

1. Multiplexer:
   a. input offset = R source x I_S(OFF)
   b. output offset = R(ON) x (I_D(ON) + I bias (S/H))
2. Sample-and-hold
   a. input offset voltage
   b. charge injection; sample-to-hold offset
   c. gain error during "hold"
   d. drift during hold
3. A/D converter:
   a. linearity
   b. gain drift
   c. offset drift

Item 1(a) and (b), and 2(d) become significant only at very high temperatures. 2(a) and (b) are initially adjusted out with the offset adjustment pot on the S/H. 2(c) is usually adjusted out by A/D gain adjustment, but could also be removed by a voltage divider feedback on the S/H to give a slightly greater than unity gain during "sample". After initial adjustments, typical S/H errors are less than 0.5mV over 0° to +75°C. Note that after adjustment, there may be an appreciable offset at the S/H output when switching from sample to hold. This is not a problem, since accuracy is required only during "hold", and the system is adjusted for this.

The largest system errors are usually 3(b) and (c), drifts with temperature and time. If two multiplexer channels can be dedicated for stable (+) and (-) reference voltage inputs, then the data processor can continuously calibrate the system, effectively removing all errors, except 1(a) and 3(a) which are usually negligible.

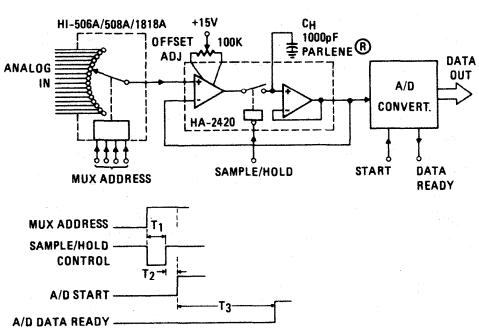


Figure 3

B. TIMING

The timing diagram in Figure 3 indicates the necessary system delays for each multiplexer address:

T_1 is the combined acquisition time for the multiplexer and S/H.

T_2 is the short interval required for the sample-to-hold transient to settle.

T_3 is the A/D conversion time.

The following table indicates minimum recommended timing for ± 10 Volt input range for acquisition/settling times to ½ L.S.B. accuracy:

	T_1	T_2
10 bit:	6μS	1μS
12 bit:	12μS	2μS

The multiplexer, by itself, requires about 2 μs and 9 μs settling to 10 bit and 12 bit accuracy, respectively; but fortunately this can be concurrent with S/H acquisition time. This is longer than would be predicted by the R_{ON} C_D time constant; probably because of internal distributed capacitance, a rather long period is required to traverse the last few millivolts towards the final value.

It should be noted that impedance conditions at the multiplexer inputs can affect the necessary acquisition time. At the instant the multiplexer switches from one channel to a new one, there is appreciable current pulled through the new channel input in order to charge C_D from its old level to its new level. This can cause ringing on signal lines, or glitches at signal conditioning amplifier outputs which require longer periods to settle. It is best for signal conditioning amplifiers to be wide band types, such as HA-2600, so that their high frequency output impedance is low and recovery from load transients is fast; even though the signal to be measured is very low bandwidth.

The T_1 and T_2 times could be eliminated by alternating two S/H circuits, acquiring a new signal on the second while A/D conversion is taking place. The two S/H circuits would have inputs connected together, and outputs alternately connected to the A/D by an analog switch. Total time, then, would be T_3 plus the analog switch settling time.

If the MUX input channels are sequentially switched, each channel will be sampled at a rate of

$$F_S = \frac{1}{N(T_1 + T_2 + T_3)}$$ samples per second, where N is the number of channels. The frequency spectra of the input signals must then be no higher than $\frac{F_S}{2}$.

In many systems, however, each channel carries a different maximum frequency of interest, and it may be desirable to depart from simple sequential scanning. Quickly varying signals, for example, could be addressed several times during a scanning period.

C. ADDING CHANNELS

For more than sixteen channels, several multiplexers may be tied together at the outputs, and addressed in parallel, but with only one "enabled" at a time. The MUX output offset will be increased, since I_D (OFF or ON) is additive. Also, output capacitance, C_D, is additive, creating increased access times.

These errors can be minimized in large systems by

having several tiered levels of multiplexing; where the outputs of a number of MUX's are individually connected to the inputs of another MUX.

D. DIFFERENTIAL MULTIPLEXING

When low level analog signals must be conducted over a distance, it is generally better, from a noise pickup standpoint, to use a balanced transmission line carrying signals which are differential with respect to ground.

A dual multiplexer is used for this purpose, as shown in Figure 4. Two sample-and-hold circuits plus an op amp form a high impedance differential sample-and-hold with gain. At gains greater than 4, the minimum sampling time (T_1 in previous example) must be increased proportionately to gain to allow for overdamped settling characteristics.

When handling low level, or high impedance signals, consideration should be given to adding signal conditioning amplifiers at the signal sources, since this can often produce less troublesome, more accurate, lower cost systems.

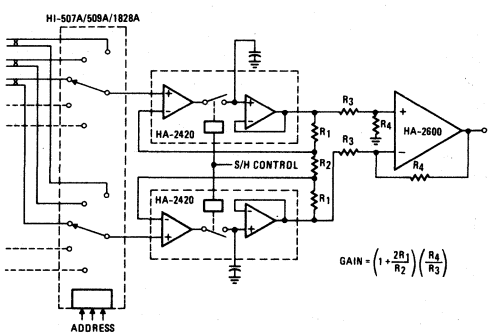


Figure 4

E. DEMULTIPLEXING

Since the switches in a CMOS MUX conduct equally well in either direction, it is perfectly feasible to use it as a single input-selected multiple output switch. Figure 5 illustrates its use as a demultiplexer, with capacitors to hold the output signal between samples. When the address lines are synchronous with the address of the original multiplexer, the output lines will recreate the original inputs, except level changes will be in steps.

Overvoltage protection is not effective with signals injected at the normal MUX output, so an external network should be added, if necessary.

A more accurate demultiplexer could be constructed using the HA-2420/2425 sample-and-hold for each channel, connecting inputs together and sampling each channel sequentially.

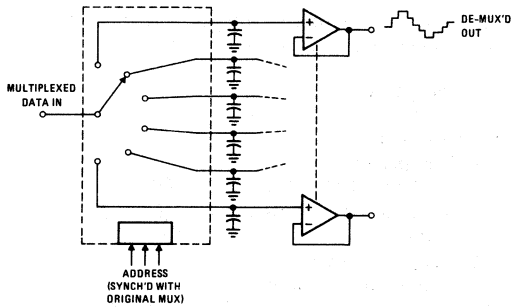


Figure 5

ANALOG SWITCH APPLICATIONS

A. HIGH CURRENT SWITCHING

Analog switches are sometimes required to conduct appreciable amounts of current, either continuous, or instantaneous—such as charging or discharging a capacitor. For best reliability, it is recommended that instantaneous current be limited to less than 80mA peak and that average power over any 100 millisecond period be limited to $I^2R_{ON} \leq$ (absolute max. derated power—quiescent power). Note that R_{ON} increases at high current levels, which is characteristic of any FET switch. Switching elements may be connected in parallel to reduce R_{ON}.

B. OP AMP SWITCHING APPLICATIONS

When analog switches are used either to select an op amp input, or to change op amp gain, minor circuit rearrangements can frequently enhance accuracy. In Figure 6 (a), R_{ON} of the input selector switch adds to R_1, reducing gain and allowing gain to change with temperature. By switching into a non-inverting amplifier (b), gain change becomes negligible. Similarly, in a gain switching circuit, R_{ON} is part of the gain determining network in (c), but has negligible effect in (d).

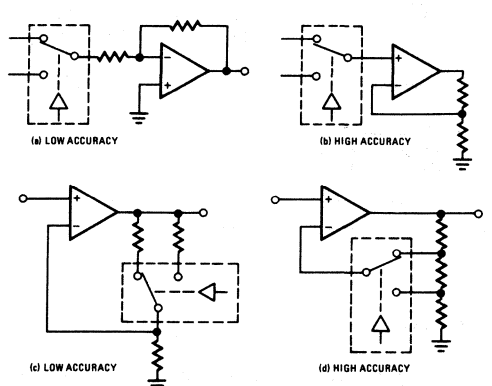


Figure 6

C. SWITCHING SPIKES AND CHARGE INJECTION

Transient effects when turning a switch off or on are of concern in certain applications. Short duration spikes are generated (Figure 7 (a)) as a result of capacitive coupling between digital signals and the analog output. These have the effect of creating an acquisition time interval during which the output level is invalid even when little or no steady state level change is involved. The total net energy (charge injection) coupled to the analog circuit is of concern when switching the voltage on a capacitor, since the injected charge will change the capacitor voltage at the instant the switch is opened (Figure 7 (b)).

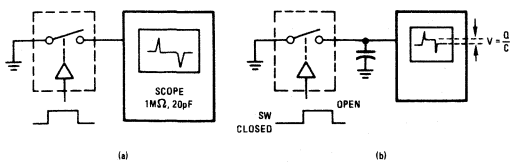


Figure 7

Charge injection is measured in pico Coulombs; the voltage transferred to the capacitor computed by

$$V = \frac{\text{Charge (pC)}}{\text{Capacitance (pF)}}$$

Both of these effects are, in general, considerably less for CMOS switches than for equivalent resistance JFET or PMOS devices, since the gate drive signals for the two switching transistors are of opposite polarity. However, complete cancellation is not possible, since the N and P channel switches do not receive gate signals quite simultaneously, and their geometrics are necessarily different to achieve the desired D.C. resistance match.

In applications where transients create a problem, it is frequently possible to minimize the effect by cancellation in a differential circuit, similar to Figure 8.

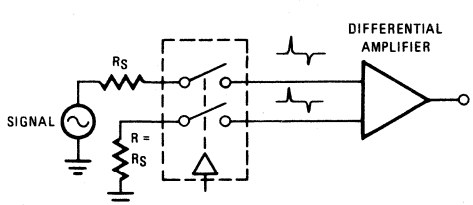


Figure 8

Among the Harris anlog switches, the HI-201 is the best from the transient standpoint, having turn-on spikes of about 100mV peak, 50ns width at the 50% point, and charge injection at turn-off of about 20 pico Coulombs. Transients of the HI-5040 series are several times higher.

D. HIGH FREQUENCY SWITCHING

When considering a switching element for R.F. or video type information, two factors must be watched: attenuation vs. frequency characteristics of an ON switch, and feedthrough vs. frequency characteristics of the OFF switch. Optimizing the first characteristic requires a low $R_{ON} \times C_D$ product, and the second a low value of C_{DS} (OFF).

The 30 ohm switch types of the HI-5040 series appear to best meet these requirements, and testing at high frequencies has verified this.

Figure 9 illustrates these circuit configurations; (a) is a simple series switch, (b) is a series-shunt configuration to reduce feedthrough, and (c) is a SPDT selector configuration with series-shunt elements. A 1K ohm load is illustrated, which might be the input impedance of a buffer amplifier stage; a lower load resistance would improve the response characteristics, but would create greater losses in the switch and would tend to distort high level signals.

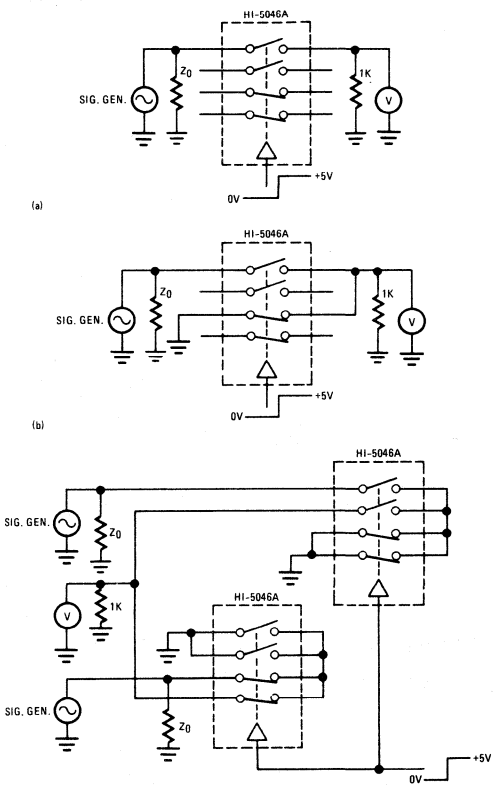


Figure 9

Figure 10 shows ON and OFF frequency response for each of the above configurations. Arbitrarily, we will define useful frequency response as the

region where ON losses are less than -3dB and OFF isolation is greater than -40dB.

The simple configuration (a) has excellent ON response, but OFF isolation limits the useful range to about 1MHz (the data sheet indicates -80dB isolation at 100kHz, but this is measured with 100 ohms load, which accounts for the 20dB difference).

The circuit in (b) shows a good improvement in isolation produced by the low impedance of the shunt switch. The useful range is about 10MHz; which could also be achieved in a simple SPDT 2-switch selector if source impedances are very low.

The selector switch in (c) has excellent characteristics, both ON and OFF curves indicating 40MHz useful response. Additional switches connected to the same point would reduce the ON response because of added shunt capacitance; but this could be eliminated by feeding separate summing amplifier inputs.

Careful layout is, of course, important for high frequency switching applications to avoid feedthrough paths or excessive load capacitance.

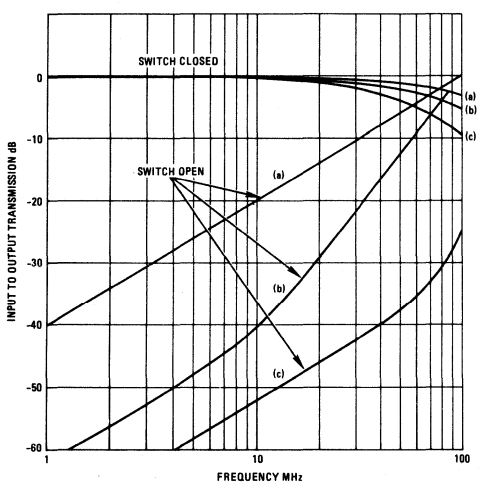


Figure 10

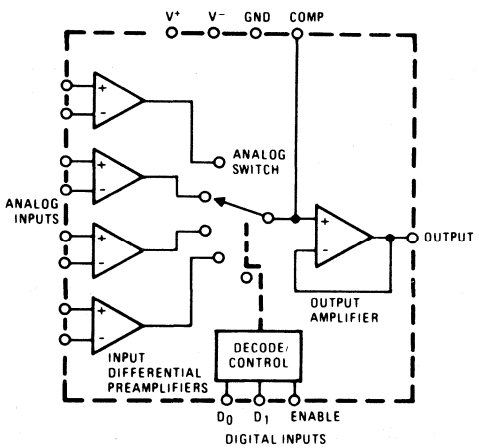
ALTERNATIVES TO CMOS SWITCHES AND MULTIPLEXERS

CMOS devices are excellent in many applications. However, there are some other devices which merit consideration in certain analog switching circuits where they may improve performance, reduce parts count, or be more economical.

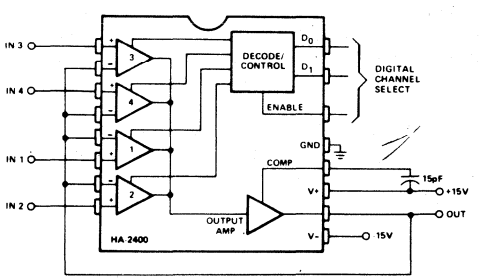
A. THE PRAM, PROGRAMMABLE AMPLIFIER

The HA-2400/2405 is a unique monolithic bipolar circuit which combines analog switching with high performance operational amplifiers. It basically consists of four op amp type input stages, any one of which is connected to a single output by bipolar switches controlled through a TTL compatible address decoder. In a single package, it contains the equivalent of 5 op amps plus a 4 channel mulitplexer. It has literally hundreds of applications in signal selection and programmable signal conditioning.

Figure 11 illustrates a four channel multiplexer. Connections from the output to each input stage are always the same as a comparable op amp circuit; the +1 gain connection is illustrated.



(a) FUNCTIONAL DIAGRAM



(b) ANALOG MULTIPLEXER WITH BUFFERED INPUT AND OUTPUT

Figure 11

Advantages over a comparable CMOS multiplexer circuit are as follows:

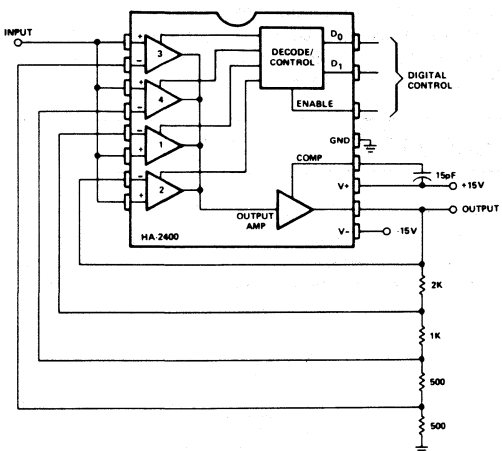
1. High input impedance (10^{12} ohms), low output impedance (< 0.1 ohm) means that ON resistance and leakage currents are no longer of concern. There is negligible transient loading of input lines.
2. Gain filtering, etc. can easily be added with feedback networks.
3. Fast acquisition (1.5μS).

4. Wide bandwidth (8 MHz).
5. Superior feedthrough characteristics (-110dB at 10kHz, -60dB at 1MHz).

Disadvantages include:

1. Less accuracy for low level D.C. signals; the offset voltages of each input stage do not necessarily match or track each other.
2. Cannot be used in reverse as a demultiplexer.
3. Disabling the device (enable pin low) does not open the output line, or drive the output to zero. Adding channels may be accomplished by tieing compensation pins together.

Figure 12 illustrates the PRAM used as a programmable gain amplifier. Any connection possible with op amps can be wired 4 ways to make programmable active filters, oscillators, etc., etc. Harris Application Note 514 shows many possibilities.



AMPLIFIER, NON-INVERTING PROGRAMMABLE GAIN

Figure 12

B. SAMPLE-AND-HOLD

The sample-and-hold function has often been accomplished with separate analog switches and op amps. These designs always involve performance tradeoffs between acquisition time, charge injection, and droop rate.

The HA-2420/2425 monolithic sample-and-hold, illustrated previously in Figure 3 has many times better tradeoffs, usually at a lower total cost than the other approaches. The switching element is a complementary bipolar circuit with feedback which allows high charging currents (30mA), low charge injection (10pC), and ultra low OFF leakage current (5pA); a combination not approached in any other electronic switch. These factors make it also superior as an integrator reset switch, or as a precision peak detector as shown in Figure 13. Harris Application Note 517 illustrates many other applications.

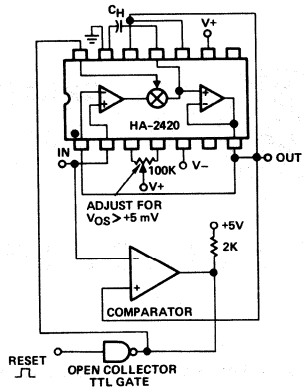


Figure 13

C. PROGRAMMABLE SUPPLY CURRENT OP AMPS

The HA-2720/2725 and HA-2730/2735 (dual amp) are op amps with an extra terminal which is used to control quiescent supply current. These are most generally used in low power systems to optimize the power dissipation vs. bandwidth and slew rate tradeoffs. They can also be used with variable set currents to make linearly variable oscillators, filters, etc. Another application is a switchable op amp as shown in Figure 14.

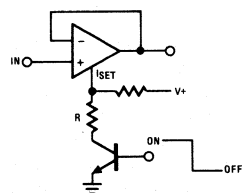


Figure 14

The illustrated transistor could be the output of high voltage open collector gate. The set resistor R is chosen so that the set current is the desired value when the transistor is ON, considering that the voltage at I_{SET} terminal when ON is about 2 forward junction drops ($\sim$ 1.5V) below V+. When the transistor is turned OFF, amplifier input, output, and supply terminals become very high impedance, so that two or more amplifier outputs could alternately be switched to the same point.

Off isolation with a 2,000 ohm load is about -80dB at 10kHz.

D. CHOPPER STABILIZED AMPLIFIER

Analog switches are sometimes used as choppers for amplifying low level D.C. signals with low offset errors. The HA-2900/2905 is a monolithic chopper stabilized amplifier in a TO-99 can. Typical offset drifts are 0.2 μV/^{o}C and 1pA/^{o}C with 5 x 10^8 open loop gain. Harris Application Note 518 describes this device.

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APPLICATION NOTE 521

GETTING THE MOST OUT OF C-MOS DEVICES FOR ANALOG SWITCHING JOBS

BY ERNIE THIBODEAUX

INTRODUCTION

Although most designers appreciate the benefits of the complementary-MOS process for digital design, few realize how effective the technology can be for analog switching. C-MOS analog switches, which consume less power than bipolar devices, exhibit no dc offset voltage and can handle signals up to the supply rails. The C-MOS bilateral property furnishes input and output functions, making multiplexing and demultiplexing possible. In addition, the on-resistance of an MOS switch is as low as 30 ohms—a third as much as a bipolar device.

Unfortunately, C-MOS analog switches, which until recently were built with junction isolation, have been difficult to design into analog multiplexers and switches. The devices latched up easily, their C-MOS inputs were destroyed by electrostatic charges, and they literally went up in smoke when confronted with input overvoltage spikes and power-supply transients. To prevent destruction, costly external protective circuits were needed, and, even then, the devices latched up unless the power was turned on and off in a set sequence.

Because latch-up problems limited the use of analog switches so severely, device designers focused a great deal of attention on eliminating the condition. Recently, the success has been noteworthy. Indeed, three new technologies now offer latch-free analog switch operation: latch-proof junction isolation (JI), floating-body junction isolation, and dielectric isolation (DI).

Both JI techniques are conventional processes that have been slightly modified to alleviate the old problem of latch-up. However, both of these JI technologies still require costly external protection circuits to guard against burn-out in such applications as analog-signal multiplexing that interface them with the outside world. That is why JI devices are best suited for internal-switching applications where the electrical environment can be controlled. In contrast, the improved DI technology, by virtue of its construction, offers analog-switching devices suitable for many inside applications, as well as providing in-board analog protection for devices that interface with the other circuits. Happily, the smaller substrate area of the DI device delivers a better speed-power product than the JI technology.

THE BASIC C-MOS SWITCH

The basic C-MOS transistor (Fig. 1) has parasitic junctions that are reverse-biased during normal operation. However, certain overvoltage conditions can forward-bias these junctions to cause high currents that could possibly destroy the devices.

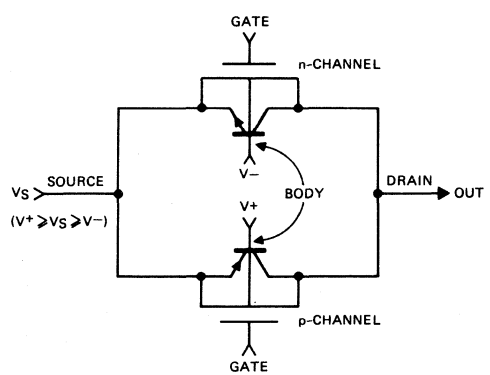

Figure 1. Bad
In the basic C-MOS analog switch, the parasitic junctions are reversed-biased during normal operation. Large overvoltages, however, make them forward-biased and draw large currents.

The parasitic junctions are actually npn and pnp transistors that are normally reverse-biased by the applied body potentials. However, because many analog switches, and especially multiplexers, are connected to their analog sources through long lines, they are highly susceptible to externally induced voltage spikes. For example, these spikes, which can often exceed the p-channel body potential, V+, can inadvertently turn on a normally off switch

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through the parasitic pnp transistor (Fig. 1).

The n-channel device is similarly affected when the parasitic npn transistor is turned on by a negative overvoltage. This action, commonly known as channel interaction, causes momentary channel-to-channel shorting, which introduces significant errors in the system. This intermittent condition, which is seldom destructive, is rarely isolated because it occurs only randomly.

One of the adverse effects of channel interaction is illustrated in Fig. 2. Channel 1 of an analog multiplexer is selected when all other channels are off. Channel 16 receives an input-noise spike that momentarily exceeds the positive supply. The sequence causes channel 1 read-out to be +16V because of interaction with channel 16 just before initiating the hold command to the sample-and-hold device. To prevent this annoyance requires additional protective circuits that clamp each channel input to a voltage below the threshold of the parasitics to ensure that the channels remain inactive under any conditions.

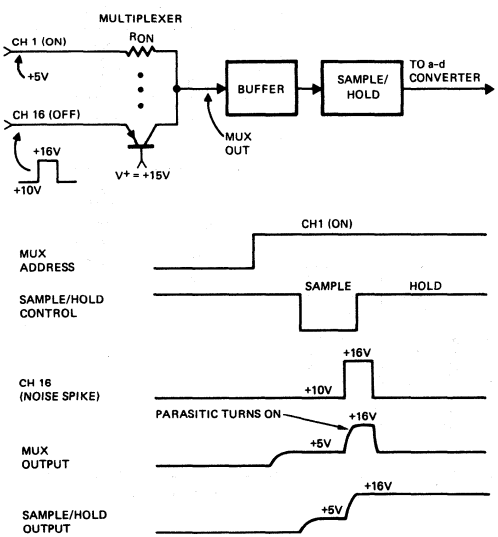

Figure 2. Worse

With CMOS devices, noise spikes can cause channel interaction. In this multiplexer, although channel 1 is only one selected, noise spikes cause cross talk in channel 16, which affects reading.

A more serious condition exists when the substrates (p- or n-) lose their respective potentials to ground (Fig. 3) —a condition that occurs when power to the device is turned off while the analog signals are still present. In this situation, the analog switch, which at that point represents a diode connected through the low impedance of the supply, draws high current from the analog source.

This current turns on the switch through its parasitics and shorts all channels to the output. These shorts can easily be catastrophic in multiplexer systems that have different power supplies for the analog source and the multiplexer switch. An error during trouble-shooting or an inadvertent supply glitch can trigger this fault mode and destroy the whole system. Therefore, there is obviously much more to system reliability than having latch-proof C-MOS devices.

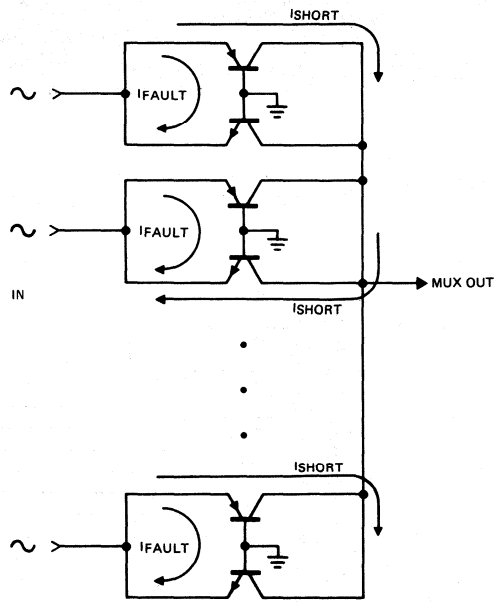

Figure 3. Still Worse

Most serious in CMOS switches is losing substrate potential to ground. This condition, which happens when power is lost and the analog signal is present, causes very high currents.

CONSIDERING LATCH-PROOF JI TECHNOLOGY

The standard JI process has been modified by what is claimed to be latch-proof construction through control of the effective betas of the parasitic transistors. A cross section in Fig. 4(a) shows the C-MOS structure along with its parasitic transistors and the equivalent circuit in Fig. 4(b) that gives rise to the silicon-controlled-rectifier latch-up problem.

Under any of the fault conditions previously mentioned, the npn and/or pnp can trigger this quasi-dual-gate SCR into a state of high conduction. If the transistor β product is 1 or greater, this configuration is sustained until either the device burns up or all sources of power are removed. By using a buried-layer configuration, as shown in the cross section, the β product is reduced to less than 1, eliminating the latch-up conditions.

Again, especially in multiplexer applications, the latch-free devices do not guarantee against destruction, and the JI multiplexer still requires costly discrete circuits around the device, as shown in Fig 5. If an overvoltage exists, the resistor/diode circuit at each analog input limits the input voltage to the

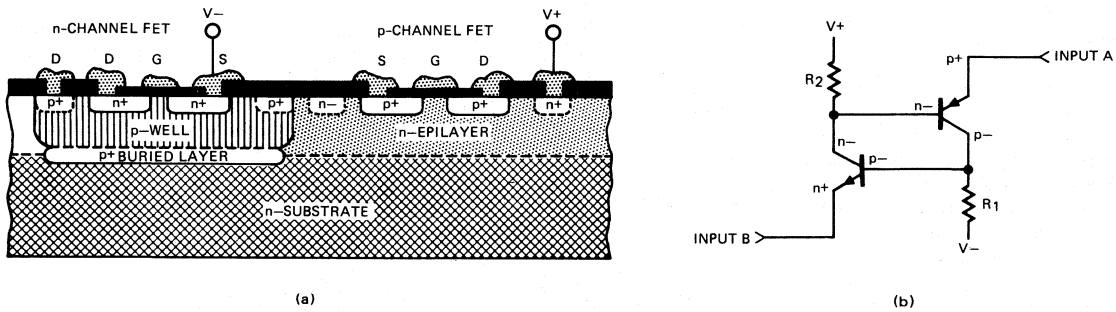

Figure 4. Latch-Proof. Junction-isolated devices are now made latch-proof with a buried-layer configuration (a), which keeps beta of parasitic transistor under unity. That kills chance for latch-up (b), which plagues devices built with older junction-isolation technology.

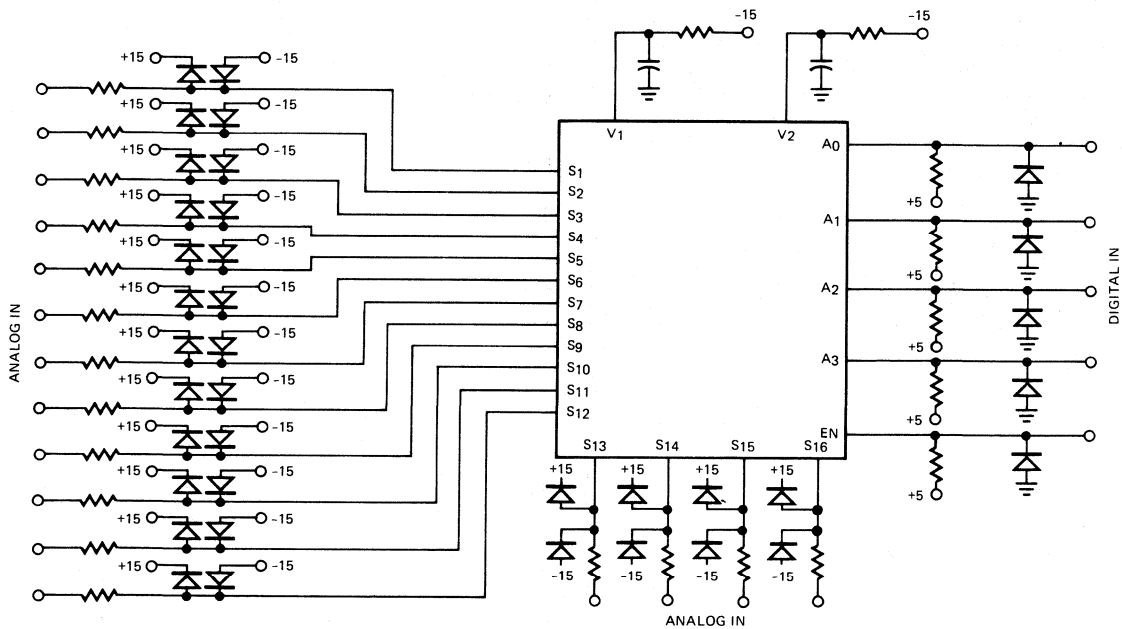

Figure 5. Protection still needed. Although new JI devices won't latch up, they still can be destroyed by large currents. That's why typical JI multiplexers, like the one shown here, still need to be surrounded by external protective components, which drive up system costs.

supply-voltage range to prevent the parasitic transistor action.

The resistors limit the overvoltage currents through the diodes. The diodes must have a low threshold voltage—much lower than the 0.6V silicon-junction threshold of the internal parasitic diodes—to ensure that the parasitics do not turn on.

A germanium diode offers a low threshold voltage, but its high leakage current makes it impractical, especially in 0.1% systems. Therefore, in most applications, more expensive low-leakage diodes are used.

For example, Schottky diodes meet the requirements, but they cost about 50 cents each in volume, and the total cost per multiplexer, including parts and labor, for the discrete protection circuit may well be double the initial purchase price of the device. Even then, its reliability will never approach that of an IC that has this protection already built in.

THE FLOATING-BODY JI TECHNOLOGY

Standard JI technology allows another approach to latch-proof device construction: a portion of the SCR continuity is broken by floating the "body" or substrate of the n-channel switching device. A cross section of this process is similar to that in Fig. 4(a), excluding the buried layer and the negative supply connection to the p- substrate, so that the dual-gate SCR is changed to a single -gate device that can only be triggered by the pnp parasitic. This, of course, reduces the latch-up probability by 50%.

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To completely eliminate latch-up, as before, the β product of the transistors is reduced to less than 1. This accomplishment, certainly a significant improvement over the conventional process, offers greater reliability, but certain trade-offs must be made when the body of a MOSFET is floated.

Nominal source-to-drain breakdown voltages are reduced which limit the peak-to-peak signal range. Over-all breakdown is limited by the collector-emitter breakdown voltage, BV_{CEO}, of the npn parasitic transistor of the floating n-channel MOSFET. The breakdown voltage increases with the degree of reverse-bias potential applied to the substrate. With a floating body, BV_{CEO} is minimum, so particular care is necessary when using these devices in configurations such as single-pole single-throw, single-pole double-throw, dpst, and dpdt, where each side of the switch connects to opposite polarities. The peak-to-peak handling capability is specified at a minimum of 22V; therefore, 30V pk-pk cannot be switched with ± 15V supplies, as it can with other C-MOS devices.

What's more, the leakage currents of floating-body JI devices are higher than other types, simply because the I_{CEO} of the floating base for the npn is much greater than the I_{CBO} of other devices having fixed reversed-biased body potentials. The increased leakage currents in spst switches may not be too significant.

However, in multiplexers that have the outputs of as many as 16 switches tied together in one IC, the total summation of currents can significantly affect system accuracy. For example, the specification for a worst-case 16-channel floating-body multiplexer is 10 microamperes, and the channel on resistance is 550 ohms . The dc-offset error would be 5.5 millivolts, representing an accuracy to 0.055%.

Other 16-channel types specify worst-case parameters of 500 nanoamperes and channel resistance between 550 ohms and 2 kilohms. Their dc-offset error is between 0.28 mV and 1 mV, respectively, allowing accuracy to 0.01% or better.

Finally, the effective off impedance of the floating-body switch is degraded by the floating-body technique. Off-isolation characteristics of a MOSFET are primarily determined by its source-to-drain capacitance. But with the base floating, the effective capacitance from emitter to collector is increased by the series combination of emitter-base and base-collector-junction capacitances (Fig. 6a). This increase degrades the over-all off-isolation characteristics. For example, the off isolation for a typical floating-body channel at 1 megahertz that has RL = 100 ohms is specified to be -54 decibels, which compares favorable with other types. However, at lower frequencies such as 1 kHz, the isolation is only -62dB, compared to more than -110dB for improved devices. Capacitances C_1 and C_2 for them are shunted by the low ac impedance of the supply voltage (Fig. 6b).

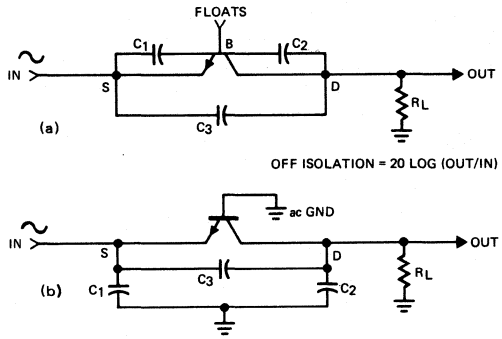

Figure 6. Floating Bodies

Floating-body switches have degraded "off" impedance because total capacitance (a) combines two junction capacitances. In DI circuit (b), capacitances are shunted out.

THE LINEAR DIELECTRIC-ISOLATION TECHNOLOGY

The linear dielectric-isolation process requires no modifications to guard against latch-up. Its basic construction ensures that the SCR configuration that causes latch-up can not exist. The functional cross section in Fig. 7 reveals the silicon-dioxide isolation barrier fabricated between all parasitic transistors. This isolation allows each active element to be self-contained and independent with no interface junctions. At most, only three-layer structures are permitted for each tub, so that four-layer strucures, or SCRs, are impossible. Also, since the DI technology requires no guard bands, junction capacitances, leakage currents, and size are minimized. The resulting increase in packing density per wafer, together with increased yields, enables these devices to be cost-competitive with other types.

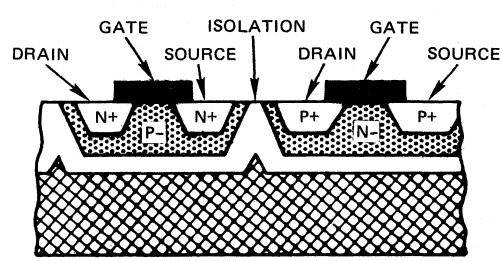

Figure 7. How DI Does It

Dielectric isolation eliminates latch-up by a silicon-dioxide isolation barrier between devices. This separates all active elements, eliminating interface junctions that cause parasitic SCR's.

In working with DI devices, the IC designer is not burdened with the fixed substrate potentials found in JI devices. He may let the substrate float, fix it to some potential, or even modulate it. Fig. 8 depicts a typical DI analog switch circuit that minimizes the variation of on resistance with the analog signal. Ordinarily, in conventional circuits, the body or

substrate potentials of the n and p-channel devices are fixed and the source-to-body bias potentials vary with the analog input voltage. This change in body bias causes a wide variation of on resistance within the analog signal range. However, in the DI circuit, the bodies of P_1 and N_1 are connected together through N_3 during the on state. This allows the body to follow the input voltage providing a constant source-body bias and therefore a constant on resistance. During the off state, the bodies of N_1 and P_1 are at their respective supply potentials through P_2 and N_2, thereby preserving high off isolation and low leakage currents.

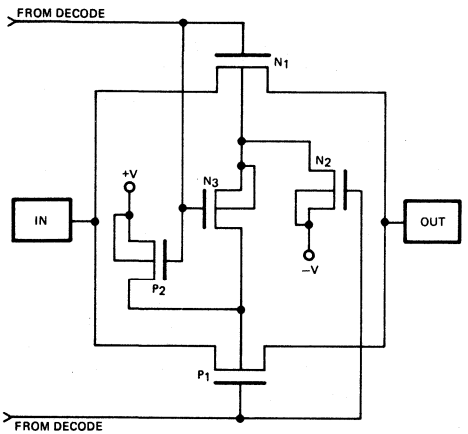

Figure 8. DI Does It

In dielectrically isolated switches, on resistance modulation by the analog input is minimized by connecting N_1 and P_1 bodies together through N_3.

DESIGNING A FOOLPROOF C-MOS ANALOG MULTIPLEXER

In dielectrically isolated multiplexer circuits, protection can be provided on the chip primarily to eliminate channel interaction. This protection prevents normally off channels from being turned on by parasitics from other channels. And because this interaction is prevented, even worst-case power-supply faults cannot destroy the device. Moreover, since DI structures have no SCR effect, protection against latch-up and power-sequencing are not necessary. In short, DI multiplexers with built-in protection can withstand virtually any conceivable fault from the outside world.

The typical protected DI multiplexer (Fig. 9) benefits from a combined bipolar/C-MOS technology. The illustrated bipolar section is used to sense an analog overvoltage condition and steer current away from the parasitic MOSFET junctions. Each of the switching devices, N_1 and P_1, has its own protection circuits. Devices P_3, D_6, D_7 and Q_6 protect P_1 while N_3, D_4, D_5, and Q_5 protect N_1. When the switch is off, the substrate of the p-channel FET, P_1, is connected to V+ through P_3 and diode D_7 for maximum isolation and low leakage currents in the off state. If the input voltage suddenly exceeds V+, the source-body junction, which would normally conduct, is instead clamped by transistor Q_6.

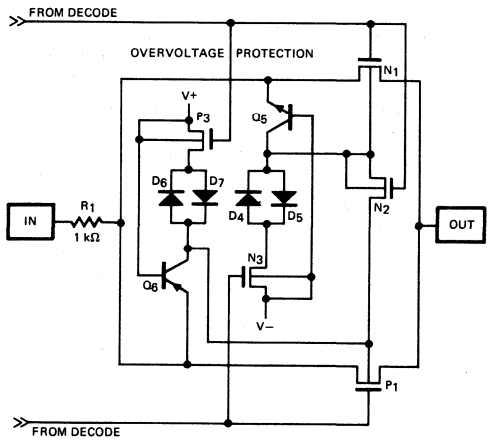

Figure 9. Winning Combination

Combining bipolar and MOS technologies in the same multiplexer gives built-in protection. This circuit is typical for each channel in multiplexers HI-506A, HI-507A, HI-508A, and HI-509A.

The base-emitter junction conducts to hold the source-body diode off with a saturation voltage $V_{CE(SAT)}$ of about 0.2V. Thus clamped, the switch is protected from the effects of overvoltage.

Clamp Q_6 always turns on before the forward-voltage drop of the source-body diode is exceeded because diode D_6 requires an additional forward-voltage drop for conduction through the parasitic junction. Moreover, resistor R_1 limits the current flowing through Q_6 when high overvoltages exist. Although R_1 adds to the total on-resistance of the channel, its associated error is insignificant, since most systems provide high-impedance buffering anyway. For negative overvoltages, N_1 is similarly protected. What's more, the protection circuit, rated at a nominal overvoltage of ±33V, reveals a cross-talk current of only about 5na (Fig. 10).

When the switch is normally turned on, the substrates of N_1 and P_1 are connected together through N_2, which, as described before, results in a constant on resistance.

This condition represents an absolute error from channel interaction of only 6 microvolts (R_{ON} x 5_{NA})—certainly negligible in most systems. In contrast, floating-body types have guarantees only that they won't be burned up by ±25V overvoltage. Their manufacturers do not make any claim against channel interaction. In fact, channel interaction occurs readily in these devices when the n- and p-channel thresholds are exceeded by an overvolt-

age. For example, the n-channel device, although floating, would be inadvertently turned on if the analog input exceeded the negative supply by its gate-to-source threshold, which is typically 1.5V.

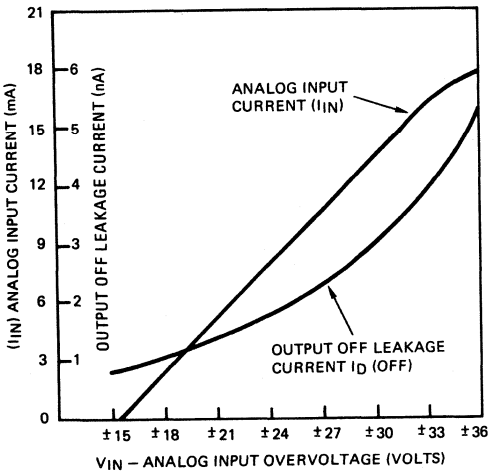

Figure 10. Blocking Cross Talk

DI switches have minimal cross-talk problems. An overvoltage of 33V produces a cross-talk current of only 5nA—an absolute error from channel interaction of only 6 μV.

ADDING BENEFITS

RESULTS OF DIGITAL-INPUT PROTECTION TESTS (20 DIELECTRICALLY ISOLATED UNITS)

STRESS STEP/VOLTS	FAILURES
500	0
1,000	0
1,500	0
2,000	1
2,500	0
3,000	3
3,500	0
4,000	3

Additional DI benefits are passed on to the user in the design of the digital input-protection circuit shown in Fig. 11. The fabrication of all components as isolated silicon islands eliminates any possibility of latch-up. The diodes switch fast and quickly discharge any static charge that may appear at the digital MOS input gates. The table gives the results of a step-stress analysis performed on 20 units. A total of 80% survived the 3.5 kilovolt level, and only one failed below 2kV.

The DI technology enables a wide variety of active elements to be integrated on the same chip to provide maximum versatility. For example, in the transistor-transistor-logic/C-MOS reference circuit shown in

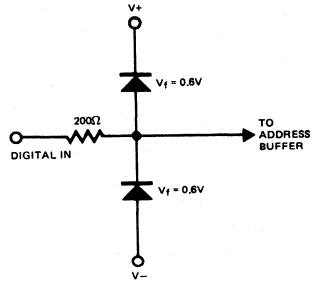

Figure 11. Digital Protection

DI devices also protect digital inputs. For example, the diodes in this circuit quickly discharge any static charge that may appear on an MOS input gate.

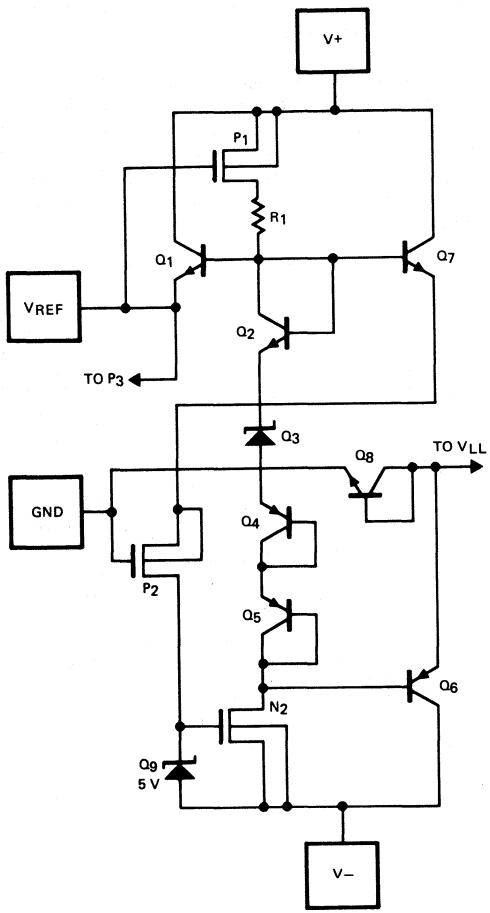

Figure 12. Packing It In

DI technology increases chip density of analog switch, allowing more circuit capability per package. For example, DI designs make possible this internal logic reference circuit in HI-200 and HI-201 switches.

Fig. 12, the bipolar technology enables realization of a simple zener reference circuit, consisting of resistor R_2 and transistors Q_1, Q_2, and Q_3.

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The circuit develops a stable 5V reference for interfacing with TTL and eliminates the need for an additional 5V logic supply. Current for the zener (Q_3) is supplied through the normally on MOSFET, P_1, which can be easily turned off if not needed to minimize power consumption when interfacing with C-MOS-logic circuits. P_1 turns off when V+ or supply voltage V_{DD} is applied to the reference terminal V_{REF} to convert the IC's power-consumption from bipolar to C-MOS level. If power is not critical, V_{REF} can be left open to speed switching.

In high-speed data-acquisition systems, the designer is concerned with both quiescent power and dynamic power consumption. If JI devices are used, the capacitance or leakage currents are so high they contribute a major portion of total power consumption. That situation is caused by the large-geometry parasitic junctions formed by the n- junction.

In contrast, the smaller substrate area of the DI device provides much less power drain. Dynamic-power consumption as a function of frequency for several 16-channel analog multiplexers with ±15V supplies is shown in Fig. 13. The DI device consumes only 100mW at 1 MHz to yield the best speed-power product.

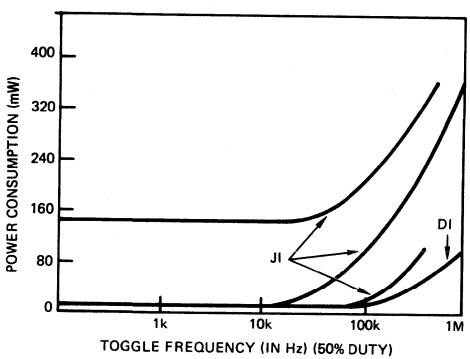

Figure 13. DI Performs
DI devices not only perform well, but do it with less power. Dynamic-power-consumption data for commercial multiplexers shows DI device consuming only 100mW at 1MHz.

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APPLICATION NOTE 522

DIGITAL TO ANALOG CONVERTER TERMINOLOGY

BY DICK TI TUNG

INTRODUCTION

In recent years the development and rapid reduction in cost of digital integrated circuits have resulted in an explosion in the applications of digital processing systems in the area of data acquisition and automatic process control. The need for a building block, such as the digital-to-analog converter (DAC), which interfaces the digital system with the analog world, is evident.

The purpose of digital-to-analog conversion is to produce a unique but consistent analog quantity, voltage or current, for a given digital input code. The most commonly used input digital code to a DAC is the natural binary number. A natural binary number is represented as

$$N = A_n2^n + A_{n-1}2^{n-1} + \ldots + A_12^1 + A_02^0 + A_{-1}2^{-1} + \ldots + A_{-n}2^{-n}$$

where the coefficients A_i (for $n \geq i \geq -n$) assume the values of "0" or "1" and is called a "bit". The left half portion of the binary number N

$$A_n2^n + A_{n-1}2^{n-1} + \ldots + A_12^1 + A_02^0$$

constitutes the integer part of the number N, whereas the right portion

$$A_{-1}2^{-1} + A_{-2}2^{-2} + \ldots + A_{-n}2^{-n}$$

constitutes the fractional part of the number N. The bit that carries the greatest weight (left most bit) is called the most significant bit, or MSB. Similarly, the bit with the smallest weight (right most bit) is called the least significant bit, or LSB.

The analog output of a n-bit binary DAC is related to its binary number in the following manner:

$$E_o = FS(A_{-1}2^{-1} + A_{-2}2^{-2} + \ldots + A_{-n}2^{-n})$$

where the term FS is defined as the nominal Full-Scale output of the DAC and it is known as the unreachable Full-Scale. It is easy to see that the actual Full-Scale output of the DAC, E_{FS}, with all the input bits "1" is

$$E_{FS} = FS(2^{-1} + 2^{-2} + \ldots + 2^{-n}) = FS(1-2^{-n}).$$

The term $FS(1/2^n)$ is the smallest output level that the DAC can resolve and it is known as the 1 LSB output level change. It is universal practice that the input code of a DAC is written in the form of binary integer with the fractional nature of the corresponding number understood.

As an example, the transfer function of an ideal 3-bit binary DAC is plotted as shown in Figure 1. Since a 3-bit DAC has only 8 discrete input codes which correspond to 8 different output levels (ranging from zero to 7/8 FS), no other output levels can exist and it is plotted as a bar graph. The line that connects the Zero and FS is called the Gain Curve.

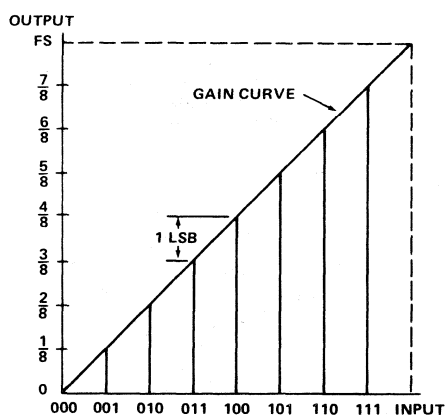

Figure 1 – Ideal Transfer Function Straight Binary (Unipolar)

There are two other input codings associated with binary DACs known as Bipolar codes, which are offset binary and two's complement binary codes. The offset binary code is obtained by offsetting the binary code such that the half-scale code, 10 . . . 0, becomes zero. And the two's complement code is achieved by inverting the MSB of the offset binary

6

code such that it is mathematically consistent with computer arithmetic. The transfer functions for the 3-bit DAC with offset binary input code and two's complement input code are plotted as shown in Figure 2 and Figure 3, respectively. (The +FS and -FS limits are used for easy interpretation of Bipolar operations. They are not confined by the previous definition of FS.)

In practical DACs, the zero output level may not be exactly zero (offset error), the range from zero to FS may not be exactly as specified (gain error), the differences in output levels may not be changing uniformly (nonlinearity), and so on. In selecting a DAC for a given application, some characteristics may have to be weighted more than the others. An understanding of some of the terms and characteristics involved in D/A conversion is helpful in choosing the correct part.

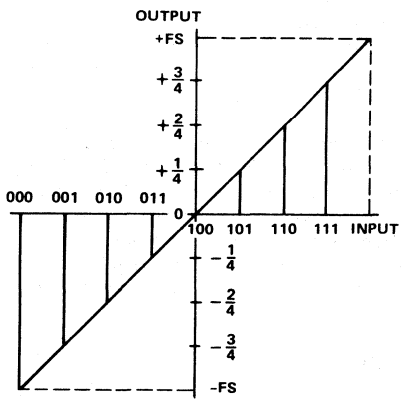

Figure 2 — Ideal Transfer Function Offset Binary (Bipolar)

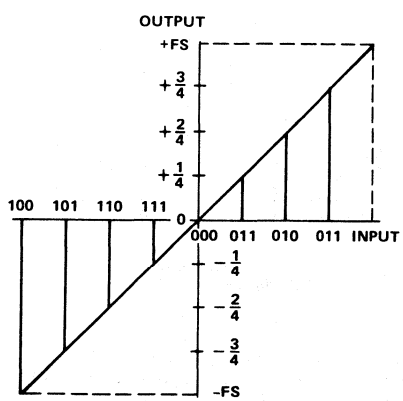

Figure 3 — Ideal Transfer Function Two's Complement (Bipolar)

TERMINOLOGY

Least Significant Bit (LSB) — The digital input bit carrying the lowest numerical weight ($1/2^n$); or the analog output level shift associated with this bit ($FSR/2^n$) which is the smallest possible analog output step.

Most Significant Bit (MSB) — The digital input bit carrying the highest numerical weight (1/2); or the analog output level shift associated with this bit. In a binary DAC the MSB creates a 1/2 FSR output level shift.

Resolution — An indication of the number of possible analog output levels a DAC will produce. Usually, it is expressed as the number of input bits. For example, a 12-bit binary DAC will have $2^{12} = 4096$ possible output levels (including zero) and it has a resolution of 12 bits.

Absolute Accuracy — A measure of the deviation of the analog output level from the ideal value under any input combination. Accuracy can be expressed as a percentage of full scale range, a number of bits (n bits accuracy means a magnitude of $1/2^n$ FSR possible error may exist), or a fraction of the LSB (if a DAC with n-bit resolution has 1/2 LSB accuracy the magnitude of the possible error is $1/2(1/2^n FSR)$). Accuracy may be of the same, higher, or lower order of magnitude as the resolution. Possible error in individual bit weight may be cumulative with combination of bits and may change due to temperature variations. Usually, the accuracy of a DAC is expressed in terms of nonlinearity, differential nonlinearity, and zero and gain drift due to temperature variations.

Nonlinearity (linearity error) — A measure of the deviation of the analog output level from an ideal straight line transfer curve drawn between zero and full scale (commonly referred as endpoint linearity).

Differential Nonlinearity — A measure of the deviation between the actual output level change from the ideal (1 LSB) output level change for a one bit change in input code. A differential nonlinearity of ± 1 LSB or less guarantees monotonicity; that is the output always increases for an increasing input.

Gain Drift — A measure of the change in full scale analog output, with all bits 1's, over the specified temperature range expressed in parts per million of full scale range per °C (PPM of FSR/°C). It is measured with respect to +25°C at high (T_H) and low (T_L) temperature, and it is specified the larger of the two representing worst case drift.

Offset Drift (Unipolar or Bipolar) — A measure of the change in analog output, with all bits 0's, over the specified temperature range expressed in parts per million of full scale range per °C (PPM of FSR/°C). It is measured with respect to +25°C at high (T_H) and low (T_L) temperature, and it is specified the larger of the two representing worst case drift.

Settling Time – The total time measured from a digital input change to the time the analog output reaches its new value within a specified error band. Usually, the settling time is specified for a DAC to settle for a Full-Scale code change (00 . . . 0 to 11 . . . 1 or 11 . . . 1 to 00 . . .0) to within ±1/2 LSB of its final value.

Compliance – Compliance voltage is the maximum output voltage range that can be tolerated and still maintain the specified accuracy.

The effects of gain error, offset error, nonlinearity, and differential nonlinearity on the transfer functions are plotted, respectively, as shown in Figure 4, 5, 6, & 7. A conversion chart which shows the number of bits and its resolution is given in Table 1.

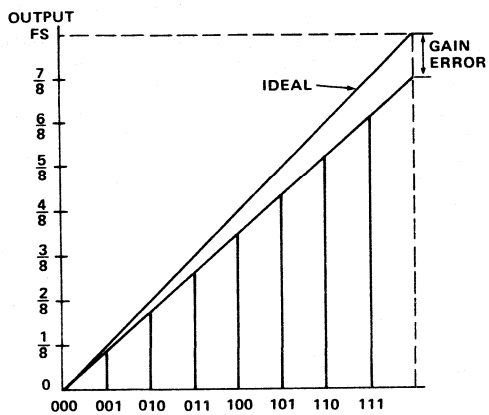

Figure 4 – Gain Error

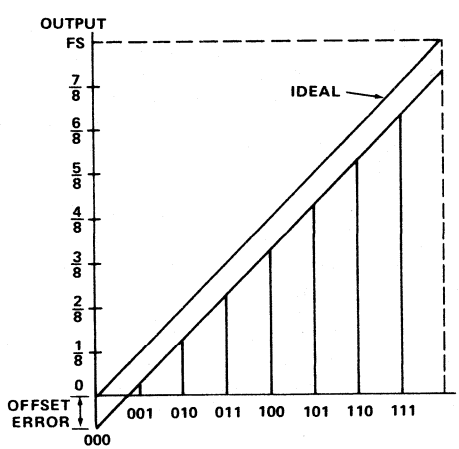

Figure 5 – Offset Error

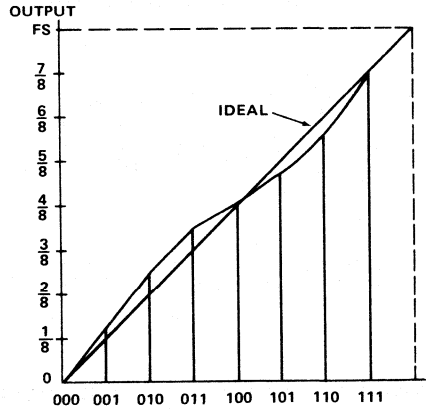

Figure 6 – Linearity Error

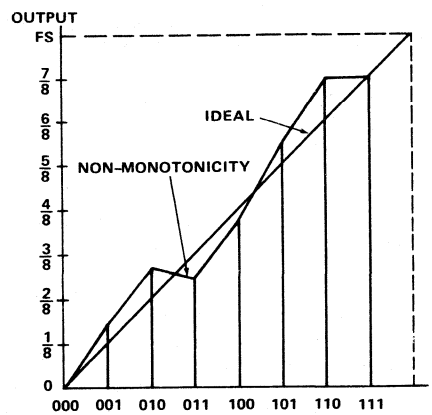

Figure 7 – Differential Linearity Error (Non-Monotonicity)

Table 1 – Conversion Chart

# OF BITS	LSB	RESOLUTION		TEMPCO PPM/°C – 1 LSB DRIFT OVER	
		%	PPM	0°C ≤ TA ≤ 75°C	-55°C ≤ TA ≤ 125°C
6	FS/64	1.5620	15,625	208.3	86.8
7	FS/128	0.7812	7.812	104.2	43.4
8	FS/256	0.3906	3,906	52.1	21.7
9	FS/512	0.1953	1,953	26.0	10.9
10	FS/1024	0.0977	977	13.0	5.4
11	FS/2048	0.0488	488	6.5	2.7
12	FS/4096	0.0244	244	3.3	1.4
13	FS/8192	0.0122	122	1.6	0.68
14	FS/16384	0.00610	61	0.8	0.34
15	FS/32768	0.00305	31	0.4	0.17
16	FS/65536	0.00153	15	0.2	0.08

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APPLICATION NOTE 523

DIGITAL TO ANALOG CONVERTER HIGH SPEED DAC FAMILY

BY DICK TI TUNG

THE HIGH SPEED DAC FAMILY

The Harris Semiconductor high speed DAC family includes the following high speed current output monolithic DAC's:

HI-562	12 bits
HI-5618	8 bits
HI-5610	10 bits

They are especially designed to meet the fast settling requirements of computer graphics, CRT displays, and high speed analog-to-digital converter applications. The high speed DAC's are constructed using the Harris high frequency bipolar dielectric isolation (DI) process. Basically, the DAC's are identical in design and have the same chip size. The operating temperature range and package of the DAC's, and their typical characteristics are tabulated in Table 1 and Table 2, respectively. The functional diagrams are shown in Figure 1 to Figure 3.

Functionally, the high speed DAC's consist of a high performance control amplifier, an array of identical current sources, an R-2R resistor ladder, and an input digital interface network. When an external +10V reference is applied to the +input of the control amplifier through the internal 8K resistor, it establishes a reference collector current of 1.25mA through the first NPN transistor and forces the other transistors to have the same collector current. These constant current sources are controlled by the digital inputs and it will either switch to ground or switch to the output through the resistor ladder network. A portion of the bias is fed back through the 2K to the control amplifier to maintain the constant current at all times.

The use of current sources to drive the ladder network has several advantages over voltage sources. Within the constant current range of the sources, the current output will remain constant regardless of variations in the negative supply voltage, and also switching of a current source generally is faster, creates less ringing at the output, and produces smaller power supply transients.

The R-2R ladder network is constructed from high stability thin film nichrome resistors deposited on the same silicon chip. Identical material is used for the resistor in the reference supply network, span resistor, and in the current source circuitry to achieve good temperature stability. The current setting resistors and span resistors are LASER trimmed to provide the guaranteed accuracy.

The output accuracy of the high speed DAC's depends mainly on the accuracy of the voltage applied to the V_{REF} inputs. The output level is directly proportional to the reference voltage. For high precision performance a precision +10V voltage reference with reasonably low temperature coefficient, such as the Harris HA-1610 is highly recommended.

In addition to an external +10V reference, the DAC's require a logic power supply (V_{PS+}) and a -15V analog power supply (V_{PS-}) for operation. The digital input logic level is TTL/CMOS selectable. For TTL input operation, connect pin 2 to ground and use +5V for logic power supply. If CMOS input level is desired, connect pin 2 to pin 1 and use the CMOS power supply as logic power supply. The analog output of a current output DAC can be terminated in a resistive load to ground to produce a voltage output within the specified compliance voltage.

For higher voltage output operation, use an external op amp as a current-to-voltage converter and the internal scaling resistors as feedback elements for optimum accuracy and temperature coefficient. The selected op amp should have a good front-end temperature coefficient such as the HA-2600/2605, with offset voltage and offset current tempco's of 5μV/^{o}C and 1nA/^{o}C, respectively. For high speed voltage output applications where fast settling is required, the HA-5190 op amp is recommended.

As a rule of thumb, when wiring a system consisting of both digital and analog signals, power supply decoupling and single point grounding method should be used. A single point grounding system means that all the ground pins of devices in the system should be connected to a single point. This reduces the effect

of ground level fluctuation between devices. The grounding and decoupling scheme of high speed DAC's is shown in Figure 4. The decoupling capacitors should be connected close to the device pins, and should be tantalum or electrolytic bypassed with ceramic types for high frequency noise rejection.

The input reference resistor (7.975K) and bipolar offset resistor (3.975K) are both internally set low by 25Ω to allow the user to externally trim-out initial errors to a high degree of precision. The simplified operational diagrams for the high speed DAC's together with op amp hookup are given as shown in Figure 5 to Figure 7. The connections for various operations and their corresponding output levels are listed in Table 3 to Table 5. The calibration procedures are given as follows.

UNIPOLAR CALIBRATION

Step 1
- Offset Adjustment
- Turn all bits off (all 0's)
- Adjust R_3 for zero volts output

Step 2
- Gain Adjustment
- Turn all bits on (all 1's)
- Adjust R_1 for an output of FS - 1LSB

BIPOLAR CALIBRATION

Step 1
- Op amp Null Adjustment
- Short op amp output to inverting input
- Adjust R_3 for zero volts output

Step 2
- Gain Adjustment
- Turn all bits on (all 1's) and all bits off (all 0's) and record the voltage difference
- Adjust R_1 till the output voltage difference equals to actual full scale voltage

Step 3
- Offset Adjustment
- Turn bit 1 (MSB) on, all other bits off (10. . .0)
- Adjust R_2 for zero volts output

MAJOR CARRY TRANSIENT AND GLITCHES

Whenever the digital input to a DAC changes, large transients, called glitches, may appear at the output before it reaches to its final value. These glitches are caused from unequal internal turn-on and turn-off switching times.

If, for example, the turn-on time is longer than turn-off time, an intermediate state of 0's occurs during a transition from binary 7 to binary 8 for a 3-bit DAC. Thus, instead of swinging smoothly from the output corresponding to 7 to that of 8, the output instantaneously swings towards zero before getting back to where it is supposed to be. It is easy to see that the worst case glitches occur at the half-scale or major carry code transition, from 01. . .1 to 10. . .0 or 10. . .0 to 01. . .1. In this case, the temporary state of all 0's can cause a half-scale magnitude glitch.

In a specific application, where glitches are highly undesirable, the use of rapid symmetrical switches at digital inputs will reduce glitches considerably. For voltage output, a sample and hold amplifier (HA-2425) used as current-to-voltage converter would also provide the deglitching function.

Figure 8 shows the diagrams of a high speed sample and hold circuit designed by Harris linear applications. It is capable of slewing a signal at a rate of 1V/50ns in the sample made, and the droop rate will not exceed 500 μV/100ns. The duration of the "hold" could be user selected by changing the RC constant of the monostable multivibrator; it in turn blanks the undesirable portion of the transient response of the DAC.

Table 1. Operating Temperature Range Selection Chart

SELECTIONS		PACKAGE	OPERATING TEMPERATURE RANGE	
			-2 AND -8	-5
HI-562	12 Bits	24-Lead DIP	-55°C to +125°C	0°C to +75°C
HI-5618	8 Bits	18-Lead DIP	-55°C to +125°C	0°C to +75°C
HI-5610	10 Bits	24-Lead DIP	-55°C to +125°C	0°C to +75°C

Table 2. Typical Characteristics

PARAMETER	TEMP	HI-562	HI-5618	HI-5610	UNITS
Resolution	Full	12	8	10	BITS
Nonlinearity	Full	1/2	1/4	1/4	LSB
Differential Nonlinearity	Full	1/2	1/4	1/4	LSB
Gain Drift	Full	5	5	5	ppm of FSR/°C
Unipolar Offset Drift	Full	2	3	3	ppm of FSR/°C
Bipolar Offset Drift	Full	2	3	3	ppm of FSR/°C
Output Current (Full Scale)	Full	-5	-5	-5	mA

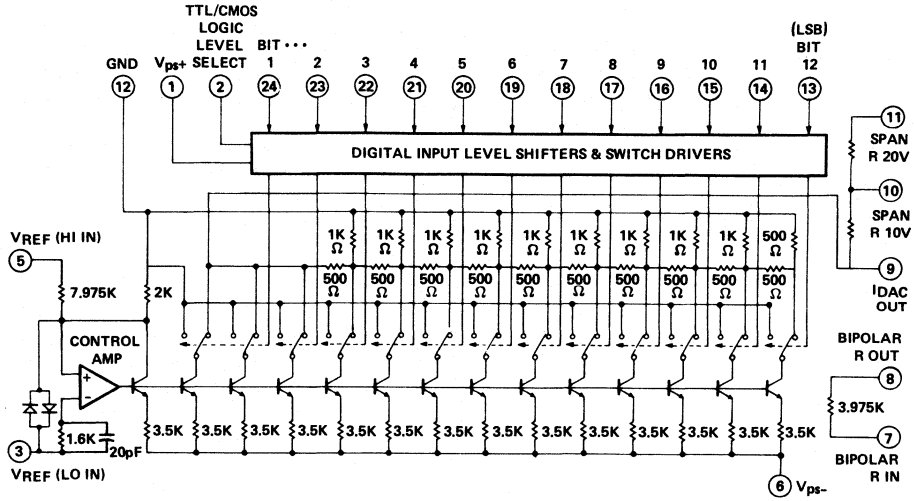


Figure 1. HI-562 Functional Diagram

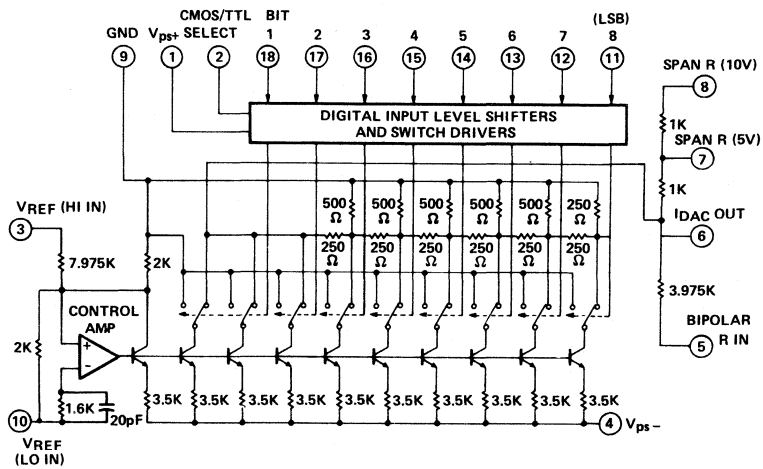


Figure 2. HI-5618 Functional Diagram

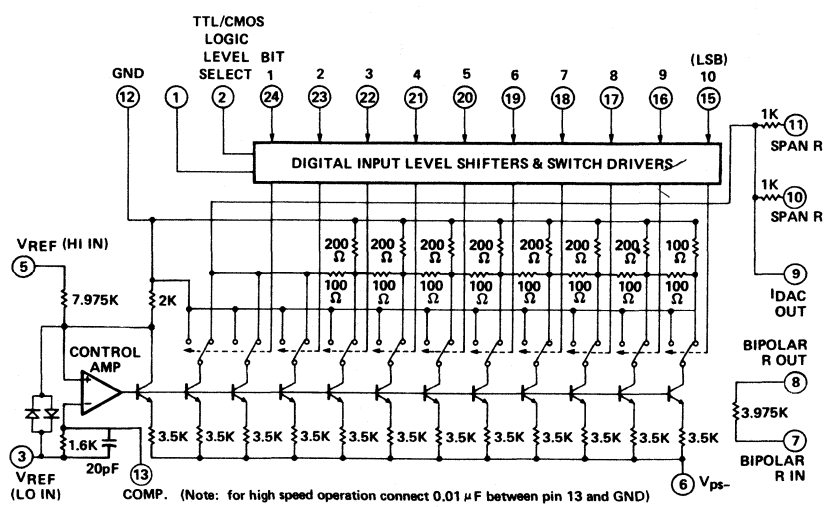
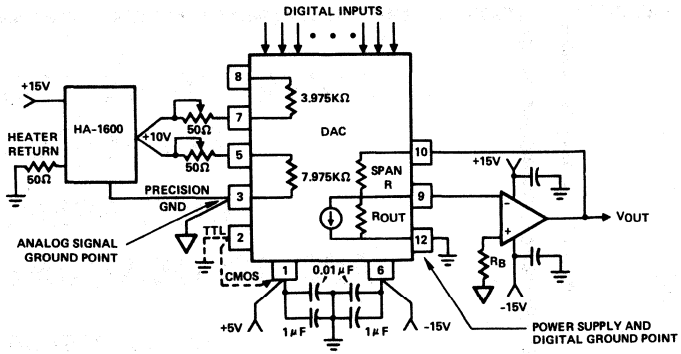


Figure 3. HI-5610 Functional Diagram



POWER SUPPLY AND DIGITAL SIGNAL GROUND. CONNECT TO PIN 12 OF THE DAC.

ANALOG SIGNAL GROUND. CONNECT TO PIN 3 OF THE DAC.

BOTH GROUNDS SHOULD BE CONNECTED WITH A HEAVIER WIRE AT PIN 12.

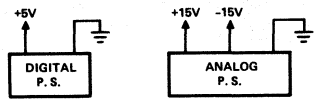


Figure 4. Decoupling and Grounding Scheme

Table 3. HI-562 Connection Chart

ANALOG OUTPUT MODE	OUTPUT RANGE	ACTUAL FULL SCALE	CONNECTIONS			R_B BIAS RESISTORS
			PIN 8 TO	PIN 10 TO	PIN 11 TO	
UNIPOLAR	0 to +10V	9.9976V	NC	A	NC	667Ω
	0 to +5V	4.9988V	NC	A	9	500Ω
BIPOLAR	±10V	19.9951V	9	NC	A	667Ω
	±5V	9.9976V	9	A	NC	580Ω
	±2.5V	4.9988V	9	A	9	444Ω

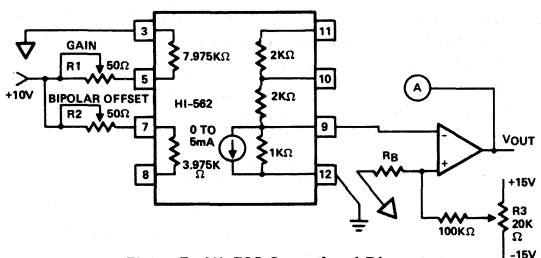


Figure 5. HI-562 Operational Diagram

Table 4. HI-5618 Connection Chart

ANALOG OUTPUT MODE	OUTPUT RANGE	ACTUAL FULL SCALE	CONNECTIONS			R_B BIAS RESISTORS
			PIN 5 TO	PIN 7 TO	PIN 8 TO	
UNIPOLAR	0 to +10V	9.9609V	NC	NC	B	400
	0 to +5V	4.9805V	NC	B	NC	333
	0 to +2.5V	2.4902V	NC	B	6	250
BIPOLAR	±5V	4.9609V	A	NC	B	364
	±2.5V	2.4805V	A	B	NC	307
	±1.25V	1.2402V	A	B	6	235

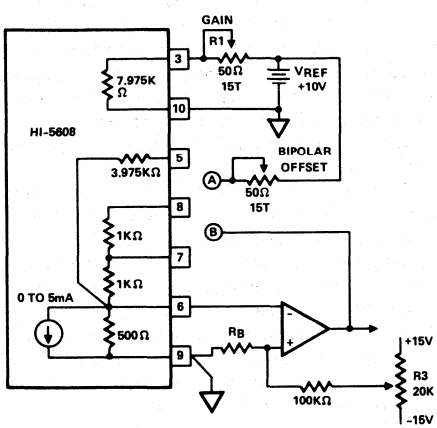


Figure 6. HI-5618 Operational Diagram

Table 5. HI-5610 Connection Chart

ANALOG OUTPUT MODE	OUTPUT RANGE	ACTUAL FULL SCALE	CONNECTIONS			R_B BIAS RESISTORS
			PIN 8 TO	PIN 10 TO	PIN 11 TO	
UNIPOLAR	0 to +5V	4.9951V	NC	A	NC	167Ω
	0 to 2.5V	2.4976V	NC	A	A	143Ω
BIPOLAR	±2.5V	4.9951V	9	A	NC	160Ω
	±1.25V	2.4976V	9	A	A	138Ω

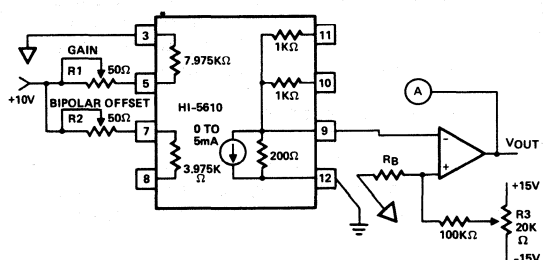


Figure 7. HI-5610 Operational Diagram

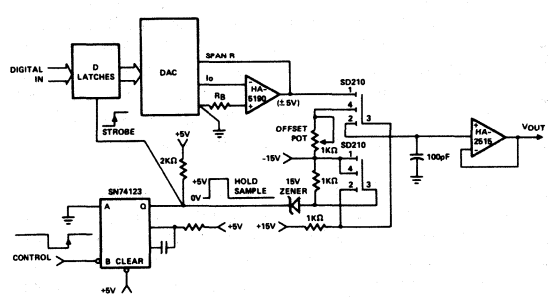


Figure 8. High Speed Deglitch Circuit

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

APPLICATION NOTE 524

DIGITAL TO ANALOG CONVERTER HIGH SPEED ADC APPLICATIONS

BY DICK TI TUNG

ANALOG-TO-DIGITAL CONVERTER (ADC)

The use of high speed DACs in CRT display, industrial process control, signal regeneration, etc., are well established. Perhaps one of the most important applications is to use the DAC in high speed ADC design. There are two types of ADC design where high speed and high resolution DACs are essential.

TRACKING ADC OR SERVO TYPE ADC

The tracking ADC is very efficient in monitoring one analog signal continuously, converting it into a sequence of digital codes representing the analog signal in real time.

Functionally, the analog input is compared with the output of a DAC, with the digital input of the DAC being driven by a counter. After the ADC is turned on, the counter increments until the DAC output crosses the analog input value. The counter will then, running up or down, drive the DAC 1 LSB at a time to track the input signal. The counter state represents the digital equivalent of the input signal.

In Figure 1, the analog input is fed into the span resistor of a DAC. The analog input voltage range is selectable in the same way as the output voltage range of the DAC. The net current flow through the ladder termination resistance, i.e. 1K for HI-562, produces an error voltage at the DAC output. This error voltage is compared with 1/2 LSB by a comparator. When the error voltage is within $\pm$ 1/2 LSB range, the Q output of the comparators are both low, which stops the counter and gives a data ready signal to indicate that the digital output is correct. If the error exceeds the $\pm$1/2 LSB range, the counter is enabled and driven in an up or down direction depending on the polarity of the error voltage.

Since the digital output changes state only when there is a significant change in the analog input, the data ready signal is then very useful in adaptive systems or computer systems for efficient data transfer. When monitoring a slowly varying input, it is necessary to read the digital output only after a change has taken place. The data ready signal could be used to trigger a flip-flop to indicate the condition and reset it after read-out.

The main disadvantage of the tracking ADC is that the time required to initially acquire a signal, for a 12 bit ADC, could be up to 4096 clock periods. The input signal usually must be filtered so that its rate of change does not exceed the tracking range of the ADC (1 LSB per clock period).

SUCCESSIVE-APPROXIMATION ADC

Perhaps the most widely used technique for a high speed analog-to-digital converter design is the successive approximation method. Ideal for interfacing with computers, this type is capable of both high speed and high resolution, and the conversion time is fixed and independent of the magnitude of the input voltage.

Figure 2 shows a block diagram of a successive-approximation ADC. When a negative going start conversion pulse is applied to the ADC, the internal registers of the successive approximation register (SAR) are set to low except for the MSB, which is set to high. This turns on the MSB of the DAC. The FS output current of the DAC is compared with the current fed through the span resistor by the analog input. The net current flow through the ladder termination resistance produces an error voltage at the DAC output. This error voltage is then compared with a fixed reference by a comparator to determine whether the analog input is greater or less than the present state of the DAC. The result of the comparison is clocked into the SAR at the rising edge of the clock. The MSB of the SAR will be set to high if the analog input is greater; otherwise, it will be set to low. At the same time, the second bit of the SAR is set to high with the remaining bits at their previous states. During the second clock period, the sum of the result of the first choice and the weight of the second bit is compared with the analog input. The second bit is set to high or low in the same manner as the MSB, and so on, until the LSB is updated.

During this conversion time, the output of a status flip-flop is set to high, indicating that a conversion is taking place. It will return to low at the end of conversion to signify that the output state of the SAR represents the digital equivalent of the input analog voltage.

It is easy to see that in any successive-approximation ADC application, the analog input should remain reasonably constant during the conversion to avoid erroneous results. This is usually accomplished by using a sample-and-hold circuit in the analog line.

DATA ACQUISITION SYSTEM

The functional diagram of a 16-channel data acquisition system is shown in Figure 3. Functionally, the outputs of the binary counter are fed to the 16-channel analog multiplexer to serve as the channel select signals, and it is also fed to the 4 line to 16 line digital decoder as address inputs. At the rising edge of the clock pulse, an analog input channel is selected, and the sample and hold circuit (S/H) is set to sample. The duration of the "1" state of the clock pulse should be adjusted such that the output of the S/H would settle to its required accuracy. At the falling edge of the clock pulse, the S/H holds the signal level acquired during the clock "1" state, and with one gate delay time, the ADC commences its conversion. Once the conversion is completed, the $\overline{CC}$ signal from the ADC will enable the decoder to send out a decoded signal to strobe the ADC output into the proper storage register. The duration of the "0" state of the clock pulse should be adjusted to allow the proper data entry to the storage register. The next analog input channel will be acquired for the next clock period, and so on. If a 50kHz clock pulse is used, the data will be refreshed every 320μs.

This 16-channel data acquisition system is applicable to industrial process control, and multi-channel panel display. It can also interface with an intelligent terminal, such as a micro-computer system, to provide multi-channel data conversion function. The offset error and gain error of the data acquisition system over the operating temperature range can be easily compensated by proper programming.

By the same token, a 15-channel data acquisition system with offset correction could be easily incorporated as shown in Figure 4. Consider the case that one of the analog input channels is dedicated to sense the ground level, and its binary equivalent is stored in latch register B in its complementary form to establish a ground reference in real time. All the other analog input channels will then be converted and stored in register A, one at a time. The binary adder will perform the binary subtraction in less than 1μs for the given pair of A and B. This, in fact, eliminates the offset error of the ADC, offset error of the S/H circuit, and excess droop of the S/H due to temperature variation.

This circuit is easy to implement and is especially useful when an intelligent terminal is not available. To expand this concept one step further, the gain error of the system due to temperature variations could also be eliminated if a binary multiplier is used to correct the gain facter in real time.

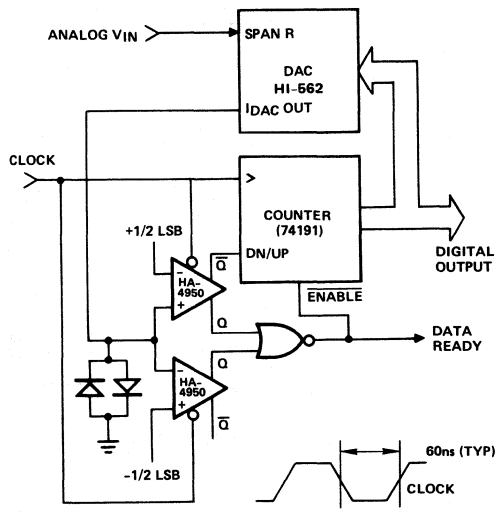


Figure 1. Tracking ADC

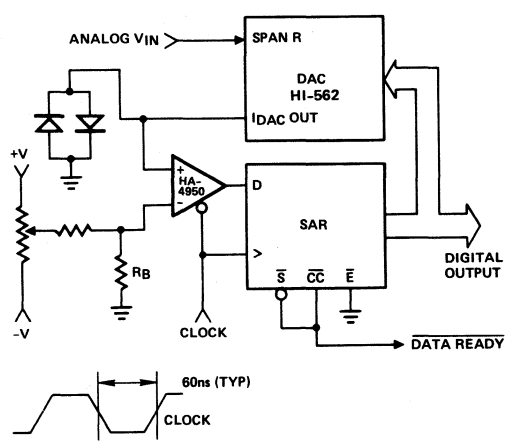


Figure 2. Successive-Approximation ADC

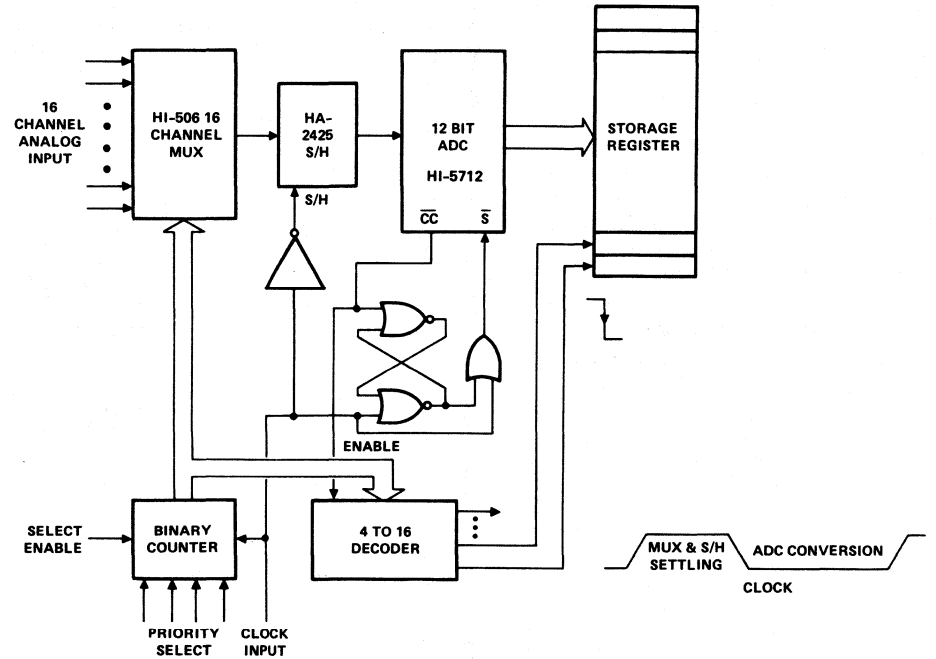


Figure 3. 16 Channel Data Acquisition System

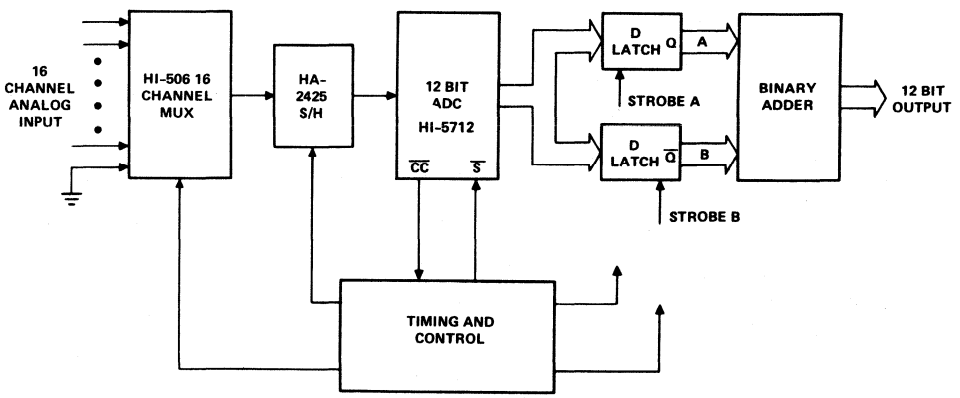


Figure 4. 15 Channel Data Acquisition System
with Offset Correction

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APPLICATION NOTE 525

HA-5190/5195 FAST SETTLING OPERATIONAL AMPLIFIER

MAY 1979

INTRODUCTION

The military temperature range HA-5190 and its commercial temperature equivalent, HA-5195, are monolithic operational amplifiers featuring ±200V/μs slew rate, 150mHz gain-bandwidth-product, and 70ns settling time. Similar performance has previously been available only in more costly modular and hybrid amplifiers, which require much higher bandwidth and slew rate to achieve the same settling time as HA-5190/5195. Since it exhibits a classical -6dB/octave rolloff over most of its frequency range, remarkably smooth output wave forms are generated by HA-5190 when reasonable care is employed.

Applications for this op amp include pulse, RF, and video amplifiers, wave form generators, high speed data acquisition and instrumentation circuits.

INSIDE THE HA-5190/5195

Figure 1 shows the schematic of the HA-5190/5195 design. The schematic can be simplified to show the AC signal path as shown in Figure 2.

The input stage consists of two symmetrical differential transistor pairs. The signal path for positive going signals is Q_1, Q_2, and Q_3, while negative going signals pass through Q_4, Q_5, and Q_6. The signal then goes through the output stage (represented by the voltage follower symbol) consisting of one PNP and two NPN emitter followers.

In Figure 2, the compensation network is C_1, C_2, C_3, and R_{29}. This network makes the amplifier system appear as second-order critically damped. The scheme produces the dominant pole plus two zeros. The zeros are positioned to cancel the effects of undesired poles developed by the F_t of the transistors.

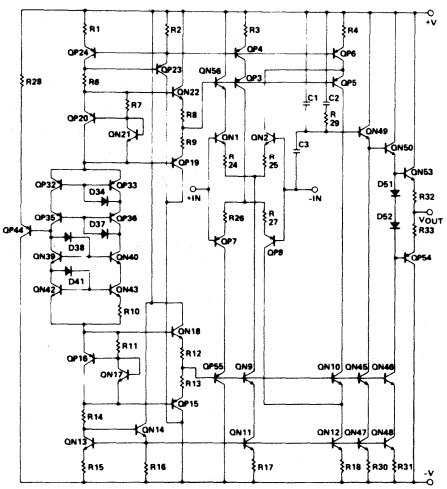


Figure 1. HA-5190/5195 Schematic.

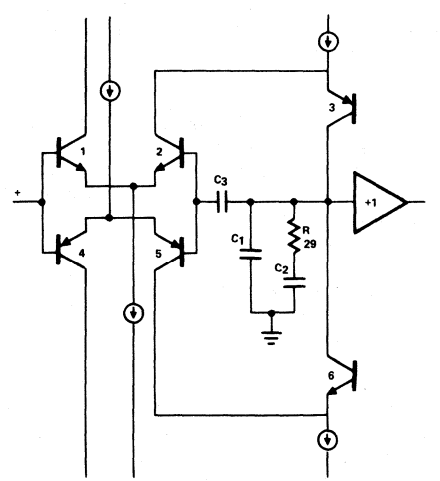


Figure 2. Simplified HA-5190 Schematic.

6

CONSIDERATIONS FOR PROTOTYPING

When using the HA-5190, high frequency layout techniques are recommended for bread-boarding. The device should be mounted through a ground plane. If an IC socket is to be used, Teflon types are recommended. Feedback components should be mounted between Teflon insulated standoffs located as close as possible to the device pins.

The input impedance characteristic of the HA-5190 is such that the closed loop performance (DC and AC) will depend on both the feedback component ratio and the actual impedance presented to each amplifier input. For best high frequency performance, resistor values for feedback networks should be limited to a maximum of 5K ohms (preferably less than 1K ohm). Film type resistors are recommended. Power supply decoupling with ceramic capacitors from the device supply pins to ground is essential.

It is recommended that optimum circuit values for a particular application be developed through experimentation using amplifiers from several production runs. The PC artwork in the vicinity of the HA-5190 should be prototyped early to determine any sensitivites to layout.

OPERATION AT ELEVATED TEMPERATURES

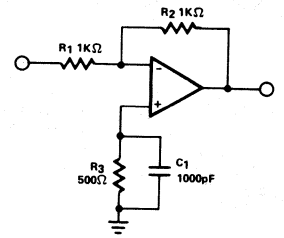
HA-5190/5195 may be used without a heat sink up to +75°C ambient. Above this temperature the power derating is 8.7mW/°C and a heat sink should be used. THERMALLOY model 6007 heat sink is recommended. For temperatures up to +125°C, the thermal resistance of the heat sink should be 30.6°C/W maximum.

FREQUENCY COMPENSATION

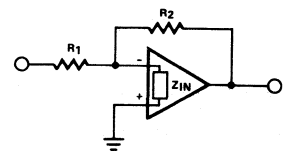
HA-5190/5195 is stable in standard DC amplifier configurations with closed loop gains exceeding +5 or -4. At these or higher gains, optimum AC performance can be achieved by keeping network resistor values as low as is practical.

Quite simple circuitry, as illustrated in Figure 3, gives excellent performance for lower closed loop gains. The compensation schemes use the amplifier's differential input impedance to reduce both the input and feedback signals thereby raising the effective noise gain approximately 14dB to a stable point on the frequency response curve.

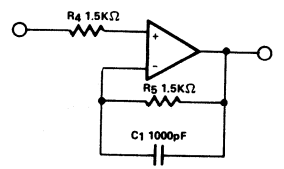
Inverting and non-inverting unity gain connections for HA-5190 are shown in Figure 3 (a) and (c). R_3 and R_5 serve only to balance DC voltage offsets due to input bias current, and may be replaced with a short for AC applications. C_1 is not neccessary for stability, but helps reduce overshoot and smooth the frequency response. Settling time or frequency response can be optimized (about 30mHz small signal bandwidth is practical) by fine tuning component values.



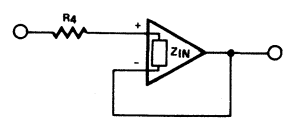
(a) Gain = -1



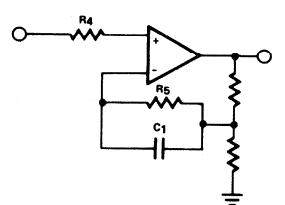
(b) Stabilization using Z_{IN}.



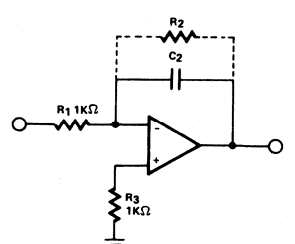
(c) Gain = +1



(d) Stabilization using Z_{IN}.



(e) Non-inverting gain stage.



(f) Integrator

Figure 3. Compensation recommended when $1 + \frac{R_2}{R_1} < 5$.

For closed loop gains between 1 and 5, reducing R_1 in Figure 3 (a) and (e) will raise the gain with minimum effect on bandwidth. However, in the inverting configuration, R_1 determines the input impedance, and it may be more practical to raise R_2 at the expense of bandwidth. In Figure 3 (e), R_4 and R_5 may be reduced as gain is increased and removed entirely at gains greater than +4.

For applications requiring 100% feedback at high frequencies, such as integrators and low pass filters, HA-5190/5195's compensation scheme should be thoroughly evaluated through experimentation. The circuit in Figure 3 (f) is quite stable, using the two 1K ohm resistors.

SUGGESTED METHODS FOR PERFORMANCE ENHANCEMENT

To avoid compromising AC performance, the HA-5190 design does not include provisions for internal offset adjustment.

The circuits in Figure 4 (a) and (b) show two possible schemes for offset voltage adjustment.

Figure 5 (a) and (b) uses the inherent qualities of the FET to reduce input bias currents by several orders of magnitude and raise input impedance to thousands of megohms. Both circuits are shown in the unity gain follower mode. Circuit gain can be implemented using normal feedback techniques. To optimize for speed, care should be taken in layout. Experimental results yielded slew rates of approximately 130V/μs.

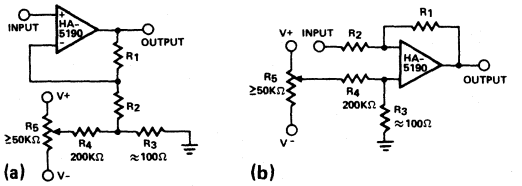
Figure 5 (c) illustrates a composite inverting amplifier which greatly reduces DC errors due to the HA-5190 input bias current and gain, while retaining superior settling time. The 0 dB frequency of the integrator section approximates the open loop low frequency pole (~2.5kHz) of the HA-5190. This circuit might also be connected as a current-to-voltage amplifier for use with a high accuracy, high speed DAC.

Figure 6 shows a composite amplifier scheme for boosting output current drive of the HA-5190/5195. The circuit gain (shown A_V = 5) can be adjusted using normal feedback systems. HA-5190 used in conjunction with HA-2630 can drive 50 ohm coaxial cable with 10 volt peak-to-peak signals at speeds up to 200V/μs.

APPLICATIONS

INTRODUCTION

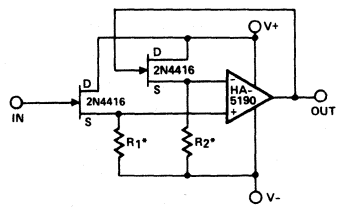
HA-5190/5195 represents an ideal building block for high speed, precision data acquisition systems and for video pulse amplification. Although this amplifier can be used in a wide variety of other applications, the ones to be discussed show where it can be used most advantageously.



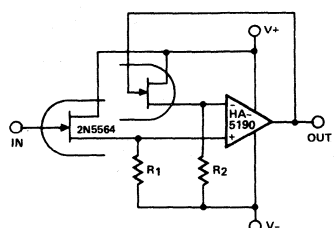
RANGE OF ADJUSTMENT FOR BOTH NON-INVERTING (LEFT) AND INVERTING AMPLIFIERS (RIGHT) DETERMINED BY PRODUCT OF V_{SUPPLY} AND R_3/R_4 RATIO.

$$A_V = 1 + \frac{R_1}{R_2 + R_3}$$

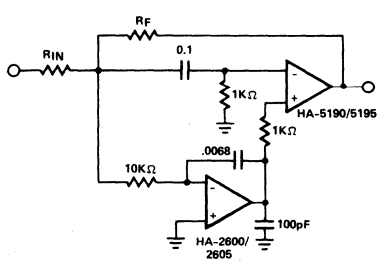
Figure 4. Offset Nulling.



(a) * VALUES SHOULD BE DETERMINED EXPERIMENTALLY FOR OPTIMIZED PERFORMANCE.



(b) R_1 AND $R_2 \approx 15K^*$
INPUT FETS ARE MATCHED PAIR 2N5564



(c)

Figure 5. Reducing Input Bias Currents.

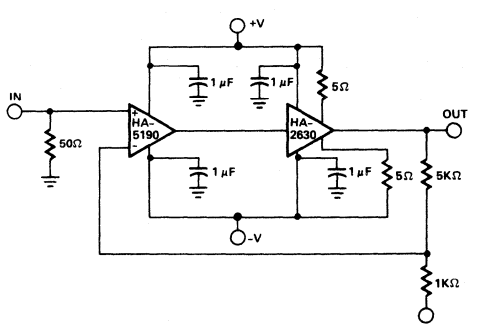


Figure 6. Boosting Output Current.

Application 1 Fast DAC Output Buffer

The circuit at right illustrates the HA-5190's usefulness as a high speed DAC buffer.

The amplifier operates as a current-to-voltage converter/output buffer to the HI-5610 which is a precision 10 bit DAC with output current settling time less than 100ns. The voltage divider on the non-inverting input serves to null any DC errors introduced into the system. The amplifier maximizes speed of the system since its dynamic performance exceeds that of the DAC.

Application 2 High Speed Sample/Hold

Sample/Hold circuits are used in many areas of data acquisition systems such as de-glitchers for D/A converters and input stages for successive approximation A/D converters.

The circuit at right uses the speed and drive capability of the HA-5190 coupled with two high speed DMOS FET switches.

The input amplifier is allowed to operate at a gain of -5 although the overall circuit gain is unity. Acquisition times of less than 100ns to 0.1% of a 1 volt input step are possible. Drift current can be appreciably reduced by using FET input buffers on the output stage of the Sample/Hold.

Application 3 Video Pulse Amplifier/75 ohm Coaxial Driver

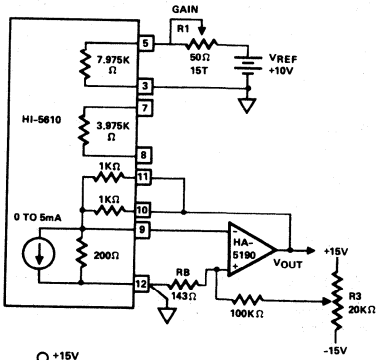
HA-5190/5195 is also well suited for video pulse applications. The circuit at right could be found in various types of video broadcasting equipment where 75 ohm systems are commonly employed.

HA-5190 can drive the 75 ohm coaxial cable with signals up to 2.5 volts peak-to-peak without the need for current boosting. In this circuit the overall gain of the circuit is approximately unity because of the impedance matching network.

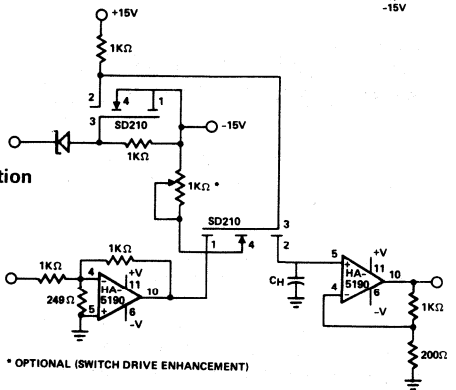
Application 4 Output Limiter

HA-5190 is rated for ± 5 volt output swing, and saturates at ± 7 volts. As with most op amps, recovery from output saturation is slow compared to the amplifier's normal response time; so some form of limiting, either of the input signal or in the feedback path, is desirable if saturation might occur. The circuit above illustrates a feedback limiter, where gain is reduced if the output exceeds ± (Vz + 2Vf). A 5 volt zener with a sharp knee characteristic is recommended.

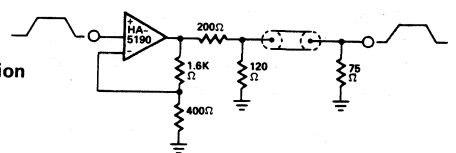
Application 1



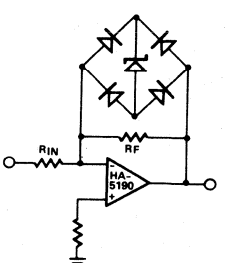
Application 2



Application 3



Application 4



HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

APPLICATION NOTE 607

DELTA MODULATION FOR VOICE TRANSMISSION

BY DON JONES

INTRODUCTION TO DELTAMOD

Delta modulation has evolved into a simple, efficient method of digitizing voice for secure, reliable communications and for voice I/O in data processing.

To illustrate basic principles, a very simple delta modulator and demodulator are illustrated in Figure 1. The modulator is a sampled data system employing a negative feedback loop. A comparator senses whether or not the instantaneous level of the analog voice input is greater or less than the feedback signal. The comparator output is clocked by a flip-flop to form a continuous NRZ digital data stream. This digital data is also integrated and fed back to the comparator. The feedback system is such that the integrator ramps up and down to produce a rough approximation of the input waveform. An identical integrator in the demodulator produces the same waveform, which when filtered, reproduces the voice.

We can see that the digital data 0's and 1's are commands to the integrators to "go up" or "go down" respectively. Another way of looking at it is that the digital data stream also has analog significance; it approximates the differential of the voice, since analog integration of the data reproduces the voice.

Note that the integrator output never stands still; it always travels either up or down by a fixed amount in any clock period. Because of its fixed integrator output slope, the simple delta modulator is less than ideal for encoding human voice which may have a wide dynamic amplitude range.

The integrator cannot track large, high frequency signals with its fixed slope. Fortunately, human speech has statistically smaller amplitudes at higher frequencies, and an integrator time constant of about 1 millisecond will satisfactorily reproduce voice in a 3kHz bandwidth.

A more serious limitation is that voice amplitude changes which are less than the heighth of the integrator ramp during one clock period cannot be resolved. So dynamic range is proportional to clock frequency, and satisfactory range cannot be obtained at desirable low clock rates.

A means of effectively increasing dynamic range is called "companding" (compressing-expanding); where at the modulator, small signals are given higher relative gain, and an inverse characteristic is produced at the demodulator.

The CVSD: A popular effective scheme for companded delta modulation is known as CVSD (continuously variable slope deltamod) shown in Figure 2. Additional digital logic, a second integrator, and an analog multiplier are added to the simple modulator.

Under small input signal conditions, the second integrator (known as the syllabic filter) has no input, and circuit function is identical to the simple modulator, except that the multiplier is biased to output quite small ramp amplitudes giving good resolution to the small signals.

A larger signal input is characterized by consecutive strings of 1's or 0's in the data as the integrator attempts to track the input. The logic input to the syllabic filter actuates whenever 3 or more consecutive 0's or 1's are present in the data. When this happens, the syllabic filter output starts to build up, increasing the multiplier gain, passing larger amplitude ramps to the comparator, enabling the system to track the larger signal. Up to a limit, the more consecutive 1's or 0's generated, the larger the ramp amplitude. Since the larger signals increase the negative feedback of the modulator and the forward gain of the demodulator, companding takes place. By listening tests, the syllabic filter time constant of 4 to 10 milliseconds is generally considered optimum.

An outstanding characteristic of CVSD is its ability, with fairly simple circuitry, to transmit intelligible voice at relatively low data rates. Companded PCM, for telephone quality transmission, requires about 64K bits/sec data rate per channel. CVSD produces equal quality at 32K bits/sec. (However, at this rate it does not handle tone signals or phase encoded modern transmissions as well.)

CVSD is useful at even lower data rates. At 16K bits/sec the reconstructed voice is remarkably natural, but has a slightly "Fuzzy Edge". At 9.6K bits/sec intelligibility is still excellent, although the sound

is reminiscent of a damaged loudspeaker. Of course, very sophisticated speech compression techniques have been used to transmit speech at even lower data rates; but CVSD is an excellent compromise between circuit simplicity and bandwidth economy.

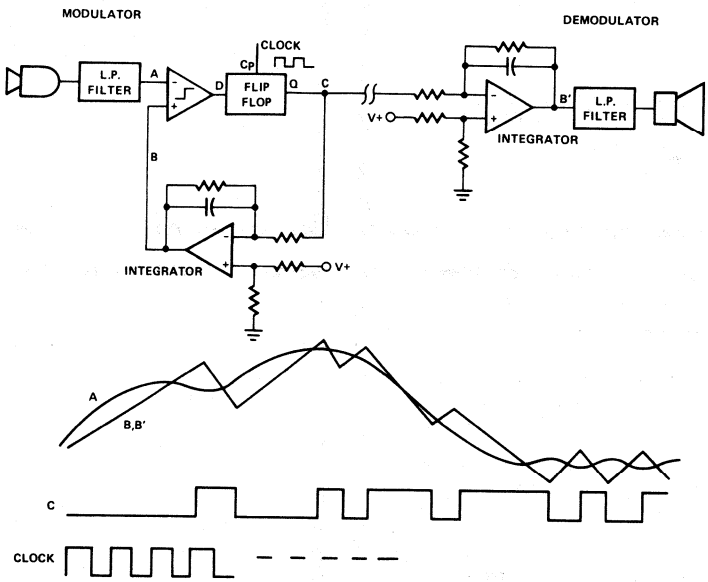


Figure 1 – Simple Delta Modulation

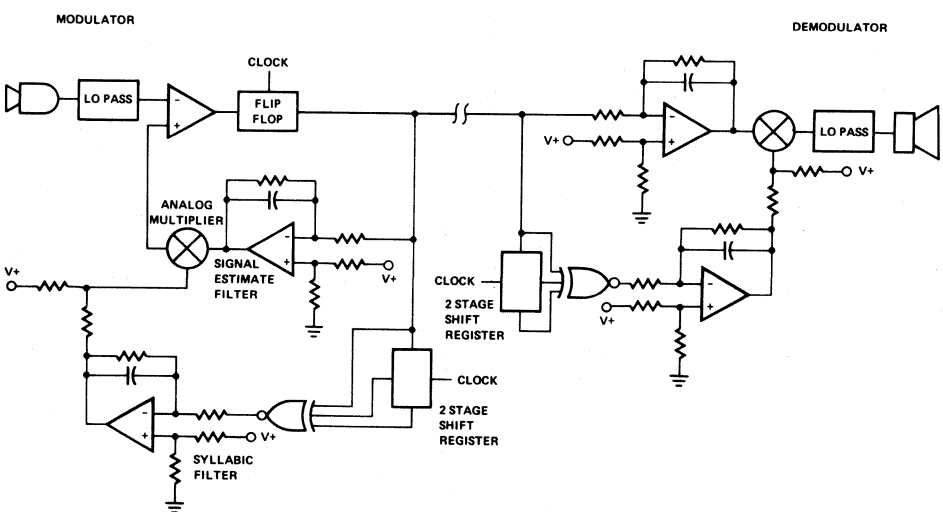


Figure 2 – Analog CVSD

THE DIGITAL CVSD

Delta modulated data is in a form which can be digitally filtered with fairly simple circuitry. A compatible CVSD can be made using digital integrators and multipliers driving a digital-to-analog converter. The block diagram of the Harris HC-55516/55532 monolithic CVSD is shown in Figure 3.

The CMOS digital circuit functions of Figure 3 closely parallel the equivalent analog function in Figure 2. The filters are single pole recursive types using shift registers with feedback. A digital multiplier feeds a 10 bit R-2R DAC which reconstructs the voice waveform. The DAC output is in steps, rather than ramps.

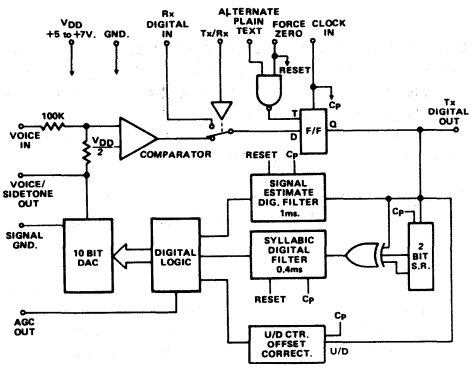


Figure 3 – HC-55516/55532 CVSD Functional Diagram

The digital CVSD has a number of advantages over its analog counterpart, and has desirable features which would otherwise require additional circuitry:

1) The all CMOS device requires only 1mA current from a single +4.5V to +7V supply.

2) No bulky external precision resistors or capacitors are required for the integrators; time constants of the digital filters are set by the clock frequency and do not drift with time or temperature.

3) For best intelligibility and freedom from listener fatigue, it is important that the recovered audio is quiet during the pauses between spoken words. During quiet periods, an alternate "1", "0" pattern should be encoded, which when decoded and filtered will be inaudible. Achieving this in the analog CVSD requires that up and down ramp slopes are precisely equal and that offsets in the comparator and amplifiers are adjusted to zero. Improper adjustment or excessive component drift can result in noisy oscillations. In the digital design, comparator offset and drift are adjusted by a long up-down counter summed to the DAC to insure that over a period of time equal numbers of 1's and 0's are generated.

   An added feature is automatic quieting, where if the DAC input would be less than 2 LSB's the quieting pattern is generated instead. This has proven to aid intelligibility.

4) To prevent momentary overload when beginning to encode or decode, it is desirable to initialize the integrators. In the analog CVSD, external analog switches would be required to discharge the capacitors.

   In the digital CVSD, the filters are reset by momentarily putting the "Force Zero" pin low. At the same time, a quieting pattern is generated without affecting internal encoding by putting the "Alternate Plain Text" pin low.

5) In some analog CVSD designs, transient noise will be generated during recovery from a low frequency overdriven input condition. The digital CVSD has a clipped output with instant recovery, when overdriven.

6) Half-duplex operation (using the same device, switching between the encode and decode functions) requires external circuits with the analog CVSD, while the digital type is switched internally by a logic input.

A possible drawback to the digital CVSD is that, since its filter time constants are proportional to the clock period, a single device will not be optimum for all clock frequencies. For this reason, Harris has two devices, the HC-55516 for clock rates below 24K bits/sec, and the HC-55532 for higher clock rates.

APPLICATIONS OF DELTA MODULATION

1) **Telecommunications:** Digitized signals are easily routed and multiplexed with low cost digital gates. Voice channels may be easily added to existing multiplexed digital data transmission systems. The digital signals are much more immune to crosstalk and noise when transmitted over long distances by wire, R.F., or optical paths. CVSD has better intelligibility than PCM when random bit errors are introduced during transmission.

2) **Secure Communications:** Digital data can be quite securely encrypted using fairly simple standard hardware (Figure 4a). Scrambled speech for audio channels may also be accomplished by encoding into a shift register, then selecting different segments of the shifted data in pseudo-random fashion and decoding it (Figure 4b).

3) **Audio Delay Lines:** Although charge-coupled deviced (CCD) will perform this function, they are still expensive and choice of configurations is quite limited. Also, there is a practical limit

to the number of CCD stages, since each introduces a slight degradation to the signal.

As shown in Figure 5, the delay line consists of a CVSD modulator, a shift register and a demodulator. Delay is proportional to the number of register stages divided by the clock frequency. This can be used in speech scrambling, as explained above, echo supression in PA systems; special echo effects; music enhancement or synthesis; and recursive or nonrecursive filtering.

4) **Voice I/O:** Digitized speech can be entered into a computer for storage, voice identification, or word recognition. Words stored in ROM's, disc memory, etc. can be used for voice output. CVSD, since it can operate at low data rates, is more efficient in storage requirements than PCM or other A to D conversions. Also, the data is in a useful form for filtering or other processing.

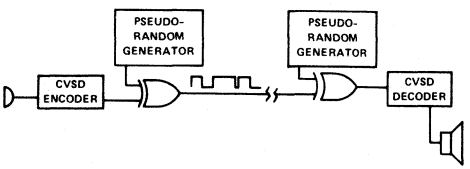


Figure 4a – Digital Transmission Encription

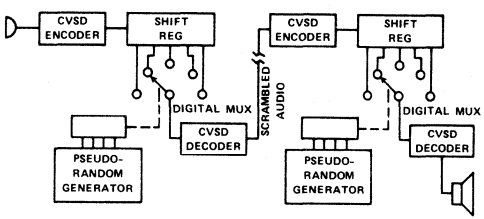


Figure 4b – Voice Transmission Scrambling

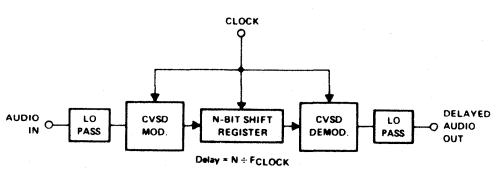


Figure 5 – Audio Delay Line

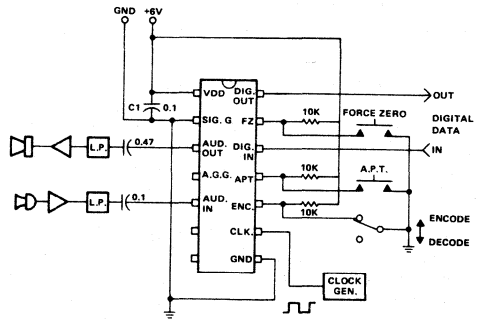


Figure 6 – CVSD Hookup for Evaluation

Figure 6 illustrates a simple evaluation breadboard circuit for the HC-55516/55532. A single device is sufficient to evaluate sound quality, etc. since, when encoding, the feedback signal at pin 3 is identical to the decoded signal from a receiver. The following are some pointers for using the devices:

1) Power supply decoupling is essential with the capacitor (C1 in Figure 6) located close to the I.C.

2) Power to the I.C. must be present before the audio input, the clock, or other digital inputs are applied. Failure to observe this may result in a latchup condition, which is usually not destructive and may be removed by cycling the supply off, then on.

3) Signal ground (pin 2) should be externally connected to pin 8 and power ground. It is recommended for noise-free operation that the audio input and output ground returns connect directly to pin 2 and to no other grounds in the system. Pins 6 and 7 must be open circuited.

4) Digital inputs and outputs are similar to and compatible with standard CMOS logic circuits using the same supply voltage. The illustrated 10K pullup resistors are necessary only with mechanical switches, and are not necessary when driving these pins with CMOS. Unused digital inputs should be tied to the appropriate supply rail for the desired operation. TTL output, however, will require pullup resistors (about 1K) to obtain the required CMOS input levels. Pins 4 and 14 will drive CMOS logic, or each can drive one low power TTL input.

5) Capacitor coupling is recommended for the audio in and out (pins 3 and 5) as each pin is internally biased to about 1/2 the supply voltage.

6) The AGC output (pin 4) is a digital output, whose duty cycle is dependent on the average audio level. This may be externally integrated to drive an AGC preamplifier; or it could be used (through a buffer gate) to drive an LED indicator to indicate proper speaking volume.

7) To prevent generation of alias frequencies, the input filter should reduce the audio amplitude at frequencies greater than half the clock rate to less than 12 millivolts peak-to-peak.

8) The complex output filter shown on the data sheet is necessary only when measuring signal to noise ratios where all frequencies above 3kHz must be removed. Generally a 2 or 3 pole filter is sufficient for acceptable voice quality.

9) A suggested receiver clock circuit is a free running multivibrator, synchronized at each transition of the incoming data. Any synch errors occurring during reception of long strings of zeros or ones will have negligible effect on the decoded voice.

Figures 7 though 11 illustrate some typical audio output (before filtering) and digital output waveforms. To make the scope picture stationary, the audio input generator was synchronized with a submultiple of the clock frequency.

Figure 7 shows the results of a large low frequency sine wave. The somewhat jagged peaks are typical of all CVSD systems. Note that the digital output is continuous "ones" while the waveform is slewing down and continuous "zeros" while slewing up.

Figure 8 shows the excellent recovery from overdriven conditions at low frequency. Some analog type CVSD's have trouble recovering from this condition.

As mentioned previously, CVSD's cannot handle large signals at high frequencies (but these are not generally present in the human voice). Figure 9 shows this limitation where the voice output is slewing at its maximum rate, but cannot catch up with the input. At reduced amplitudes, however, the same signal can be reproduced, as shown in Figure 10.

The transfer function curve on the data sheet shows that at 16kHz clock rate, a 1.4V RMS signal can be tracked up to 500Hz. With a 32kHz clock, the same curves may be used, but with each of the indicated frequencies doubled. Likewise, each of the SNR figures shown on the data sheet will be 6dB better with a 32kHz clock.

Figure 11 shows the 12 millivolt voice output waveform at 1/2 the clock rate, when there is no audio input. After filtering, this signal is inaudible.

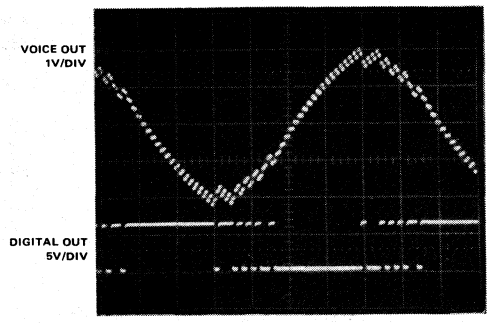


Figure 7 – CVSD Large Signal Sine Wave Reconstruction

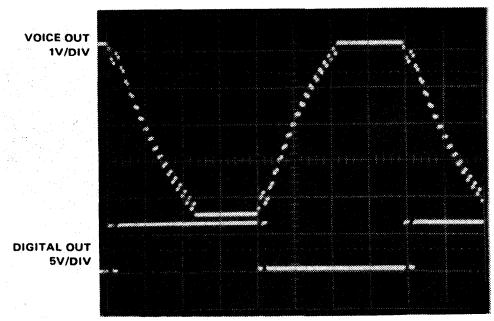


Figure 8 – CVSD Large Signal, Low Frequency Clipped Waveform

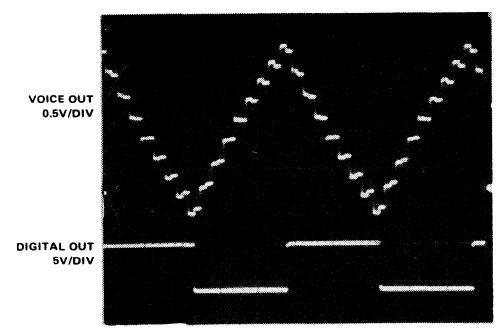
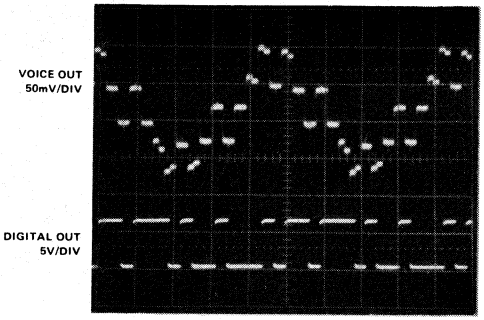
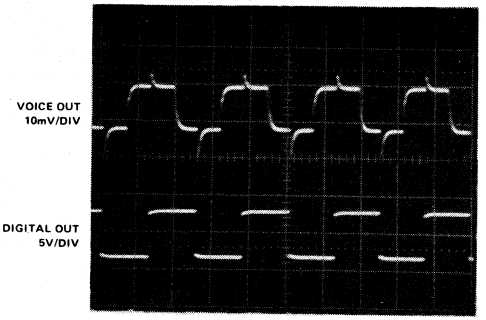


Figure 9 – CVSD Large Signal, High Frequency Slew Limiting



0.2ms/DIV.
VOICE IN = 1kHz, 0.15V P-P SINE WAVE
CLOCK = 16kHz

Figure 10 – CVSD Small Signal Sine Wave Reconstruction



50μs/DIV.
VOICE IN = 0
CLOCK = 16kHz

Figure 11 – CVSD Zero Signal Idle Pattern

Chip Information

GENERAL INFORMATION

Most of the Harris Analog standard products are available in chip form to the hybrid micro circuit designer. The standard chips are DC electrically tested at +25°C to the data sheet limits for the commercial device and are 100% visually inspected to MIL-STD-883, Method 2010, Condition B criteria. Packaging for shipments consists of waffle pack carriers plus an anti-static cushioning strip for extra protection.

Certain products are also available with guaranteed performance specified over an extended temperature range. Harris also has several options additional to standard chip processing available upon request at extra cost. These include: gold backing, SEM, class A visual.

All specifications in this book are applicable only to packaged products. Specifications for dice are obtained in Harris Semiconductor's Analog Chip Data Book or from the factory or authorized sales representatives.

CHIP DATA BOOK

Harris Semiconductor publishes a data book which provides ordering, processing and performance specifications for various Analog products in dice form. This data book is reprinted for your information and convenience starting on page 7-9. Individual copies of the chip brochure are available from the factory and your local Harris sales office.

CHIP ORDERING INFORMATION

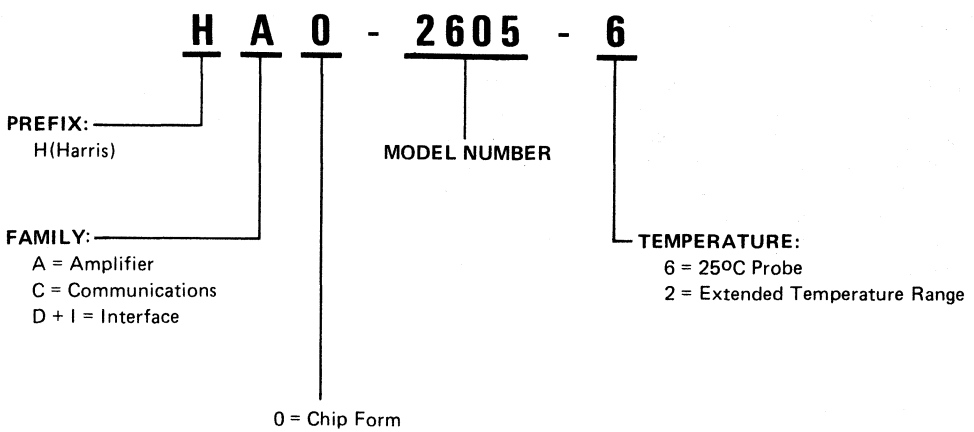
Standard and special chip sales are direct factory order only. The minimum order on all sales is $250.00 per line item. Contact the local Harris Sales Office or Representative for pricing and delivery on special chip requirements.

MECHANICAL INFORMATION

Dimensions: All chip dimensions nominal with a tolerance of ±.003". Maximum chip thickness is .012".

Bonding Pads: Minimum bonding pad size is .004" x .004" unless otherwise specified.

PRODUCT CODE EXAMPLE



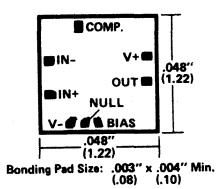
NOTE: Certain performance guaranteed over -55°C to +125°C or 0°C to +125°C depending on product. Consult general information statement on page 7-1.

Chip Geometries

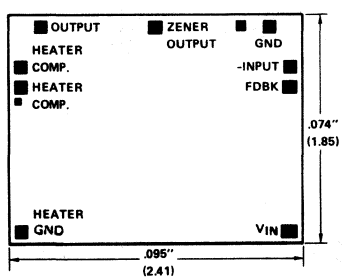
1. All dimensions in inches, millimeters are shown in parentheses.
2. Unless otherwise specified, minimum bonding pad size for all devices is .004" x .004" (.10mm x .10mm).

OPERATIONAL AMPLIFIERS & COMPARATORS

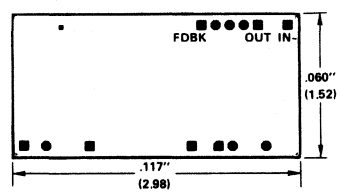
HA0-909/911



HA0-1600/02/05



HA0-1610/15



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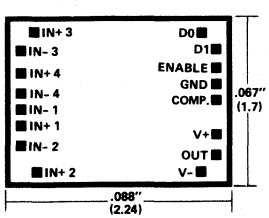

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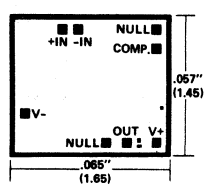

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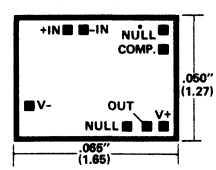

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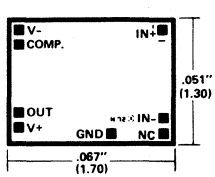

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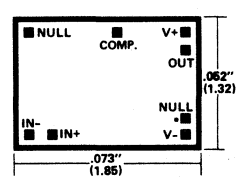

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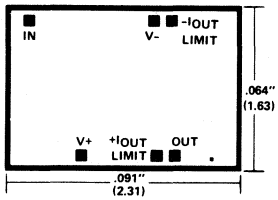

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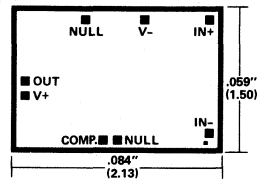

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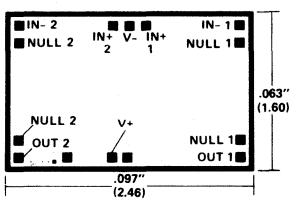

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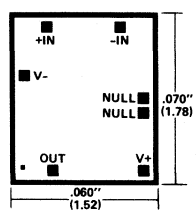

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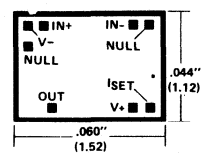

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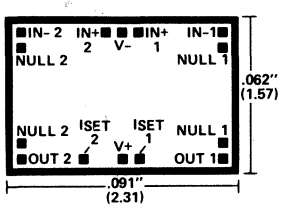

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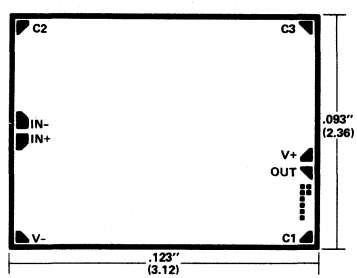

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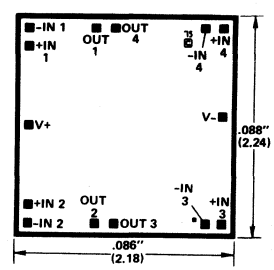

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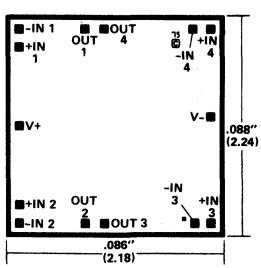

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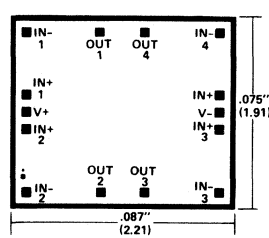

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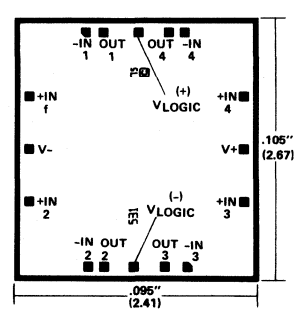

OPERATIONAL AMPLIFIERS & COMPARATORS

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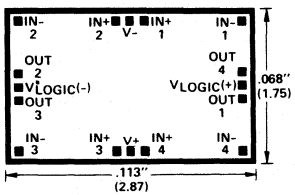

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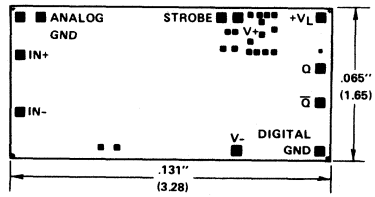

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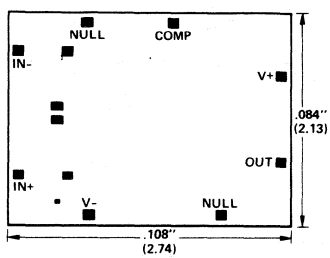

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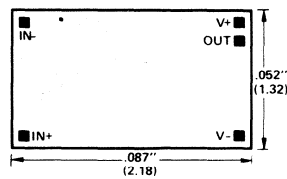

CMOS ANALOG SWITCHES & MULTIPLEXERS

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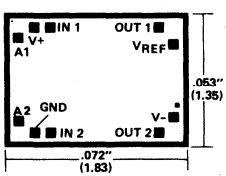

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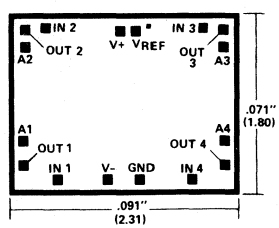

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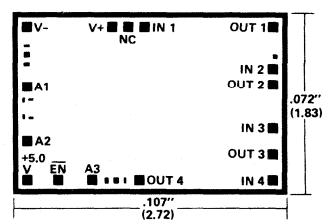

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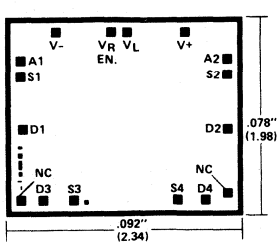

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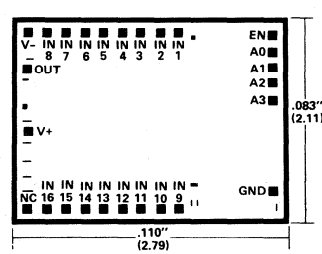

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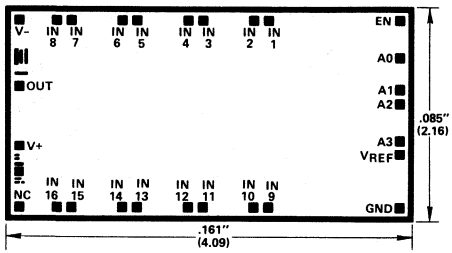

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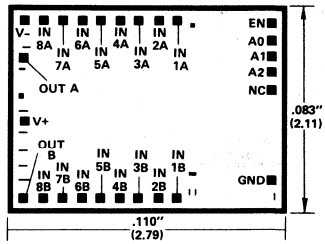

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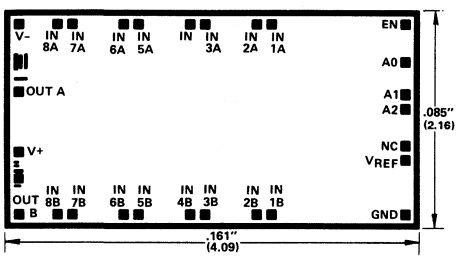

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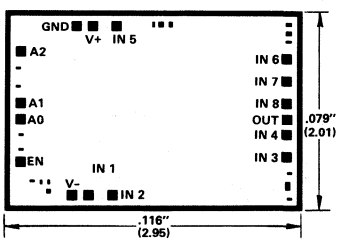

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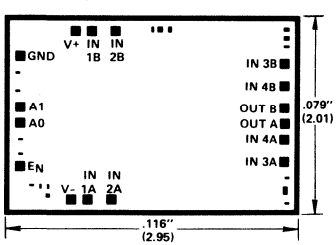

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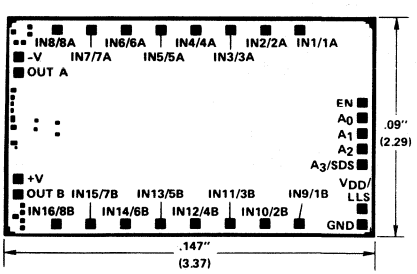

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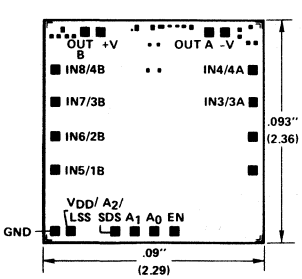

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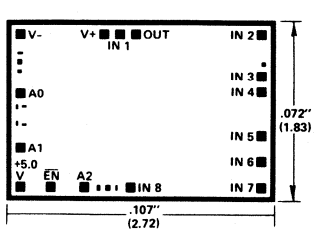

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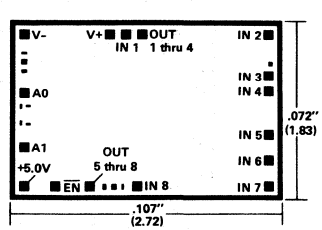

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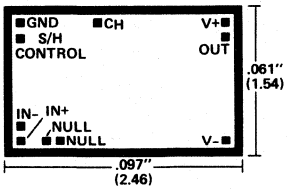

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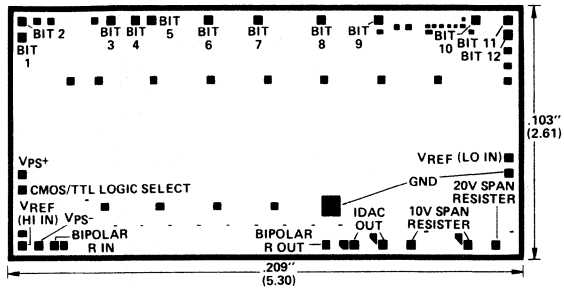

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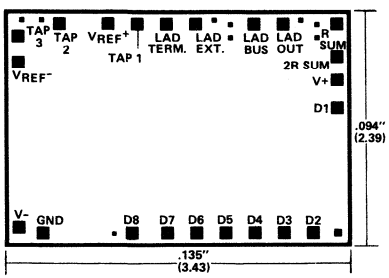

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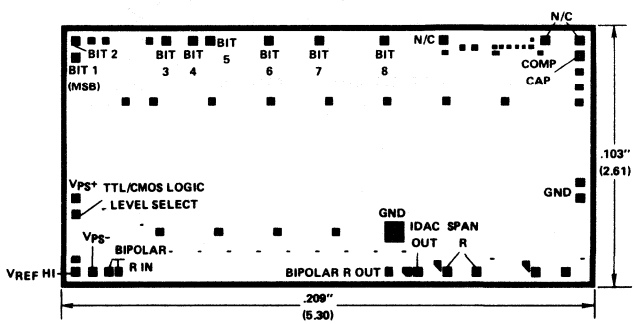

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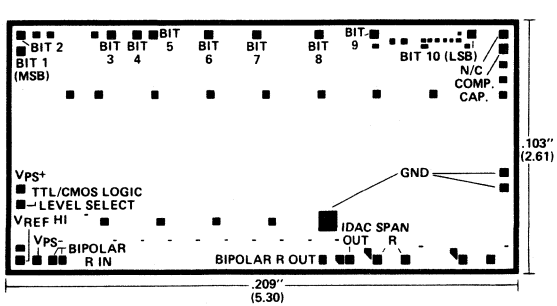

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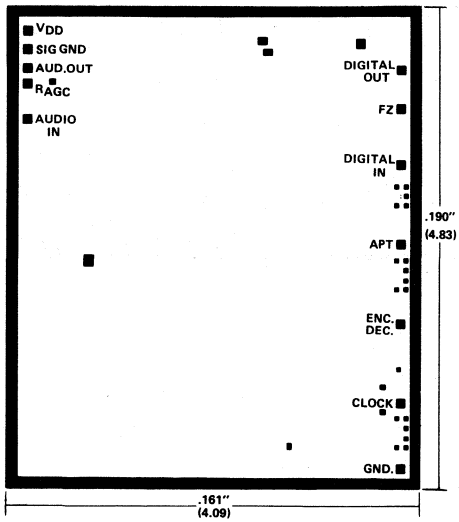

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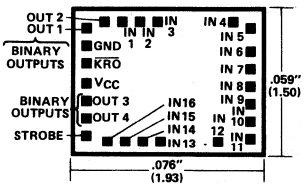

7

Analog Chip Data Book

Harris Semiconductor Analog Integrated Circuits represent the state-of-the-art in linear and data acquisition components. This book presents those integrated circuits that are available as a standard product in chip form. These chips offer precision, reliability, and performance comparable to that of Harris' packaged parts.

The introductory section of this book provides information on product assurance, testing, recommended handling, and ordering information. The characteristics section provides the DC and AC specifications, chip layout, and a functional layout where required.

If you need more information on these or other Harris products, please contact the nearest Harris sales office listed in the back of this chip data book.

Harris Semiconductor's products are sold by description only. Harris reserves the right to make changes in circuit design, specifications and other information at any time without prior notice. Accordingly, the reader is cautioned to verify that data sheets and other information in this publication are current before placing orders. Use of the information for user's specific application is at user's risk.

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Printed in USA

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(continued)

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Data Conversion Products

Communications Products

Chip Geometries

7

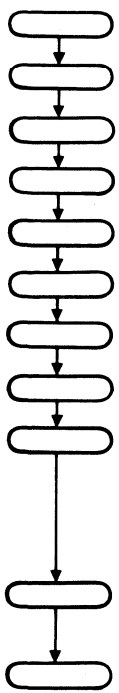
Product Assurance at Harris

Our Product Assurance Department strives to ensure that the dice shipped to our customers are reliable, of a high quality level, and consistent with customer requirements. During product processing there are several independent visual and electrical checks performed by Quality Assurance personnel based on various process and control documents. This ensures that the dice meet the specifications controlling fabrication and workmanship, thus enhancing the quality and reliability of the product.

A final inspection prior to shipment is performed at Quality Assurance Plant Clearance to ensure that all requirements of the purchase order and customer specifications are met. The systems procedures implemented are based on MIL-M-38510, MIL-STD-883, and MIL-C-45662.

Standard Chip Processing

Harris maintains the same processing and control requirements for chips destined for dice sales as for those assembled in packages. This ensures the continued reliability and high performance of Harris chips. The following diagram shows the processing steps for chips once the wafer has been processed.



Wafer Processing

100% Wafer Probe for DC characteristics at specified temperatures

In-Process Sample Inspection

Scribe and Break

Die Sort

Die Clean

100% Visual

Dice to Q.A. For acceptance

Q.A. Sample Inspection
- Acceptance Visual Test to LTPD of 15%
- Physical Quantity
- Confirmation of Product
- Documentation

Q.A. Plant Clearance – Final inspection of packaging, quantity, marking per customer requirements

Shipping

Product Testing

All chips offered in the data book are 100% visually screened to meet the criteria of MIL-STD-883, Method 2010.3, Test Condition B. This is the standard visual test for all chips available from the data book. As an option for all chips, Harris also offers visual testing in compliance with MIL-STD-883, Method 2010.3, Test Condition A. The factory should be consulted to determine the additional charges involved for a particular order requiring Condition A visual inspection.

Most of the chips produced by Harris are available in both a commercial and a military grade. Consult the specific data sheet to determine which grades are available for a particular chip. The following electrical tests are applicable to commercial (-6) chips:

1. Chips are 100% probe tested at 25°C to guarantee the maximum/minimum DC characteristics listed in the data sheets at 25°C.

2. For AC characteristics where a minimum or maximum is shown, the specifications are guaranteed at 25°C although the chips are not probed for AC. For those AC characteristics where only typicals are given, the values are for design aid only and are neither tested nor guaranteed.

3. The DC and AC characteristics are guaranteed to the following LTPD's at 25°C:

   a. Chips will meet an LTPD of 20/2 for DC characteristics.

   b. Chips will meet an LTPD fo 20/3 for AC characteristics.

The following electrical tests are applicable to military (-2) chips:

1. Chips are 100% probe tested to guarantee the maximum/minimum DC characteristics listed in the data sheets. The DC characteristics are guaranteed over the temperature range shown in the individual data sheets, although the chips are not necessarily probed at the temperature limits. Characteristics for -2 parts are guaranteed from -55°C to +125°C, or from 0°C to +125°C depending on type of device (see individual data sheets).

   Some DC characteristics are guaranteed only at 25°C and not over the full temperature range, as indicated in the data sheets. For those DC characteristics where only typicals are given, the values are for design aid only and are not tested or guaranteed.

2. For AC characteristics where a minimum or maximum is shown, the specifications are guaranteed at 25°C although the chips are not probed for AC. For those AC characteristics where only typicals are given, the values are for design aid only and are neither tested nor guaranteed.

3. The DC and AC characteristics are guaranteed to the following LTPD's (where applicable):

   a. Chips will meet an LTPD of 20/2 for DC characteristics at 25°C.

   b. Chips will meet an LTPD of 20/3 for DC characteristics at +125°C.

   c. Chips will meet an LTPD of 20/3 for DC characteristics at -55°C. (Only where specified)

   d. Chips will meet an LTPD of 20/3 for AC characteristics at 25°C

To assure that the DC and AC specifications are being consistently met, the chips are sampled systematically by Quality Assurance. The dice are assembled in standard packages and tested at the appropriate temperatures to the LTPD's stated above.

Lot acceptance send ahead testing for DC and AC specifications is available as an option at an additional charge when ordering chips. Sample dice are assembled in a standard package and tested to the indicated LTPD's. Consult the factory when placing an order requiring lot acceptance send ahead test data.

Quality Assurance also systematically samples wafer lots using a Scanning Electron Microscope (SEM) for inspection of the metallization. This test is available as an option at an additional charge for most orders. Please consult the factory for additional information.

NOTE 1 – Explanation of Grades:

Military chips are 100% probe tested to guarantee the maximum/minimum DC specifications over the temperature range indicated. The temperature range for (-2) dice is -55°C to +125°C, or 0°C to +125°C depending on type of device. Dice are not necessarily probed at the temperature limits but the DC characteristics are guaranteed over the applicable temperature range.

Commercial (-6) are 100% probe tested at 25°C to guaranteed the maximum/minimum DC characteristics at 25°C.

Mechanical Information

Dimensions: All chip dimensions given in the layouts in the data sheet section are nominal with a tolerance of ±.003 inches (±.08mm). Die thickness is nominally .011 inches ±.002 inches (.28mm ±.05mm).

Bonding Pads: Minimum bonding pad size is .004 x .004 inches (.10mm x.10mm).

Passivation

All Harris dice are passivated with a layer of protective dielectric material to guard against deterioration of the dice. Passivation is applied to all areas of the die except the bonding pads and scribe lines.

Storage

Harris stores its dice in a dry nitrogen atmosphere and recommends that the customer do the same. If dice are exposed to air the aluminum metallization will slowly oxidize at the bonding pads. The aluminum oxide will make bonding more difficult, especially if thermal compression gold ball bonding is used.

The humidity should be kept as low as possible with a relative humidity of no more than 50%.

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Shipping

Dice are placed in conductive waffle carriers and covered with a layer of bibilious paper and with a layer of mylar. The waffle pack is then sealed and labeled. The label contains the part number of the chips, the quantity, and the lot number. The waffle pack is placed in a polyethelene bag along with a humidity indicating desiccant. The bag is then heat sealed and packaged in a suitable shipping container.

Recommended Handling

It is suggested that all dice be handled, tested, and installed using standard MOS handling techniques. This includes the use of conductive carriers and grounding of equipment and personnel. It has been found that handling equipment and personnel can generate static potentials in excess of 10kV in a low humidity environment. Therefore, proper handling procedures must be adopted to reduce static charge. Harris recommends using the following procedures when handling dice:

1. Use conductive work stations. Metallic or conductive plastic* tops on work benches connected to ground help eliminate static build-up.

   *Such as 3M "Velostat"

2. Ground all handling equipment. To prevent scratches, it is recommended that a vacuum pick-up with protected tip be used for handling the dice. If tweezers are used, the dice should be gripped only on its sides.

3. Ground all handling personnel with a conductive bracelet through a 1M ohm resistor to ground. The resistor will prevent electroshock to personnel.

4. Smocks, clothing, and especially shoes of certain insulating materials (notably nylon) should not be worn in areas where devices are handled. These materials, highly dielectric in nature, will hold or aid in the generation of a static charge. Instead, natural materials such as cotton should be used to minimize charge generation.

5. Ionized air blowers reduce charge build-up in areas where grounding is not possible or desirable.

6. Devices should be in conductive carriers during all phases of transport.

Recommended Die Attachment

Harris uses gold eutectic die-attach for its packaged circuits and recommends this procedure for use with its chips. The die-attach area of the package should be gold plated. Gold preforms are usually not required. The recommended temperature for die-attachment is 420°C ±10°C and should remain constant throughout the procedure. To prevent oxidation a laminar flow of nitrogen should be provided over the chip sufrace of approximately 30 liters/hour.

The package should be placed on the heater block and allowed to arrive at a uniform temperature. With tweezers, the die should be picked up and placed on the package. Using an orbital motion, the die should be rubbed on the package until eutectic melt is visible along the entire periphery of the die. There should be no evidence of balling or flaking of die-attach material. The die should be level with respect to the package and the die-attach material should be no higher than the top edges of the die.

Although Harris recommends using gold eutectic die-attach, conductive epoxy die-attach may also be used. Specific directions depend upon the epoxy used.

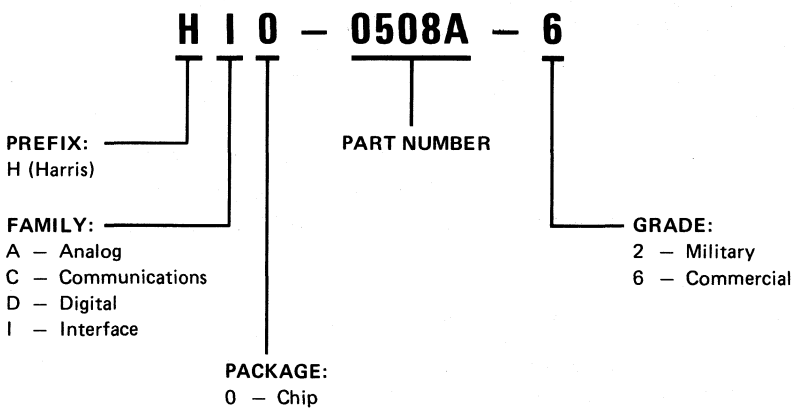
Recommended Bonding Procedures

Harris uses ultrasonic aluminum wire bonding and recommends this procedure be used by our customers for best results. Harris uses an aluminum-silicon alloy wire, 99% aluminum and 1% silicon. The diameter is 0.00125 inches, tensile strength is 22 ±2g, and elongation is 1.0 to 4.5%. Harris recommends similar wire be used by the customer. Actual bonding procedure will be governed by the manufacturer's instructions for the particular bonding equipment being used. A minimum bond pull strength of 3g is recommended to assure mechanical bond quality.

Ordering Information

Harris chips are designated by a Product Code. When ordering standard chips from this data book, please refer to the chips by the full product code. Harris chip codes will always begin with an H. Specific device numbers will always be isolated by hyphens.

Chip Code Example



Specifications are not included in this data book for the parts listed below. For information on the availability and specifications of these products in chip form consult a Harris salesman or Representative or call the factory.

HA-911	HA-4905
HA-2535	HA-5105
HA-2635	HA-5115
HA-2645	HA-5195

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Chips are generally available on new Harris IC's at the time of introduction. Consult a salesman, representative or the factory regarding availability and specifications.

Options Available

1. Visual testing in compliance with MIL-STD-883, Method 2010.1, Test Condition A is available as an option for most chips (military grade only). Consult the factory to determine the additional charges involved and the availability of this option.

2. Lot acceptance send ahead testing is available an an option for most chips. Consult the factory to determine the additional charges involved and the availability of this option.

3. Scanning Electron Microscope (SEM) inspection is also available as an option. Consult the factory regarding this option.

4. Gold backing is available for those chips for which it is not a standard feature. The specification page for each chip indicates whether or not gold backing is standard. If gold backing is required, consult the factory for specific ordering information and pricing.

Special Orders

For best availability and price, it is urged that standard chips as specified in this data book be orderd. If additional electrical specification guarantees or reliability screening are absolutely required, a Request for Quotation and Source Control Drawing should be submitted through the local Harris Sales Office or Sales Representative.

Harris reserves the right to decline to quote, or to request modification to special screening requirements.

Return Policy

After customer receipt of the dice, Harris recommends that the customer first perform a visual inspection of the dice. Harris guarantees that the dice will pass the visual inspection based upon the appropriate MIL-STD-883 Condition (A or B) and the specified LTPD limits. Customer inspection must be performed at the power of magnification indicated in the MIL specification.

If the lot fails visual inspection, the containers should be closed and the entire lot must be returned to Harris. If the visual inspection is acceptable, samples should be taken for the electrical testing of the DC and AC parameters. If the sample fails the electrical test based on the specified LTPD, then the entire lot must be returned to Harris. A detailed inspection report must accompany all returns. Harris will accept dice returns only when the entire lot is returned in its original container. The sample dice should be packaged separately and identified by the customer. Harris will not accept rejected dice from a lot that has been inspected 100% by the customer.

To return dice, the customer should first contact the field salesmen for instructions. Once approved, the customer will be sent a Material Return Authorization (MRA). The material can then be returned to Harris Receiving with the appropriate copies of the MRA attached to the outside of the package.

Leadless Chip Carriers

Most of our devices will be offered in leadless chip carriers. These packages provide an alternative to conventional chip-and-wire hybrids with many significant advantages. The important characteristics of leadless chip carrier technology include the following:

- High Functional Density
- Hermetic Package for Each Die
- Full AC/DC and Temperature Testing at the Die Level
- Die Level Burn-In Capability
- Compatibility with Automatic Handling Equipment
- Compatible with Reflow Solder Techniques, Resulting in Simple Reworks and High-Yield, Low Cost Assemblies

Consult the factory for additional information.

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
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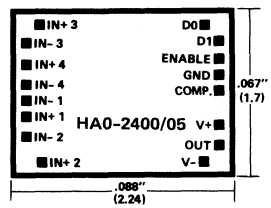
HA0-2400/2405

PRAM Four Channel Programmable Amplifier

Description

HA0-2400 and HA0-2405 are four-channel programmable amplifiers providing a level of versatility unsurpassed by any other monolithic operational amplifier. Versatility is achieved by employing four input amplifier channels, any one (or none) of which may be electrically selected and connected to a single output stage through DTL/TTL compatible address inputs. The device formed by the output and the selected input is an op amp which delivers excellent slew rate, gain bandwidth, and power bandwidth performance. Other advantages of these dielectrically isolated amplifiers include high voltage gain and high input impedance coupled with low input offset voltage and low offset current.

Chip Layout and Dimensions



For Chip Geometries see Drawing 1, page 7-49.

Specifications

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Pads	45.0V	Operating Temperature Range	
Differential Input Voltage	$\pm V_{SUPPLY}$	HA0-2400-2	$-55^oC \leq T_A \leq +125^oC$
Digital Input Voltage	-0.76V to 10.0V	HA0-2405-5	$0^oC \leq T_A \leq +75^oC$
Output Current	Short Circuit Protected	Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$

ELECTRICAL SPECIFICATIONS

	PARAMETER	TEMPERATURE	HA0-2400-2 MINIMUM	HA0-2400-2 MAXIMUM	HA0-2405-6 MINIMUM	HA0-2405-6 MAXIMUM	UNITS
GUARANTEED CHARACTERISTICS Unless otherwise specified, Supplies = +15V, -15V; V_{IL} = +0.5V, V_{IH} = +2.4V(Limits apply to each of the four channels, when addressed).	INPUT CHARACTERISTICS						
	Offset Voltage	+25°C		5		9	mV
		0°C to +125°C		7			mV
	Bias Current (12)	+25°C		200		250	nA
		0°C to +125°C		400			nA
	Offset Current (12)	+25°C		50		50	nA
		0°C to +125°C		100			nA
	Common Mode Range	+25°C	±10.0		±10.0		V
		0°C to +125°C	±10.0				V
	TRANSFER CHARACTERISTICS						
	Large Signal Voltage Gain (1, 5)	+25°C	50k		50k		V/V
		0°C to +125°C	25k				V/V
	Common Mode Rejection Ratio (2)	+25°C	80		74		dB
		0°C to +125°C	80				dB
	OUTPUT CHARACTERISTICS						
	Output Voltage Swing (1)	+25°C	±10.0		±10.0		V
		0°C to +125°C	±10.0				V
	POWER SUPPLY CHARACTERISTICS						
	Supply Current	+25°C		6.0		6.0	mA
	Power Supply Rejection Ratio (11)	+25°C	74		74		dB
		0°C to +125°C	74				dB
TYPICAL CHARACTERISTICS	Input Resistance	+25°C	30		30		MΩ
	Gain Bandwidth Product (3)	+25°C	40		40		MHz
	(4)	+25°C	8		8		MHz
	Output Current	+25°C	20		20		mA
	Full Power Bandwidth (3, 5)	+25°C	500		500		kHz
	(4, 5)	+25°C	200		200		kHz
	Rise Time (4, 6)	+25°C	20		20		ns
	Overshoot (4, 6)	+25°C	25		25		%
	Slew Rate (3, 7)	+25°C	30		30		V/μs
	(4, 7)	+25°C	8		8		V/μs
	Settling Time (4, 7, 8)	+25°C	1.5		1.5		μs
	Digital Input Current (V_{IN} = 0V)	+25°C	1		1		mA
	(V_{IN} = +5.0V)	+25°C	5		5		nA
	Output Delay (9)	+25°C	100		100		ns
	Crosstalk (10)	+25°C	90		90		dB

NOTES:
1. $R_L = 2k\Omega$.
2. $V_{CM} = \pm 5VDC$.
3. $A_V = +10$, $C_{COMP} = 0$, $R_L = 2k\Omega$, $C_L = 50pF$.
4. $A_V = +1$, $C_{COMP} = 15pF$, $R_L = 2k\Omega$, $C_L = 50pF$.
5. V_{OUT} = 20V peak to peak.
6. V_{OUT} = 200 mV peak to peak.
7. V_{OUT} = 10.0V peak to peak.
8. To 0.1% of final value.
9. To 10% of final value; output then slews at normal rate to final value.
10. Unselected input to output, $V_{IN} = \pm 10VDC$.
11. $V_{SUPPLY} = \pm 10VDC$ to $\pm 20VDC$.
12. Unselected channels have approx. the same input parameters.

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
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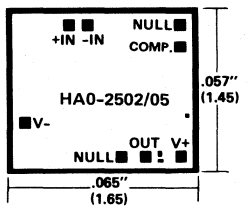
HA0-2502/2505

Precision High Slew Rate Operational Amplifier

Description

HA0-2502 and HA0-2505 are monolithic operational amplifiers whose designs are optimized to deliver excellent slew rate, bandwidth, and settling time specifications. Typical specifications include a slew rate of ±25V/μs, settling time of 330ns, power bandwidth of 500kHz, and gain bandwidth of 12MHz. These outstanding dynamic features of these internally compensated devices are complemented with a low offset voltage and low offset current. These dielectrically isolated amplifiers are ideally suited for applications such as data acquisition, R.F., video, and pulse conditioning circuits.

Chip Layout and Dimensions



For Chip Geometries see Drawing 2, page 7-49.

Specifications

ABSOLUTE MAXIMUM RATINGS T_A = +25°C unless otherwise stated.

Voltage Between V^+ and V^- Pads	40.0V	Operating Temp. Range HA0-2502-2	-55°C ≤ T_A ≤ +125°C
Differential Input Voltage	± 15.0V	HA0-2505-6	0°C ≤ T_A ≤ +75°C
Peak Output Current	50mA	Storage Temperature Range	-65°C ≤ T_A ≤ +150°C

ELECTRICAL SPECIFICATIONS

GUARANTEED CHARACTERISTICS V^+ = +15VDC, V^- = -15VDC

PARAMETER	TEMPERATURE	HA0-2502-2 MINIMUM	HA0-2502-2 MAXIMUM	HA0-2505-6 MINIMUM	HA0-2505-6 MAXIMUM	UNITS
INPUT CHARACTERISTICS						
Offset Voltage	+25°C		8		8	mV
	0°C to +125°C		10			mV
Bias Current	+25°C		250		250	nA
	0°C to +125°C		500			nA
Offset Current	+25°C		50		50	nA
	0°C to +125°C		100			nA
Common Mode Range	+25°C	± 10.0		± 10.0		V
	0°C to +125°C	± 10.0				V
TRANSFER CHARACTERISTICS						
Large Signal Voltage Gain (1, 4)	+25°C	15K		15K		V/V
	0°C to +125°C	10K				V/V
Common Mode Rejection Ratio (2)	+25°C	74		74		dB
	0°C to +125°C	74				dB
OUTPUT CHARACTERISTICS						
Output Voltage Swing (1)	+25°C	± 10.0		± 10.0		V
	0°C to +125°C	± 10.0				V
Output Current (4)	+25°C	± 10		± 10		mA
Full Power Bandwidth (4, 9)	+25°C	300				kHz
TRANSIENT RESPONSE						
Rise Time (1, 5, 6)	+25°C		50			ns
Overshoot (1, 5, 7)	+25°C		50			%
Slew Rate (1, 5)	+25°C	± 20				V/μs
POWER SUPPLY CHARACTERISTICS						
Supply Current	+25°C		6		6	mA
Power Supply Rejection Ratio (8)	+25°C	74		74		dB
	0°C to +125°C	74				dB

TYPICAL CHARACTERISTICS

Input Resistance	+25°C	50	50	MΩ
Gain Bandwidth Product (3)	+25°C	12	12	MHz
Full Power Bandwidth (4)	+25°C	500	500	kHz
Rise Time (1, 5, 6)	+25°C	25	25	ns
Overshoot (1, 5, 7)	+25°C	25	25	%
Slew Rate (1, 4, 5)	+25°C	± 30	± 30	V/μs
Settling Time to 0.1% (1, 4, 5)	+25°C	0.8	0.8	μs

NOTES:
1. R_L = 2k.
2. V_{CM} = ±10V.
3. A_V > 10.
4. V_O = ±10.0V.
5. C_L = 50pF.
6. V_O = ± 200mV.
7. V_O = ± 200mV.
8. ΔV = ± 5.0V.
9. Guaranteed based on $FPBW = \frac{\text{Slew Rate}}{2\pi T}$

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HARRIS SEMICONDUCTOR PRODUCTS DIVISION
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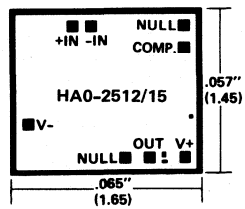
HA0-2512/2515

High Slew Rate Operational Amplifier

Description

HA0-2512 and HA0-2515 are high performance operational amplifiers designed to provide superior slew rate, settling time, and bandwidth. Typical specifications include a slew rate of 60V/μs, settling time of 250ns, power bandwidth of 1000kHz, and gain bandwidth of 12MHz. In addition to these outstanding dynamic features, these internally compensated amplifiers offer dielectric isolation and low offset currents. These amplifiers are ideally suited for applications such as high speed A/D and D/A converters, pulse amplification, and R.F. and video circuits.

Chip Layout and Dimensions



For Chip Geometries see Drawing 3, page 7-49.

Specifications

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Pads	40.0V	Operating Temp. Range HA0-2512-2	$-55^oC \leq T_A \leq +125^oC$
Differential Input Voltage	± 15.0V	HA0-2515-6	$0^oC \leq T_A \leq +75^oC$
Peak Output Current	50mA	Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$

ELECTRICAL SPECIFICATIONS

	PARAMETER	TEMPERATURE	HA0-2512-2 MINIMUM	HA0-2512-2 MAXIMUM	HA0-2515-6 MINIMUM	HA0-2515-6 MAXIMUM	UNITS
GUARANTEED CHARACTERISTICS $V^+ = +15VDC$, $V^- = -15VDC$	**INPUT CHARACTERISTICS**						
	Offset Voltage	+25°C		10		10	mV
		0°C to +125°C		14			mV
	Bias Current	+25°C		250		250	nA
		0°C to +125°C		500			nA
	Offset Current	+25°C		50		50	nA
		0°C to +125°C		100			nA
	Common Mode Range	+25°C	± 10.0		± 10.0		V
		0°C to +125°C	± 10.0				V
	TRANSFER CHARACTERISTICS						
	Large Signal Voltage Gain (1, 4)	+25°C	7.5K		7.5K		V/V
		0°C to +125°C	5K				V/V
	Common Mode Rejection Ratio (2)	+25°C	74		74		dB
		0°C to +125°C	74				dB
	OUTPUT CHARACTERISTICS						
	Output Voltage Swing (1)	+25°C	± 10.0		± 10.0		V
		0°C to +125°C	± 10.0				V
	Output Current (4)	+25°C	± 10		± 10		mA
	Full Power Bandwidth (4, 9)	+25°C	600				kHz
	TRANSIENT RESPONSE						
	Rise Time (1, 5, 6)	+25°C		50			ns
	Overshoot (1, 5, 7)	+25°C		50			%
	Slew Rate (1, 5)	+25°C	± 40				V/μs
	POWER SUPPLY CHARACTERISTICS						
	Supply Current	+25°C		6		6	mA
	Power Supply Rejection Ratio (8)	+25°C	74		74		dB
		0°C to +125°C	74				dB
TYPICAL CHARACTERISTICS	Input Resistance	+25°C	100		100		MΩ
	Gain Bandwidth Product (3)	+25°C	12		12		MHz
	Full Power Bandwidth (4)	+25°C	1,000		1,000		kHz
	Rise Time (1, 5, 6)	+25°C	25		25		ns
	Overshoot (1, 5, 7)	+25°C	25		25		%
	Slew Rate (1, 5)	+25°C	± 60		± 60		V/μs
	Settling Time (1, 4, 5)	+25°C	0.25		0.25		μs

NOTES:
1. $R_L = 2k$.
2. $V_{CM} = \pm 10V$.
3. $A_V < 10$.
4. $V_O = \pm 10.0V$.
5. $C_L = 50pF$.
6. $V_O = \pm 200mV$.
7. $V_O = \pm 200mV$.
8. $\Delta V = \pm 5.0V$.
9. Guaranteed based on $FPBW = \frac{\text{Slew Rate}}{20\pi}$

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HARRIS SEMICONDUCTOR PRODUCTS DIVISION
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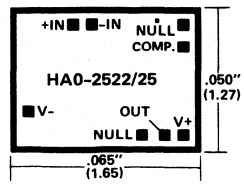
HA0-2522/25

Uncompensated High Slew Rate Operational Amplifiers

Description

HA0-2522 and HA0-2525 are high performance operational amplifiers designed to provide an unsurpassed combination of specifications for slew rate, bandwidth and settling time. A typical slew rate of 120V/μs and settling time of 700ns make these ideal for use in data acquisition systems and pulse amplification circuits. Typical gain bandwidth is 20MHz, with a power bandwidth of 2MHz. These dielectrically isolated amplifiers are controlled at closed loop gains greater than 3 without external compensation, and also provide low offset currents.

Chip Layout and Dimensions



For Chip Geometries see Drawing 4, page 7-49.

Specifications

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Pads	40.0V	Operating Temperature Range	
Differential Input Voltage	±15.0V	HA0-2522-2	$-55^{o}C \leq T_A \leq +125^{o}C$
Peak Output Current	50mA	HA0-2525-6	$0^{o}C \leq T_A \leq +75^{o}C$
		Storage Temperature Range	$-65^{o}C \leq T_A \leq +150^{o}C$

ELECTRICAL SPECIFICATIONS

	PARAMETER	TEMPERATURE	HA0-2522-2 MINIMUM	HA0-2522-2 MAXIMUM	HA0-2525-6 MINIMUM	HA0-2525-6 MAXIMUM	UNITS
GUARANTEED CHARACTERISTICS V+ = +15VDC, V- = -15VDC	INPUT CHARACTERISTICS						
	Offset Voltage	+25°C		10		10	mV
		0°C to +125°C		14			mV
	Bias Current	+25°C		250		250	nA
		0°C to +125°C		500			nA
	Offset Current	+25°C		50		50	nA
		0°C to +125°C		100			nA
	Common Mode Range	+25°C	±10.0		±10.0		V
		0°C to +125°C	±10.0				V
	TRANSFER CHARACTERISTICS						
	Large Signal Voltage Gain (1,4)	+25°C	7.5K		7.5K		V/V
		0°C to +125°C	5K				V/V
	Common Mode Rejection Ratio (2)	+25°C	74		74		dB
		0°C to +125°C	74				dB
	OUTPUT CHARACTERISTICS						
	Output Voltage Swing (1)	+25°C	±10.0		±10.0		V
		0°C to +125°C	±10.0				V
	Output Current (4)	+25°C	±10		±10		mA
	Full Power Bandwidth (4,8)	+25°C	1200				kHz
	TRANSIENT RESPONSE (A_V = +3)						
	Rise Time (1,5,6)	+25°C		50			ns
	Overshoot (1,5,6)	+25°C		50			%
	Slew Rate (1, 5)	+25°C	±80				V/μs
	POWER SUPPLY CHARACTERISTICS						
	Supply Current	+25°C		6		6	mA
	Power Supply Rejection Ratio (7)	+25°C	74		74		dB
		0°C to +125°C	74				dB
TYPICAL CHARACTERISTICS	Input Resistance	25°C	100		100		MΩ
	Gain Bandwidth Product (3)	25°C	20		20		MHz
	Full Power Bandwidth (4)	25°C	1600		1600		kHz
	Rise Time (1,5,6)	25°C	25		25		ns
	Overshoot (1,5,6)	25°C	25		25		%
	Slew Rate (1, 5)	25°C	±120		±120		V/μs
	Settling Time (1,4,5)	25°C	0.70		0.70		μs

NOTES:
1. R_L = 2K
2. V_{CM} = ±5.0V
3. $A_V > 10$
4. V_O = ± 10.0V.
5. C_L = 50pF.
6. V_O = ± 200mV.
7. V = 10V.
8. Guaranteed based on $FPBW = \frac{\text{Slew Rate}}{20\pi}$

7

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

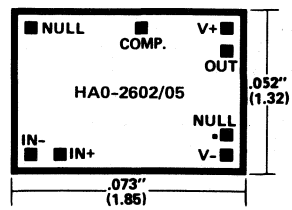
HA0-2602/2605

Wide Band, High Impedance Operational Amplifier

Description

HA0-2602 and HA0-2605 are internally compensated, dielectrically isolated, bipolar operational amplifiers that feature high input impedance (300MΩ typ.) and wide band AC performance. Typical specifications include a unity gain bandwidth of 12MHz, slew rate of 7V/μs, and 150K open loop gain enabling these amplifiers to perform high gain amplification of fast wide band signals. The frequency response of the amplifiers can be tailored to exact design requirements by means of an external bandwidth control capacitor. Applications include pulse amplification, high frequency circuits, and high gain, low distortion audio amplifiers.

Chip Layout and Dimensions



For Chip Geometries see Drawing 5, page 7-49.

Specifications

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Pads	45.0V	Operating Temp. Range HA0-2602-2	$-55^oC \leq T_A \leq +125^oC$
Differential Input Voltage	± 12.0V	HA0-2605-6	$0^oC \leq T_A \leq +75^oC$
Peak Output Current	Full Short Circuit Protection	Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$

ELECTRICAL SPECIFICATIONS

	PARAMETER	TEMPERATURE	HA0-2602-2 MINIMUM	HA0-2602-2 MAXIMUM	HA0-2605-6 MINIMUM	HA0-2605-6 MAXIMUM	UNITS
GUARANTEED CHARACTERISTICS $V^+ = +15VDC$ $V^- = -15VDC$	INPUT CHARACTERISTICS						
	Offset Voltage	+25°C		5		5	mV
		0°C to +125°C		7			mV
	Bias Current	+25°C		25		25	nA
		0°C to +125°C		60			nA
	Offset Current	+25°C		25		25	nA
		0°C to +125°C		60			nA
	Common Mode Range	+25°C	± 11.0		± 11.0		V
		0°C to +125°C	± 11.0				V
	TRANSFER CHARACTERISTICS						
	Large Signal Voltage Gain (1, 4)	+25°C	80K		80K		V/V
		0°C to +125°C	60K				V/V
	Common Mode Rejection Ratio (2)	+25°C	74		74		dB
		0°C to +125°C	74				dB
	OUTPUT CHARACTERISTICS						
	Output Voltage Swing (1)	+25°C	± 10.0		± 10.0		V
		0°C to +125°C	± 10.0				V
	Output Current (4)	+25°C	± 10		± 10		mA
	Full Power Bandwidth (4, 9)	+25°C	50				kHz
	TRANSIENT RESPONSE						
	Rise Time (1, 5, 6)	+25°C		60			ns
	Overshoot (1, 5, 7)	+25°C		40			%
	Slew Rate (1, 5)	+25°C	± 4				V/μs
	POWER SUPPLY CHARACTERISTICS						
	Supply Current	+25°C		4.0		4.0	mA
	Power Supply Rejection Ratio (8)	+25°C	74		74		dB
		0°C to +125°C	74				dB
TYPICAL CHARACTERISTICS	Input Resistance	+25°C	300		300		MΩ
	Unity Gain Bandwidth (3)	+25°C	12		12		MHz
	Full Power Bandwidth (4)	+25°C	75		75		kHz
	Rise Time (1, 5, 6)	+25°C	30		30		ns
	Overshoot (1, 5, 7)	+25°C	25		25		%
	Slew Rate (1, 5)	+25°C	± 7		± 7		V/μs
	Settling Time (1, 4, 5)	+25°C	1.5		1.5		μs

NOTES:
1. R_L - 2k.
2. $V_{CM} = \pm 5.0V$.
3. $V_O < 90mV$.
4. $V_O = \pm 10V$.
5. $C_L = 100pF$.
6. $V_O = \pm 200mV$.
7. $V_S = \pm 9.0V$ to $\pm 15V$.
8. Guaranteed based on

$$FPBW = \frac{\text{Slew Rate}}{2\pi V_{OUT}\ (\text{Peak})}$$

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

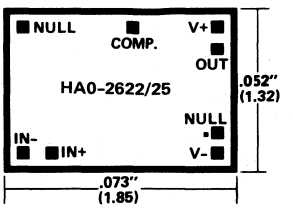
HA0-2622/2625

Very Wide Band, Uncompensated Operational Amplifier

Description

HA0-2622 and HA0-2625 are uncompensated, dielectrically isolated, bipolar operational amplifiers that feature high impedance (300MΩ , typ.) and wide band AC performance. Typical specifications include a gain bandwidth product of 100MHz, open loop gain of 150k, and a slew rate of 35V/μs. These outstanding dynamic features are complemented by low bias and offset currents and a low offset voltage. These amplifiers are ideally suited for pulse amplification and high frequency circuits. The frequency response is adjustable by means of an external capacitor.

Chip Layout and Dimensions



For Chip Geometries see Drawing 6, page 7-49.

Specifications

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Pads 45.0V
Differential Input Voltage ±12.0V
Peak Output Current Full Short Circuit Protection

Operating Temp. Range HA0-2622-2 $-55^{o}C \leq T_A \leq +125^{o}C$
HA0-2625-6 $0^{o}C \leq T_A \leq +75^{o}C$
Storage Temperature Range $-65^{o}C \leq T_A \leq +150^{o}C$

ELECTRICAL SPECIFICATIONS

	PARAMETER	TEMPERATURE	HA0-2622-2 MINIMUM	HA0-2622-2 MAXIMUM	HA0-2625-6 MINIMUM	HA0-2625-6 MAXIMUM	UNITS
GUARANTEED CHARACTERISTICS $V^+ = +15VDC$, $V^- = -15VDC$.	INPUT CHARACTERISTICS						
	Offset Voltage (1)	+25°C		5		5	mV
		0°C to +125°C		7			mV
	Bias Current	+25°C		25		25	nA
		0°C to +125°C		60			nA
	Offset Current	+25°C		25		25	nA
		0°C to +125°C		60			nA
	Common Mode Range	+25°C	±11.0		±11.0		V
		0°C to +125°C	±11.0				V
	TRANSFER CHARACTERISTICS						
	Large Signal Voltage Gain (2, 3)	+25°C	80K		80K		V/V
		0°C to +125°C	60K				V/V
	Common Mode Rejection Ratio (4)	+25°C	74		74		dB
		0°C to +125°C	74				dB
	OUTPUT CHARACTERISTICS						
	Output Voltage Swing (2)	+25°C	±10.0		±10.0		V
		0°C to +125°C	±10.0				V
	Output Current (3)	+25°C	±10		±10		mA
	Full Power Bandwidth (2, 3, 10)	+25°C	320				kHz
	TRANSIENT RESPONSE						
	Rise Time (2, 5, 7)	+25°C		45			ns
	Slew Rate (2, 7, 9)	+25°C	±20				V/μs
	POWER SUPPLY CHARACTERISTICS						
	Supply Current	+25°C		4.0		4.0	mA
	Power Supply Rejection Ratio (8)	+25°C	74		74		dB
		0°C to +125°C	74				dB
TYPICAL CHARACTERISTICS	Input Resistance	+25°C	300		300		MΩ
	Gain Bandwidth Product (2, 5, 6)	+25°C	100		100		MHz
	Full Power Bandwidth (2, 3)	+25°C	600		600		kHz
	Rise Time (2, 5, 7)	+25°C	17		17		ns
	Slew Rate (2, 7, 9)	+25°C	±35		±35		V/μs

NOTES:
1. Offset may be externally adjusted to zero.
2. $R_L = 2K\Omega$, $C_L = 50pF$.
3. $V_O = \pm 10.0V$.
4. $V_{CM} = \pm 10V$.
5. $V_O < 90mV$.
6. 40dB Gain.
7. $A_V = 5$ (The HA-2620 family is not stable at unity gain without external compensation)
8. $V_{SUPPLY} = \pm 9.0$ to $\pm 15.0V$.
9. $V_O = 5.0V$.
10. Guaranteed based on

$$FPBW = \frac{\text{Slew Rate}}{2\pi V_{OUT}\ (\text{Peak})}$$

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HARRIS SEMICONDUCTOR PRODUCTS DIVISION
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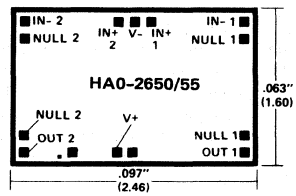
HA0-2650/2655

Dual High Performance Operational Amplifier

Description

HA0-2650 and HA0-2655 contain two internally compensated operational amplifiers offering high slew rate and high frequency performance conbined with exceptional DC characteristics. A 5V/μs slew rate and 8MHz bandwidth make these amplifiers suitable for processing fast, wide band signals extending into video frequencies. Signal processing is further enhanced by front-end performance including a 1.5mV offset voltage, 8μV/^{o}C offset voltage drift, and low offset and bias currents. Applications for these dielectrically isolated devices include video circuit designs and active filters.

Chip Layout and Dimensions



For Chip Geometries see Drawing 7, page 7-50.

Specifications

ABSOLUTE MAXIMUM RATINGS T_A = +25^{o}C unless otherwise stated.

Voltage Between V^+ and V^- Pads	40.0V	Operating Temperature Range	
Differential Input Voltage	±30.0V	HA0-2650-2	-55^{o}C ≤ T_A ≤ +125^{o}C
Input Voltage (1)	±15.0V	HA0-2655-6	0^{o}C ≤ T_A ≤ +75^{o}C
Output Short Circuit Duration (2)	Indefinite	Storage Temperature Range	-65^{o}C ≤ T_A ≤ +150^{o}C

ELECTRICAL SPECIFICATIONS

	PARAMETER	TEMPERATURE	HA0-2650-2 MINIMUM	HA0-2650-2 MAXIMUM	HA0-2655-6 MINIMUM	HA0-2655-6 MAXIMUM	UNITS
GUARANTEED CHARACTERISTICS V^+ = +15VDC, V^- = -15VDC	INPUT CHARACTERISTICS						
	Offset Voltage	+25^{o}C		3		5	mV
		0^{o}C to +125^{o}C		5			mV
	Bias Current	+25^{o}C		100		200	nA
		0^{o}C to +125^{o}C		200			nA
	Offset Current	+25^{o}C		30		60	nA
		0^{o}C to +125^{o}C		60			nA
	Common Mode Range	+25^{o}C	±13		±13		V
		0^{o}C to +125^{o}C	±13				V
	TRANSFER CHARACTERISTICS						
	Large Signal Voltage Gain (2A, B)	+25^{o}C	25K		20K		V/V
		0^{o}C to +125^{o}C	20K				V/V
	Common Mode Rejection Ratio (3)	+25^{o}C	80		74		dB
		0^{o}C to +125^{o}C	80				dB
	OUTPUT CHARACTERISTICS						
	Output Voltage Swing (2C)	+25^{o}C	±13		±13		V
		0^{o}C to +125^{o}C	±13				V
	Full Power Bandwidth (4, 7)	+25^{o}C	30		30		kHz
	TRANSIENT RESPONSE						
	Slew Rate	+25^{o}C	±2				V/μs
	POWER SUPPLY CHARACTERISTICS						
	Supply Current	+25^{o}C		3		4	mA
	Power Supply Rejection Ratio (6)	+25^{o}C	80		74		dB
		0^{o}C to +125^{o}C	80				dB
TYPICAL CHARACTERISTICS	Differential Input Resistance	+25^{o}C	20		20		MΩ
	Common Mode Input Resistance	+25^{o}C	500		500		MΩ
	Full Power Bandwidth (4)	+25^{o}C	80		80		kHz
	Output Current (2A)	+25^{o}C	±20		±18		mA
	Rise Time (5)	+25^{o}C	40		40		ns
	Overshoot (5)	+25^{o}C	15		15		%
	Slew Rate	+25^{o}C	±5		±5		V/μs

NOTES:
1. For supply voltages ±15V, the ab. max. input voltage is equal to the supply voltage.
2. a) V_O = ±10V
   b) R_L = 2k.
   c) R_L = 10k.
3. V_{CM} = ±10V.
4. A_V = 1, R_L = 2k, V_O = 20V_{p-p}.
5. V_{IN} = 200mV.
6. ΔV = ±5.0V.
7. Guaranteed based on

$$FPBW = \frac{\text{Slew Rate}}{2\pi V_{OUT}\ \text{(Peak)}}$$

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

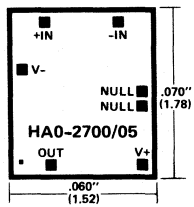
HA0-2700/2705

Low Power, High Performance Operational Amplifier

Description

HA0-2700 and HA0-2705 are internally compensated operational amplifiers employing dielectric isolation to achieve excellent dynamic and DC performance with very low power consumption (2.24mW @ ±15.0V typ.). Accurate high gain signal amplification is provided by an open loop gain of 300k and a high CMRR (106dB), low offset voltage, and low offset and bias currents. A gain bandwidth of 1MHz and a slew rate of 20V/μs allow for processing of fast, wide band signals. These amplifiers operate from a wide power supply range and are ideally suited for low power applications requiring a fast, accurate response over a wide frequency signal range.

Chip Layout and Dimensions



For Chip Geometries see Drawing 8, page 7-50.

Specifications

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- pads	44.0V	Operating Temperature Range	
Differential Input Voltage	±18.0V	HA0-2700-2	$-55^{o}C \leq T_A \leq +125^{o}C$
Storage Temperature Range	$-65^{o}C \leq T_A \leq +150^{o}C$	HA0-2705-6	$0^{o}C \leq T_A \leq +75^{o}C$

ELECTRICAL SPECIFICATIONS

	PARAMETER	TEMPERATURE	HA0-2700-2 MINIMUM	HA0-2700-2 MAXIMUM	HA0-2705-6 MINIMUM	HA0-2705-6 MAXIMUM	UNITS
GUARANTEED CHARACTERISTICS $V^+ = +15VDC$, $V^- = -15VDC$.	INPUT CHARACTERISTICS						
	Offset Voltage (1)	+25°C		3.0		5.0	mV
		0°C to +125°C		5.0			mV
	Bias Current	+25°C		20		40	nA
		0°C to +125°C		50			nA
	Offset Current	+25°C		10		15	nA
		0°C to +125°C		30			nA
	Common Mode Range	+25°C	± 11.0		± 11.0		V
		0°C to +125°C	± 11.0				V
	TRANSFER CHARACTERISTICS						
	Large Signal Voltage Gain (2, 3)	+25°C	200K		200K		V/V
		0°C to +125°C	100K				V/V
	Common Mode Rejection Ratio (4)	+25°C	86		80		dB
		0°C to +125°C	86				dB
	OUTPUT CHARACTERISTICS						
	Output Voltage Swing (2)	+25°C	± 12.0		± 12.0		V
		0°C to +125°C	± 11.0				V
	TRANSIENT RESPONSE						
	Slew Rate (2, 6)	+25°C	10				V/μs
	POWER SUPPLY CHARACTERISTICS						
	Supply Current	+25°C		150		150	μA
	Power Supply Rejection Ratio (5)	+25°C	86		80		dB
		0°C to +125°C	86				dB
TYPICAL CHARACTERISTICS	Gain Bandwidth Product	+25°C	1.0		1.0		MHz
	Output Current	+25°C	10		10		mA
	Slew Rate (2, 6)	+25°C	20		20		V/μs

NOTES:
1. Can be adjusted to zero with 1MΩ pot. between Pads 1 and 8 with the tap to Pad 7.
2. $R_L = 2k$, $C_L = 100pF$.
3. $V_O = \pm 10.0V$.
4. $V_{CM} = \pm 5.0V$.
5. $V_S = \pm 10.0V$ to $\pm 20.0V$.
6. $A_V = 5$.

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HARRIS SEMICONDUCTOR PRODUCTS DIVISION
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HA0-2720/2725

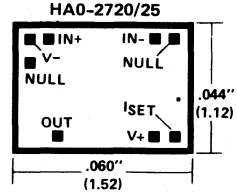
Wide Range Programmable Operational Amplifier

Description

HA0-2720 and HA0-2725 are internally compensated programmable amplifiers offering a wide performance range that is adjustable by means of the circuits' set current (I_{SET}). By means of adjusting an external resistor or current source, power dissipation, slew rate, bandwidth, output current, and input noise can be programmed to desired levels. This versatile adjustment capability enables the HA0-2720/25 to provide optimum design solutions by delivering the required level of performance with the minimum power dissipation. HA0-2720/25 also operate over a wide supply range (±1.2V to ±15V).

Chip Layout and Dimensions

HA0-2720/25



For Chip Geometries see Drawing 9, page 7-50.

Specifications

ABSOLUTE MAXIMUM RATINGS

I_{SET} (Current at I_{SET})	500μA	V_{SET} (Voltage to Gnd. at I_{SET})	$V^+ - 2.0V \leq V_{SET} \leq V^+$
Differential Input Voltage	± 30.0V	Operating Temperature HA0-2720-2	$-55^oC \leq T_A \leq +125^oC$
Input Voltage (1)	± 15.0V	HA0-2725-6	$0^oC \leq T_A \leq +75^oC$
Voltage Between V^+ and V^- Pads	45.0V	Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$

ELECTRICAL SPECIFICATIONS

	PARAMETER	TEMPERATURE	HA0-2720-2 MINIMUM	HA0-2720-2 MAXIMUM	HA0-2725-6 MINIMUM	HA0-2725-6 MAXIMUM	UNITS
GUARANTEED CHARACTERISTICS $V^+ = +15VDC$, $V^- = -15VDC$, $I_{SET} = 15\mu A$	INPUT CHARACTERISTICS						
	Offset Voltage	+25°C		3.0		5.0	mV
		0°C to +125°C		5.0			mV
	Offset Current	+25°C		10		10	nA
		0°C to +125°C		20			nA
	Bias Current	+25°C		20		30	nA
		0°C to +125°C		40			nA
	TRANSFER CHARACTERISTICS						
	Large Signal Voltage Gain (4)	+25°C	40K		25K		V/V
		0°C to +125°C	25K				V/V
	Common Mode Rejection Ratio (3)	+25°C	80		74		dB
		0°C to +125°C	80				dB
	OUTPUT CHARACTERISTICS						
	Output Voltage Swing (2)	+25°C	±12		±12		V
		0°C to +125°C	±10				V
	POWER SUPPLY CHARACTERISTICS						
	Supply Current (Each Amp)	+25°C		250		250	μA
		0°C to +125°C		250			μA
	Power Supply Rejection Ratio (7)	+25°C	80		76		dB
		0°C to +125°C	80				dB
TYPICAL CHARACTERISTICS	Input Resistance	+25°C	5		5		MΩ
	Output Current (4)	+25°C	±5.0		±5.0		mA
	Rise Time (5)	+25°C	0.2		0.2		μs
	Overshoot (5)	+25°C	15		15		%
	Slew Rate (6)	+25°C	0.8		0.8		V/μs

NOTES:
1. For supply voltages $< \pm 15.0V$, the ab. max. input voltage is equal to supply voltage.
2. For T = +25°C $R_L = 5k\Omega$, For T = +125°C $R_L = 75k\Omega$.
3. $V_{CM} = \pm 5.0V$.
4. $V_O = \pm 10.0V$.
5. $A_V = +1$, $V_{IN} = 400mV$, $R_L = 5k\Omega$ $C_L = 100pF$.
6. $V_O = +10.0V$, $R_L = 5k\Omega$.
7. $\Delta V = \pm 5.0V$.

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HARRIS SEMICONDUCTOR PRODUCTS DIVISION
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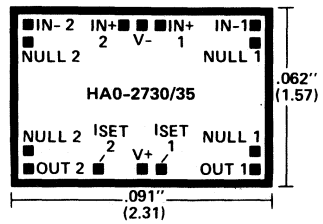
HA0-2730/2735

Wide Range Dual Programmable Operational Amplifier

Description

HA0-2730 and HA0-2735 are internally compensated programmable amplifiers offering a wide performance range that is adjustable by means of the circuits' set current (I_{SET}). By means of adjusting an external resistor or current source, power dissipation, slew rate, bandwidth, output current, and input noise can be programmed to desired levels. This versatile adjustment capability enables the HA0-2730/35 to provide optimum design solutions by delivering the required level of performance with the minimum power dissipation. HA0-2730/35 also operate over a wide supply range (±1.2V to ±15V).

Chip Layout and Dimensions



For Chip Geometries see Drawing 10, page 7-50.

Specifications

ABSOLUTE MAXIMUM RATINGS

I_{SET} (Current at I_{SET})	500μA	V_{SET} (Voltage to Gnd. at I_{SET})	$V^+ - 2.0V \leq V_{SET} \leq V^+$
Voltage Between V^+ and V^- Pads	45.0V	Operating Temp. Range HA0-2730-2	$-55^oC \leq T_A \leq +125^oC$
Differential Input Voltage	±30.0V	HA0-2735-6	$0^oC \leq T_A \leq +75^oC$
Input Voltage	± 15.0V	Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$

ELECTRICAL SPECIFICATIONS

	PARAMETER	TEMPERATURE	HA0-2730-2 MINIMUM	HA0-2730-2 MAXIMUM	HA0-2735-6 MINIMUM	HA0-2735-6 MAXIMUM	UNITS
GUARANTEED CHARACTERISTICS $V^+ = +15VDC$, $V^- = -15VDC$, $I_{SET} = 15\mu A$	INPUT CHARACTERISTICS						
	Offset Voltage	+25°C		3.0		5.0	mV
		0°C to +125°C		5.0			mV
	Offset Current	+25°C		10		10	nA
		0°C to +125°C		20			nA
	Bias Current	+25°C		20		30	nA
		0°C to +125°C		40			nA
	TRANSFER CHARACTERISTICS						
	Large Signal Voltage Gain (4)	+25°C	40K		25K		V/V
		0°C to +125°C	25K				V/V
	Common Mode Rejection Ratio (3)	+25°C	80		74		dB
		0°C to +125°C	80				dB
	OUTPUT CHARACTERISTICS						
	Output Voltage Swing (2)	+25°C	± 12		± 12		V
		0°C to +125°C	± 10				V
	POWER SUPPLY CHARACTERISTICS						
	Supply Current (Each Amp)	+25°C		250		250	μA
		0°C to +125°C		250			μA
	Power Supply Rejection Ratio (7)	+25°C	80		76		dB
		0°C to +125°C	80				dB
TYPICAL CHARACTERISTICS	Input Resistance	+25°C	5		5		MΩ
	Output Current (4)	+25°C	± 5.0		± 5.0		mA
	Rise Time (5)	+25°C	0.2		0.2		μs
	Overshoot (5)	+25°C	15		15		%
	Slew Rate (6)	+25°C	0.8		0.8		V/μs

NOTES:
1. For supply voltages $< \pm 15.0V$, the ab. max. input voltage is equal to supply voltage.
2. For T = +25°C $R_L = 5k\Omega$. For T = +125°C $R_L = 75k\Omega$.
3. $V_{CM} = \pm 1.5V$.
4. $V_O = \pm 10.0V$.
5. $A_V = +1$, $V_{IN} = 400mV$, $R_L = 5k\Omega$, $C_L = 100pF$.
6. $V_O = \pm 10.0V$, $R_L = 5k$.
7. $\Delta V = \pm 1.5V$.

7

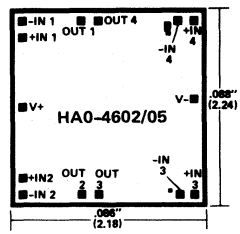
HA0-4602/4605

High Performance Quad Operational Amplifier

Description

HA0-4602 and HA0-4605 are high performance quad operational amplifiers offering superior specifications over existing quad amplifiers. These dielectrically isolated devices offer excellent dynamic performance coupled with low value for offset voltage, drift, input noise voltage, and power consumption. A wide bandwidth of 8MHz, low power of 35mW/amp, and internal compensation make these devices ideal for precision active filters. Other applications include audio circuits, instrumentation and signal conditioning, and data acquisition systems.

Chip Layout and Dimensions



For Chip Geometries see Drawing 11, page 7-50.

Specifications

ABSOLUTE MAXIMUM RATINGS T_A = +25°C unless otherwise stated

Voltage Between V^+ and V^- Pads	40.0V	Operating Temperature Range	
Differential Input Voltage	±7V	HA0-4602-2	-55°C ≤ T_A ≤ +125°C
Input Voltage (1)	±15.0V	HA0-4605-6	0°C ≤ T_A ≤ +75°C
Output Short Circuit Duration (2)	Indefinite	Storage Temperature Range	-65°C ≤ T_A ≤ +150°C

ELECTRICAL SPECIFICATIONS

	PARAMETER	TEMPERATURE	HA0-4602-2* MINIMUM	HA0-4602-2* MAXIMUM	HA0-4605-6 MINIMUM	HA0-4605-6 MAXIMUM	UNITS
GUARANTEED CHARACTERISTICS V^+ = +15VDC, V^- = -15VDC	**INPUT CHARACTERISTICS**						
	Offset Voltage	+25°C		2.5		3.5	mV
		0°C to +125°C		3.0			mV
	Bias Current	+25°C		200		300	nA
		0°C to +125°C		325			nA
	Offset Current	+25°C		75		100	nA
		0°C to +125°C		125			nA
	Common Mode Range	+25°C	±12		±12		V
		0°C to +125°C	±12				V
	TRANSFER CHARACTERISTICS						
	Large Signal Voltage Gain (3)	+25°C	100k		75k		V/V
		0°C to +125°C	100k				V/V
	Common Mode Rejection Ratio (6)	+25°C	86		80		dB
		0°C to +125°C	86				dB
	OUTPUT CHARACTERISTICS						
	Output Voltage Swing R_L = 10k	+25°C	±12		±12		V
		0°C to +125°C	±12				V
	R_L = 2k	+25°C	±10		±10		V
		0°C to +125°C	±10				V
	Output Current (5)	+25°C	±10		±8		mA
		0°C to +125°C	±10				mA
	POWER SUPPLY CHARACTERISTICS						
	Supply Current	+25°C		5.5		6.5	mA
	Power Supply Rejection Ratio (6)	+25°C	86		80		dB
		0°C to +125°C	86				dB
TYPICAL CHARACTERISTICS	Input Noise Voltage (f = 1kHz)	+25°C	8		8		$nV/\sqrt{Hz}$
	Input Resistance	+25°C	500		500		kΩ
	Channel Separation (4)	+25°C	-108		-108		dB
	Small Signal Bandwidth	+25°C	8		8		MHz
	Full Power Bandwidth (3)	+25°C	60		60		kHz
	Rise Time	+25°C	50		50		ns
	Overshoot	+25°C	30		30		%
	Slew Rate	+25°C	±4		±4		V/μs
	Settling Time (7)	+25°C	4.2		4.2		μs

*Preliminary, consult factory for final specifications.

NOTES:
1. For supply voltages < ±15V, the ab. max. input voltage is equal to the supply voltage.
2. Any one amplifier may be shorted to ground indefinitely.
3. V_{OUT} = ±10V, R_L = 2kΩ.
4. Channel separation value is referred to the input of the amp. Input test conditions are: f = 10kHz, V_{IN} = 200mV_{p-p}, R_S = 1kΩ.
5. V_{OUT} = ±5V.
6. ΔV = ±5.0V.
7. To 0.01% of final value, ΔV_{OUT} = ±10V, A_V = -1.

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
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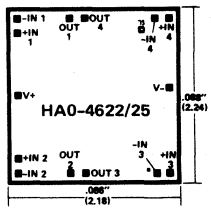
HA0-4622/4625

Wideband, High Performance Quad Operational Amplifiers

Description

HA0-4622 and HA0-4625 are wide band quad operational amplifiers featuring high slew rate, wide bandwidth and fast settling time. These devices are optimized to provide superior operating characteristics in applications where a gain of 10 or greater is to be used. In addition to 70MHz gain bandwidth and 20V/μsec slew rate, HA0-4622/4625 offer low power consumption of 35mW/amp and very low input noise voltage of $8nV/\sqrt{Hz}$.

Chip Layout and Dimensions



For Chip Geometries see Drawing 12, page 7-50.

Specifications

ABSOLUTE MAXIMUM RATINGS T_A = +25°C unless otherwise stated

Voltage Between V^+ and V^- Pads	40.0V	Operating Temperature Range	
Differential Input Voltage	±7V	HA0-4602-2	-55°C ≤ T_A ≤ +125°C
Input Voltage (1)	±15.0V	HA0-4605-6	0°C ≤ T_A ≤ +75°C
Output Short Circuit Duration (2)	Indefinite	Storage Temperature Range	-65°C ≤ T_A ≤ +150°C

ELECTRICAL SPECIFICATIONS

	PARAMETER	TEMPERATURE	HA0-4622-2* MINIMUM	HA0-4622-2* MAXIMUM	HA0-4625-6 MINIMUM	HA0-4625-6 MAXIMUM	UNITS
GUARANTEED CHARACTERISTICS V^+ = +15VDC, V^- = -15VDC.	INPUT CHARACTERISTICS						
	Offset Voltage	+25°C		2.5		3.5	mV
		0°C to +125°C		3.0			mV
	Bias Current	+25°C		200		300	nA
		0°C to +125°C		325			nA
	Offset Current	+25°C		75		100	nA
		0°C to +125°C		125			nA
	Common Mode Range	+25°C	±12		±12		V
		0°C to +125°C	±12				V
	TRANSFER CHARACTERISTICS						
	Large Signal Voltage Gain (3)	+25°C	100K		75K		V/V
		0°C to +125°C	100K				V/V
	Common Mode Rejection Ratio (6)	+25°C	86		80		dB
		0°C to +125°C	86				dB
	OUTPUT CHARACTERISTICS						
	Output Voltage Swing R_L = 10kΩ	+25°C	±12		±12		V
		0°C to +125°C	±12				V
	R_L = 2kΩ	+25°C	±10		±10		V
		0°C to +125°C	±10				V
	Output Current (5)	+25°C	±10		±8		mA
		0°C to +125°C	±10				mA
	POWER SUPPLY CHARACTERISTICS						
	Supply Current	+25°C		5.5		6.5	mA
	Power Supply Rejection Ratio (6)	+25°C	86		80		dB
		0°C to +125°C	86				dB

TYPICAL CHARACTERISTICS	Input Noise Voltage (f = 1kHz)	+25°C	8	8	$nV/\sqrt{Hz}$
	Input Resistance	+25°C	500	500	kΩ
	Channel Separation (4)	+25°C	-108	-108	dB
	Gain Bandwidth Product (5)	+25°C	70	70	MHz
	Full Power Bandwidth (3)	+25°C	260	260	kHz
	Rise Time	+25°C	40	40	ns
	Overshoot	+25°C	45	45	%
	Slew Rate	+25°C	±20	±20	V/μs
	Settling Time (7)	+25°C	2.5	2.5	μs

NOTES:
1. For supply voltages ±15V, the ab. max. input voltage is equal to the supply voltage.
2. Any one amplifier may be shorted to ground indefinitely.
3. V_{OUT} = ±10V, R_L = 2kΩ
4. Channel separation value is referred to the input of the amp. Input test conditions are: f = 10kHz, V_{IN} = 200mV_{p-p}, R_S = 1kΩ.
5. V_{OUT} = ±5V.
6. ΔV = ±5.0V.
7. To 0.01% of final value, ΔV_{OUT} = ±10V, A_V = -1.
8. A_V = 10; R_L = 2k; C_L ≤ 10pf.

*Preliminary, consult factory for final specifications.

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HARRIS SEMICONDUCTOR PRODUCTS DIVISION
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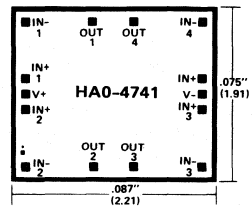
HA0-4741

Quad Operational Amplifier

Description

The HA0-4741 is a quad operational amplifier with operating characteristics that equal or exceed those of the 741 type amplifier in all categories of performance. The HA0-4741 is well suited for applications requiring accurate signal processing by virtue of its low values of input offset voltage (0.5mV typ.), input bias current and input voltage noise. The 3.5MHz bandwidth, coupled with high open loop gain, allow the HA0-4741 to be used in designs requiring amplification of wide band signals. These amplifiers also feature a wide supply range and a high level of amplifier to amplifier isolation.

Chip Layout and Dimensions



For Chip Geometries see Drawing 13, page 7-51.

Specifications

ABSOLUTE MAXIMUM RATINGS T_A = +25°C Unless otherwise stated.

Voltage Between V+ and V- Pads	40.0V	Operating Temperature Range	
Differential Input Voltage	±30.0V	HA0-4741-2	-55°C ≤ T_A ≤ +125°C
Input Voltage (1)	±15.0V	HA0-4741-6	0°C ≤ T_A ≤ +75°C
Output Short Circuit Duration (2)	Indefinite	Storage Temperature Range	-65°C ≤ T_A ≤ +150°C

ELECTRICAL SPECIFICATIONS

	PARAMETER	TEMPERATURE	HA0-4741-2 MINIMUM	HA0-4741-2 MAXIMUM	HA0-4741-6 MINIMUM	HA0-4741-6 MAXIMUM	UNITS
GUARANTEED CHARACTERISTICS V^+ = +15VDC V^- = -15VDC	INPUT CHARACTERISTICS						
	Offset Voltage	+25°C		3.0		5.0	mV
		0°C to +125°C		5.0			mV
	Bias Current	+25°C		200		300	nA
		0°C to +125°C		325			nA
	Offset Current	+25°C		30		50	nA
		0°C to +125°C		75			nA
	Common Mode Range	+25°C	±12		±12		V
		0°C to +125°C	±12				V
	TRANSFER CHARACTERISTICS						
	Large Signal Voltage Gain (3)	+25°C	50K		25K		V/V
		0°C to +125°C	25K				V/V
	Common Mode Rejection Ratio (6)	+25°C	80		80		dB
		0°C to +125°C	74				dB
	OUTPUT CHARACTERISTICS						
	Output Voltage Swing (R_L = 2kΩ)	+25°C	±10		±10		V
		0°C to +125°C	±10				V
	Output Current (5)	+25°C	±5		±5		mA
		0°C to +125°C	±5				mA
	POWER SUPPLY CHARACTERISTICS						
	Supply Current (I^+ or I^-)	+25°C		5.0		7.0	mA
	Power Supply Rejection Ratio (6)	+25°C	80		80		dB
		0°C to +125°C	80				dB
TYPICAL CHARACTERISTICS	Differential Input Resistance	+25°C	5		5		MΩ
	Input Noise Voltage (f = 1kHz)	+25°C	9		9		$nV/\sqrt{Hz}$
	Channel Separation (4)	+25°C	-108		-108		dB
	Small Signal Bandwidth	+25°C	3.5		3.5		MHz
	Full Power Bandwidth (3)	+25°C	25		25		kHz
	Rise Time	+25°C	75		75		ns
	Overshoot	+25°C	25		25		%
	Slew Rate	+25°C	±1.6		±1.6		V/μs

NOTES:
1. For supply voltages < ±15V, the ab. max. input voltage is equal to the supply voltage.
2. One amp may be shorted to ground indefinitely.
3. V_{OUT} = ±10, R_L = 2k.
4. Referred to input: f = 10kHz, R_S = 1k.
5. V_{OUT} = ±10.
6. Δ V = ±5.0V.

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HARRIS SEMICONDUCTOR PRODUCTS DIVISION
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HI0-200

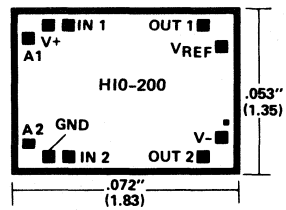
Dual SPST CMOS Analog Switch

Description

HI0-200 is a dual SPST CMOS analog switch featuring independently selectable switches and fast switching speeds (240ns typ.). Each switch provides low "ON" resistance operation for input signal voltages up to the supply rails and for signal current up to 80mA. Employing dielectric isolation and CMOS processing, HI0-200 operates without any problems induced by latch-up or SCR mode phenomena.

All devices provide break-before-make switching and are TTL and CMOS compatible. HI0-200 is an ideal component for use in high frequency analog switching. Typical applications include signal path switching, sample and hold circuits, digital filters, and op amp gain switching networks.

Chip Layout and Dimensions



For Chip Geometries see Drawing 14, page 7-51.

Specifications

ABSOLUTE MAXIMUM RATINGS

Supply Voltage between pads 6 and 10	+40V	Operating Temperature Range	
V_{REF} to Ground	+20, -5V	HI0-0200-2	-55°C to +125°C
Digital Input Voltage	$+V_{SUPPLY}$ +4V, $-V_{SUPPLY}$ -4V	HI0-0200-6	0°C to 75°C
Analog Input Voltage (1 Switch)	$+V_{SUPPLY}$ +2.0V, $-V_{SUPPLY}$ -2.0V	Storage Temperature	-65°C to +150°C

ELECTRICAL SPECIFICATIONS

GUARANTEED CHARACTERISTICS Unless otherwise specified, Supplies = +15V, -15V: V_{REF} = Open; V_{AH} (Logic Level High) = 3.0V, V_{AL} (Logic Level Low) = +0.8V.

PARAMETER	TEMPERATURE	HI0-0200-2 MINIMUM	HI0-0200-2 MAXIMUM	HI0-0200-6 MINIMUM	HI0-0200-6 MAXIMUM	UNITS
ANALOG SWITCH CHARACTERISTICS						
V_S, Analog Signal Range	+25°C	-15	+15	-15	+15	V
	-55°C to +125°C	-15	+15			V
R_{ON}, On Resistance (1)	+25°C		70		80	Ω
	-55°C to +125°C		100			Ω
I_S (OFF), Off Input Leakage Current	+25°C		500		500	nA
	-55°C to +125°C		500			nA
I_D (OFF), Off Output Leakage Current	+25°C		500		500	nA
	-55°C to +125°C		500			nA
I_D (ON), On Leakage Current	+25°C		500		500	nA
	-55°C to +125°C		500			nA
DIGITAL INPUT CHARACTERISTICS						
V_{AL}, Input Low Threshold	+25°C		0.8		0.8	V
	-55°C to +125°C		0.8			V
V_{AH}, Input High Threshold	+25°C	3.0		3.0		V
	-55°C to +125°C	3.0				V
I_A, Input Leakage Current (High or Low) (2)	+25°C		1.0		1.0	μA
	-55°C to +125°C		1.0			μA
SWITCHING CHARACTERISTICS						
t_{ON}, Switch ON Time	+25°C		500			ns
t_{OFF}, Switch OFF Time	+25°C		500			ns
POWER REQUIREMENTS (3)						
P_D, Power Dissipation	+25°C		60		60	mW
	-55°C to +125°C		60			mW
I^+, Current	+25°C		2.0		2.0	mA
	-55°C to +125°C		2.0			mA
I^-, Current	+25°C		2.0		2.0	mA
	-55°C to +125°C		2.0			mA

TYPICAL CHARACTERISTICS

Break Before Make Delay (4)	+25°C		60		60	ns
t_{ON}, Switch ON Time	+25°C		240		240	ns
t_{OFF}, Switch OFF Time	+25°C		330		500	ns
Off Isolation (5)	+25°C		70		70	dB

NOTES:
1. V_{OUT} = +10V, I_{OUT} = 1mA.
2. Digital inputs are MOS gates. Typical leakage is < 1nA.
3. V_A = +3V or V_A = 0V for both switches.
4. V_{AH} = 4.0V.
5. V_A = +3V, R_L = 1kΩ, C_L = 10pF, V_S = 3Vrms, f = 100kHz.

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HARRIS SEMICONDUCTOR PRODUCTS DIVISION
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HIO-201

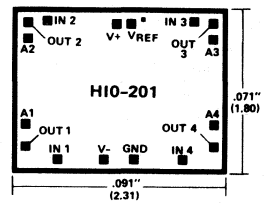
Quad SPST CMOS Analog Switch

Description

HIO-201 is a quad SPST CMOS analog switch featuring independently selectable switches and fast switching speeds (185ns typ.). Each switch provides low "ON" resistance operation for input signal voltages up to the supply rails and for signal currents up to 80mA. Employing dielectric isolation and CMOS processing, HIO-201 operates without any problems induced by latch-up or SCR mode phenomena.

All devices provide break-before-make switching and are TTL and CMOS compatible. HIU-201 is an ideal component for use in high frequency analog switching, sample and hold circuits, digital filters, and op amp gain switching networks.

Chip Layout and Dimensions



For Chip Geometries see Drawing 15, page 7-51.

Specifications

ABSOLUTE MAXIMUM RATINGS

V_{REF} to Ground	+20V, -5V	Operating Temperature Range	
Digital Input Voltage	$+V_{SUPPLY}$ +4V	HIO-0201-2	-55°C to +125°C
	$-V_{SUPPLY}$ -4V	HIO-0201-6	0°C to +75°C
Analog Input Voltage (One Switch)	$+V_{SUPPLY}$ +2.0V	Storage Temperature Range	-65°C to +150°C
	$-V_{SUPPLY}$ -2.0V	Supply Voltage Between Pads 4 and 13	+40V

ELECTRICAL SPECIFICATIONS

GUARANTEED CHARACTERISTICS Unless otherwise specified, Supplies = +15V, -15V: V_{REF} = Open; V_{AH} (Logic Level High) = 3.0V, V_{AL} (Logic Level Low) = +0.8V.

PARAMETER	TEMPERATURE	HIO-0201-2 MINIMUM	HIO-0201-2 MAXIMUM	HIO-0201-6 MINIMUM	HIO-0201-6 MAXIMUM	UNITS
ANALOG SWITCH CHARACTERISTICS						
V_S, Analog Signal Range	+25°C	-15	+15	-15	+15	V
	-55°C to +125°C	-15	+15			V
R_{ON}, On Resistance (1)	+25°C		80		100	Ω
	-55°C to +125°C		125			Ω
I_S (OFF), Off Input Leakage Current (6)	+25°C		250		250	nA
	-55°C to +125°C		500			nA
I_D (OFF), Off Output Leakage Current (6)	+25°C		250		250	nA
	-55°C to +125°C		500			nA
I_D (ON), On Leakage Current (6)	+25°C		250		250	nA
	-55°C to +125°C		500			nA
DIGITAL INPUT CHARACTERISTICS						
V_{AL}, Input Low Threshold	+25°C		0.8		0.8	V
	-55°C to +125°C		0.8			V
V_{AH}, Input High Threshold	+25°C	3.0		3.0		V
	-55°C to +125°C	3.0				V
I_A, Input Leakage Current (High or Low) (2)	+25°C		1.0		1.0	μA
	-55°C to +125°C		1.0			μA
SWITCHING CHARACTERISTICS						
t_{ON}, Switch ON Time	+25°C		500			ns
t_{OFF}, Switch OFF Time	+25°C		500			ns
POWER REQUIREMENTS (3)						
P_D, Power Dissipation	+25°C		60		60	mW
	-55°C to +125°C		60			mW
I^+, Current	+25°C		2.0		2.0	mA
	-55°C to +125°C		2.0			mA
I^-, Current	+25°C		2.0		2.0	mA
	-55°C to +125°C		2.0			mA

TYPICAL CHARACTERISTICS

t_{OPEN}, Break Before Make Delay (4)	+25°C	30		30		ns
t_{ON}, Switch ON Time	+25°C	185		185		ns
t_{OFF}, Switch OFF Time	+25°C	220		220		ns
Off Isolation (5)	+25°C	80		80		dB

NOTES:
1. V_{OUT} = +10V, I_{OUT} = 1mA.
2. Digital inputs are MOS gates. Typical leakage is <1nA.
3. V_A = +3V or V_A = 0V for all switches.
4. V_{AH} = 4.0V.
5. V_A = 5V, R_L = 1kΩ, C_L = 10pF, V_S = 3Vrms, f = 100kHz.
6. V_{ANL} = ±14V.

HIO-5046/5047/5049/5051

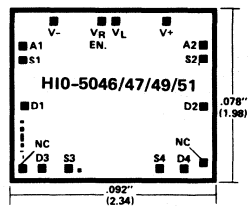
Low Resistance CMOS Analog Switch

Description

This family of CMOS switches offers a variety of switching functions featuring low resistance operation for analog voltages up to the supply rails and signal currents up to 80mA. The "ON" resistance is reasonably constant over variations in temperature, input voltage and input current. R_{ON} remains exceptionally constant for input voltages between +5V and -5V and currents up to 50mA.

All devices provide break-before-make switching and are TTL and CMOS compatible. Performance is further enhanced by dielectric isolation processing insuring latch-free operation and very low leakage currents (0.8nA at 25°C typ.). These switches also feature very low power operation (1.5mW at 25°C typ.).

Chip Layout and Dimensions



For Chip Geometries see Drawing 16 -19, pages 7-51 & 52.

Specifications

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V^+, V^-)	36V	Operating Temperature Range	
V_R to Ground	V^+, V^-	HIO-5046/47/49/51-2	-55°C to +125°C
Digital and Analog Input Voltage	V^- - 4V, V^+ + 4V	HIO-5046/47/49/51-6	0°C to 75°C
Analog Current (S to D)	80mA	Storage Temperature Range	-65°C to +150°C

ELECTRICAL SPECIFICATIONS

	PARAMETER	TEMPERATURE	HIO-5046/47-2 HIO-5049/51-2 MINIMUM	HIO-5046/47-2 HIO-5049/51-2 MAXIMUM	HIO-5046/47-6 HIO-5049/51-6 MINIMUM	HIO-5046/47-6 HIO-5049/51-6 MAXIMUM	UNITS
GUARANTEED CHARACTERISTICS Unless otherwise specified supplies = +15V,-15V, V_R = 0V, V_{AH} (Logic Level High) = 3.0V, V_{AL} (Logic Level Low) = +0.8V, V_L = +5V	ANALOG SWITCH CHARACTERISTICS						
	Analog Signal Range	+25°C	-15	+15	-15	+15	V
		-55°C to +125°C	-15	+15			V
	R_{ON}, On Resistance (1)	+25°C		75		75	Ω
		-55°C to +125°C		75			Ω
	I_S (OFF), Off Input Leakage Current	+25°C		500		500	nA
		-55°C to +125°C		500			nA
	I_D (OFF), Off Output Leakage Current	+25°C		500		500	nA
		-55°C to +125°C		500			nA
	I_D (ON), On Leakage Current	+25°C		500		500	nA
		-55°C to +125°C		500			nA
	DIGITAL INPUT CHARACTERISTICS						
	V_{AL}, Input Low Threshold	+25°C		0.8		0.8	V
		-55°C to +125°C		0.8			V
	V_{AH}, Input High Threshold	+25°C	3.0		3.0		V
		-55°C to +125°C	3.0				V
	I_A, Input Leakage Current	+25°C		1.0			μA
		-55°C to +125°C		1.0			μA
	SWITCHING CHARACTERISTICS						
	t_{ON}, Switch ON Time	+25°C		1000			ns
	t_{OFF}, Switch OFF Time	+25°C		500			ns
	POWER REQUIREMENTS						
	I^+, +15V Quiescent Current	+25°C		0.3		0.5	mA
		-55°C to +125°C		0.3			mA
	I^-, -15V Quiescent Current	+25°C		0.3		0.5	mA
		-55°C to +125°C		0.3			mA
	I_L, +5V Quiescent Current	+25°C		0.3		0.5	mA
		-55°C to +125°C		0.3			mA
	I_R, Gnd. Quiescent Current	+25°C		0.3		0.5	mA
		-55°C to +125°C		0.3			mA

TYPICAL CHARACTERISTICS	t_{ON}, Switch ON Time	25°C	370		370	ns
	t_{OFF}, Switch OFF Time	25°C	280		280	ns
	Charge Injection (2)	25°C	5		5	mV
	Off Isolation (3)	25°C	80		80	dB
	Crosstalk (3)	25°C	88		88	dB

NOTES:
1. $V_{OUT} = \pm 10V$, $I_{OUT} = 1mA$.
2. $V_{IN} = 0V$, $C_L = 10{,}000pF$.
3. $R_L = 100\Omega$, f = 100kHz, $V_{IN} = 2V_{p-p}$, $C_L = 5pF$.

7

HIO-506/507

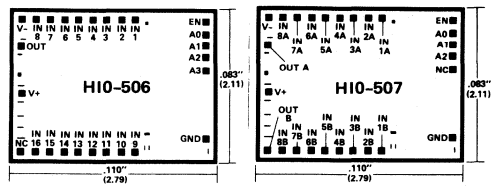
CMOS Analog Multiplexers
Single 16/Differential 8 Channel

Description

HIO-506/507 are CMOS analog multiplexers employing dielectric isolation processing for high performance and reliability. The DI process yields low leakage currents and low parasitic capacitances resulting in extremely low static errors and high throughput rates. Low output leakage (0.3nA typ.) and low channel ON resistance (170Ω typ.) assure optimum performance in low level or current mode applications. These multiplexers are TTL/CMOS compatible and require no pull-up resistors.

HIO-506 is a single-ended 16 channel multiplexer while HIO-507 is a differential 8 channel version.

Chip Layout and Dimensions



For Chip Geometries see Drawings 20, 21, page 7-52.

Specifications

ABSOLUTE MAXIMUM RATINGS

V_{EN}, V_A, Digital Input Overvoltage — V_A: V^+SUPPLY +4V; V^-SUPPLY -2V

Analog Input Overvoltage — V_D or V_S: V^+SUPPLY +2V; V^-SUPPLY -2V

Operating Temp. Range HIO-0506/7-2 -55°C to +125°C
HIO-0506/7-6 0°C to +75°C

Storage Temperature Range -65°C to +150°C

Supply Voltage Between Pads 1 and 27 40V

ELECTRICAL SPECIFICATIONS

PARAMETER	TEMPERATURE	HIO-0506/07-2 MINIMUM	HIO-0506/07-2 MAXIMUM	HIO-0506/07-6 MINIMUM	HIO-0506/07-6 MAXIMUM	UNITS
GUARANTEED CHARACTERISTICS Unless otherwise specified, Supplies = +15V, -15V; V_{AH} (Logic Level High) = +2.4V, V_{AL} (Logic Level Low) = +0.8V.						
ANALOG CHANNEL CHARACTERISTICS						
V_S, Analog Signal Range	+25°C	-15	+15	-15	+15	V
	-55°C to +125°C	-15	+15			V
R_{ON}, On Resistance (1)	+25°C		300		400	Ω
	-55°C to +125°C		400			Ω
I_S (OFF), Off Input Leakage Current	+25°C		±50		±50	nA
	-55°C to +125°C		±50			nA
I_D (OFF), Off Output Leakage Current						
HI-0506	+25°C		±500		±500	nA
	-55°C to +125°C		±500			nA
HI-0507	+25°C		±250		±250	nA
	-55°C to +125°C		±250			nA
I_D (ON), On Channel Leakage Current						
HI-0506	+25°C		±500		±500	nA
	-55°C to +125°C		±500			nA
HI-0507	+25°C		±250		±250	nA
	-55°C to +125°C		±250			nA
DIGITAL INPUT CHARACTERISTICS						
V_{AL}, Input Low Threshold	+25°C		+0.8		+0.8	V
	-55°C to +125°C		+0.8			V
V_{AH}, Input High Threshold	+25°C	+2.4		+2.4		V
	-55°C to +125°C	+2.4				V
I_A, Input Leakage Current (High or Low) (2)	+25°C		1.0		1.0	μA
	-55°C to +125°C		1.0			μA
SWITCHING CHARACTERISTICS						
t_A, Access Time	+25°C		1000			ns
t_{ON} (EN), Enable Delay (ON)	+25°C		1000			ns
t_{OFF} (EN), Enable Delay (OFF)	+25°C		1000			ns
POWER REQUIREMENTS						
I^+, Current (3)	+25°C		3.0		5.0	mA
	-55°C to +125°C		3.0			mA
I^-, Current (3)	+25°C		1.0		2.0	mA
	-55°C to +125°C		1.0			mA
I^+, Standby (4)	+25°C		3.0		5.0	mA
	-55°C to +125°C		3.0			mA
I^-, Standby (4)	+25°C		1.0		2.0	
	-55°C to +125°C		1.0			mA

TYPICAL CHARACTERISTICS					
t_A, Access Time	+25°C	300	300		ns
t_{OPEN}, Break-Before Make Delay	+25°C	80	80		ns
t_{ON} (EN), Enable Delay (ON)	+25°C	300	300		ns
t_{OFF} (EN), Enable Delay (OFF)	+25°C	300	300		ns
Settling Time (to 0.1%)	+25°C	1.2	1.2		μs
(to 0.025%)	+25°C	2.4	2.4		μs
Off Isolation (5)	+25°C	75	75		dB

NOTES:
1. V_{OUT} = ±10V, I_{OUT} = -1mA.
2. Digital inputs are MOS gates. Typical leakage is < 1nA.
3. V_{EN} = 4.0V, All V_A = 4.0V.
4. V_{EN} = 0V, All V_A = 0V.
5. V_{EN} = 0.8V, R_L = 1K, C_L = 28pF, V_S = 7Vrms, f = 500kHz.

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
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HI0-506A/507A

Overvoltage Protected CMOS Analog Multiplexer

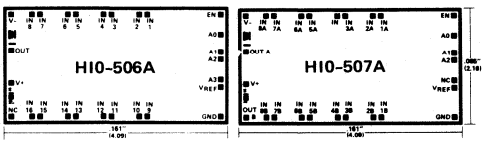
Single 16/Differential 8 Channel

Description

HI0-506A/507A are dielectrically isolated CMOS analog multiplexers featuring analog input overvoltage protection. These devices can withstand a continuous input up to 10 volts greater than either supply, which eliminates the possibilities of damage when supplies are off but input signals are present. Equally important, they can withstand brief input transient spikes of several hundred volts. These multiplexers are also TTL/CMOS compatible.

HI0-506A is a single ended 16 channel multiplexer while HI0-507A is a differential 8 channel version.

Chip Layout and Dimensions



For Chip Geometries see Drawings 22, 23 page 7-52.

Specifications

ABSOLUTE MAXIMUM RATINGS

V_{REF} to Ground, V^+ to Ground +20V

V_{EN}, V_A, Digital Input Overvoltage
- V_A: V^+SUPPLY +4V
- V_A: V^-SUPPLY -4V

Analog Overvoltage
- V_S: V^+SUPPLY +20V
- V_S: V^-SUPPLY -20V

Operating Temperature Range
- HI0-0506A/7A-2: -55°C to +125°C
- HI0-0506A/7A-6: 0°C to +75°C

Storage Temperature Range -65°C to +150°C

Supply Voltage Between Pads 1 and 27 40V

ELECTRICAL SPECIFICATIONS

	PARAMETER	TEMPERATURE	HI0-0506A/07A-2 MINIMUM	HI0-0506A/07A-2 MAXIMUM	HI0-0506A/07A-6 MINIMUM	HI0-0506A/07A-6 MAXIMUM	UNITS
GUARANTEED CHARACTERISTICS Unless otherwise specified, Supplies = +15V, -15V; V_{AH} (Logic Level High) = +4.0V, V_{AL} (Logic Level Low) = +0.8V.	ANALOG CHANNEL CHARACTERISTICS						
	V_S, Analog Signal Range	+25°C	-15	+15	-15	+15	V
		-55°C to +125°C	-15	+15			V
	R_{ON}, On Resistance (1)	+25°C		1.5		1.8	kΩ
		-55°C to +125°C		2.0			kΩ
	I_S (OFF), Off Input Leakage Current	+25°C		±50		±50	nA
		-55°C to +125°C		±50			nA
	I_D (OFF), Off Output Leakage Current HI-0506A	+25°C		±500		±500	nA
		-55°C to +125°C		±500			nA
	HI-0507A	+25°C		±250		±250	nA
		-55°C to +125°C		±250			nA
	I_D (ON), On Channel Leakage Current HI-0506A	+25°C		±500		±500	nA
		-55°C to +125°C		±500			nA
	HI-0507A	+25°C		±250		±250	nA
		-55°C to +125°C		±250			nA
	DIGITAL INPUT CHARACTERISTICS						
	V_{AL}, Input Low Threshold (TTL Drive)(2)	+25°C		0.8		0.8	V
		-55°C to +125°C		0.8			V
	V_{AH}, Input High Threshold (TTL Drive)(2)	+25°C	4.0		4.0		V
		-55°C to +125°C	4.0				V
	V_{AL} (MOS Drive) (3)	+25°C		0.8		0.8	V
	V_{AH} (MOS Drive((3)	+25°C	6.0		6.0		V
	I_A, Input Leakage Current (High or Low)	+25°C		1.0		5.0	μA
		-55°C to +125°C		1.0			μA
	SWITCHING CHARACTERISTICS						
	t_A, Access Time	+25°C		1000			ns
	t_{ON} (EN), Enable Delay (ON)	+25°C		1000			ns
	t_{OFF} (EN), Enable Delay (OFF)	+25°C		1000			ns
	POWER REQUIREMENTS						
	I^+, Current (4)	+25°C		2.0		5.0	
		-55°C to +125°C		2.0			
	I^-, Current (4)	+25°C		1.0		2.0	
		-55°C to +125°C		1.0			
	I^+, Standby (5)	+25°C		2.0		5.0	
		-55°C to +125°C		2.0			
	I^-, Standby (5)	+125°C		1.0		2.0	
		-55°C to +125°C		1.0			

TYPICAL CHARACTERISTICS	t_A, Access Time	+25°C	500		500	ns
	t_{OPEN}, Break-Before Make Delay	+25°C	80		80	ns
	t_{ON} (EN), Enable Delay (ON)	+25°C	300		300	ns
	t_{OFF} (EN), Enable Delay (OFF)	+25°C	300		300	ns
	Settling Time (to 0.1%)	+25°C	1.3		1.3	μs
	(to 0.025%)	+25°C	4.4		4.4	μs
	Off Isolation (6)	+25°C	65		65	dB

NOTES:
1. V_{OUT} = ± 10V, I_{OUT} = -100μA
2. To drive from DTL/TTL circuits, 1k pull-up resistors to +5.0V supply are recommended.
3. V_{REF} = +10V.
4. V_{EN} = +4.0V.
5. V_{EN} = 0.8V.
6. V_{EN} = 0.8V, R_L = 1k, C_L = 7pF, V_S = 3Vrms, f = 500kHz.

7

HI0-508A/509A

Overvoltage Protected CMOS Analog Multiplexer

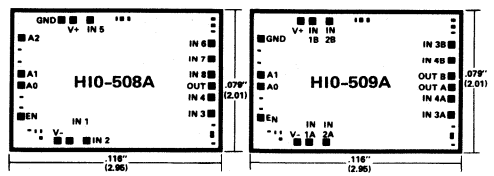
Single 8/Differential 4 Channel

Description

HI0-508A/509A are dielectrically isolated CMOS analog multiplexers featuring analog input overvoltage protection. These devices can withstand a continuous input up to 10 volts greater than either supply, which eliminates the possibilities of damage when supplies are off but input signals are present. Equally important, they can withstand brief input transient spikes of several hundred volts. These multiplexers are also TTL/CMOS compatible.

HI0-508A is a single ended 8 channel multiplexer while HI0-509A is a differential 4 channel version.

Chip Layout and Dimensions



For Chip Geometries see Drawings 24, 25, pages 7-52 & 53.

Specifications

ABSOLUTE MAXIMUM RATINGS

V_{EN}, V_A, Digital Input Overvoltage — V_A: V^+SUPPLY +4V; V^-SUPPLY -4V

Analog Input Overvoltage — V_S: V^+SUPPLY +20V; V^-SUPPLY -20V

Operating Temp. Range HI0-0509A-2 -55°C to +125°C

HI0-0509A-6 0°C to +75°C

Storage Temperature Range -65°C to +150°C

Voltage Between Supply Pads 40V

V+ to Ground 20V

ELECTRICAL SPECIFICATIONS

	PARAMETER	TEMPERATURE	HI0-0508A/09A-2 MINIMUM	HI0-0508A/09A-2 MAXIMUM	HI0-0508A/09A-6 MINIMUM	HI0-0508A/09A-6 MAXIMUM	UNITS
GUARANTEED CHARACTERISTICS Unless otherwise specified, Supplies = +15V, -15V; V_{AH} (Logic Level High) = +4.0V, V_{AL} (Logic Level Low) = +0.8V.	ANALOG CHANNEL CHARACTERISTICS						
	V_S, Analog Signal Range	+25°C	-15	+15	-15	+15	V
		-55°C to +125°C	-15	+15			V
	R_{ON}, On Resistance (1)	+25°C		1.5		1.8	kΩ
		-55°C to +125°C		1.8			kΩ
	I_S (OFF), Off Input Leakage Current	+25°C		±50		±50	nA
		-55°C to +125°C		±50			nA
	I_D (OFF), Off Output Leakage Current HI-0508A	+25°C		±250		±250	nA
		-55°C to +125°C		±250			nA
	HI-0509A	+25°C		±125		±125	nA
		-55°C to +125°C		±125			nA
	I_D (ON), On Channel Leakage Current HI-0508A	+25°C		±250		±250	nA
		-55°C to +125°C		±250			nA
	HI-0509A	+25°C		±125		±125	nA
		-55°C to +125°C		±125			nA
	DIGITAL INPUT CHARACTERISTICS						
	V_{AL}, Input Low Threshold	+25°C		0.8		0.8	V
		-55°C to +125°C		0.8			V
	V_{AH}, Input High Threshold (2)	+25°C	4.0		4.0		V
		-55°C to +125°C	4.0				V
	I_A, Input Leakage Current (High or Low)	+25°C		1.0		1.0	μA
		-55°C to +125°C		1.0			μA
	SWITCHING CHARACTERISTICS						
	t_A, Access Time	+25°C		1000			ns
	t_{ON} (EN), Enable Delay (ON)	+25°C		1000			ns
	t_{OFF} (EN), Enable Delay (OFF)	+25°C		1000			ns
	POWER REQUIREMENTS						
	I^+, Current (3)	+25°C		2.0		5.0	mA
		-55°C to +125°C		2.0			mA
	I^-, Current (3)	+25°C		1.0		2.0	mA
		-55°C to +125°C		1.0			mA
	I^+, Standby (4)	+25°C		2.0		5.0	mA
		-55°C to +125°C		2.0			mA
	I^-, Standby (4)	+25°C		1.0		2.0	mA
		-55°C to +125°C		1.0			mA
TYPICAL CHARACTERISTICS	t_A, Access Time	+25°C		500		500	ns
	t_{OPEN}, Break-Before Make Delay	+25°C		80		80	ns
	t_{ON} (EN), Enable Delay (ON)	+25°C		300		300	ns
	t_{OFF} (EN), Enable Delay (OFF)	+25°C		300		300	ns
	Settling Time (to 0.1%)	+25°C		1.2		1.2	μs
	(to 0.025%)	+25°C		3.5		3.5	μs
	Off Isolation (5)	+25°C		65		65	dB

NOTES:
1. V_{OUT} = ±10V, I_{OUT} = -100μA.
2. To drive from DTL/TTL circuits, 1kΩ Pull-up resistors to +5.0V supply are recommended.
3. V_{EN} = +4.0V.
4. V_{EN} = 0.8V.
5. V_{EN} = 0.8V, R_L = 1k, C_L = 7pF, V_S = 3Vrms, f = 500kHz.

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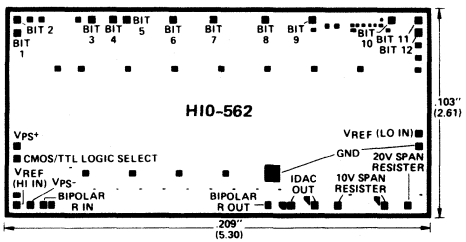
HI0-562

12 Bit High Speed Digital To Analog Converter

Description

The Harris HI0-562-6 is a monolithic, ultra-high speed, 12 bit, digital to analog converter. The HI0-562-6's fast output of 400ns max. to 0.01% is achieved using dielectric isolation processing to reduce internal parasitics for fast rise and fall times. Output glitches are minimized by incorporating equally weighted current sources switched into an R-2R ladder network for symmetrical turn ON and turn OFF times. The HI0-562-6 is especially suited for use in high speed, successive approximation analog to digital converters.

Chip Layout and Dimensions



For Chip Geometries see Drawing 26, page 7-53.

Specifications

ABSOLUTE MAXIMUM RATINGS (referred to Ground) (1)

Power Supply Inputs	$V_{PS}+$	+20V	Outputs Pins 7, 8, 10, 11	$\pm V_{PS}$
	$V_{PS}-$	-20V	Pin 9	$+V_{PS}$, -5V
Reference Inputs	V_{REF} (HI)	$\pm V_{PS}$	Operating Temperature Range	0°C to +75°C
	V_{REF} (LO)	0	Storage Temperature Range	-65°C to +150°C
Digital Inputs	Bits 1 - 12	-1V, +12V		
	CMOS/TTL Logic Select	-1V, +12V		

ELECTRICAL SPECIFICATIONS

	PARAMETER	CONDITIONS	HI0-562-6 MINIMUM	HI0-562-6 MAXIMUM	UNITS
GUARANTEED CHARACTERISTICS @ +25°C, $V_{PS}+$ = +5V, $V_{PS}-$ = -15V, V_{REF} = +10V; pin 2 tied to pin 12 unless otherwise noted.	INPUT CHARACTERISTICS				
	Digital Inputs	Bit ON "Logic 1"			
	TTL Input Voltage (2)	Bit OFF "Logic 0"			
	Logic "1"	0°C to +75°C	2.0		V
	Logic "0"	Pin 2 tied to pin 12		0.8	V
	TTL Input Current (2)				
	Logic "1"			100	nA
	Logic "0"			-100	μA
	CMOS Input Voltage	Pin 2 tied to pin 1			
	Logic "1" (5)	+4.75V ≤ $V_{PS}+$ ≤ +12V	0.7 $V_{PS}+$		V
	Logic "0"	0°C to +75°C		0.3 $V_{PS}+$	V
	CMOS Input Current				
	Logic "1"			100	nA
	Logic "0"			-100	μA
	TRANSFER CHARACTERISTICS				
	Resolution	0°C to 75°C	12		Bits
	Settling Time to ± ½LSB (4)	All bits ON to OFF or OFF to ON		400	ns
	Compliance Limit	0°C to +75°C	-3	+10	V
	POWER REQUIREMENTS				
	$V_{PS}+$ (3)	0°C to +75°C	4.75	15	V
	$V_{PS}-$		13.50	16.5	V
TYPICAL CHARACTERISTICS	Reference Input				
	Input Resistance			8 k	Ω
	Input Voltage	I_{OUT} = 5mA (± 20%)		+10	V
	Output Noise	0.1 to 10Hz (all Bits ON)		30	V(p-p)
		0.1 to 5MHz (all Bits ON)		100	V(p-p)
	Output Current				
	Unipolar			-5	mA
	Bipolar			± 2.5	mA
	Resistance			1000	Ω
	Capacitance			20	pF
	Output Voltage Ranges				
	Unipolar	Using external op amp and internal scaling resistors		0 to +5	V
				0 to +10	V
	Bipolar			± 2.5	V
				± 5	V
				± 10	V
	$I_{PS}+$			11	mA
	$I_{PS}-$			33	mA

NOTES:
1. Ab. max. ratings are limiting values, applied indiv.'ly, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. $V_{PS}+$ is ± 5% for HI0-562-6.
3. Max. V_{PS} is +12V for high level logic only, i.e., when pin 2 is tied to pin 1.
4. Settling time is the time required for the output to settle within the specified error band for any input code transaction. It is usually specified for a full scale or major carry transition. This characteristic is not measured on dice but is guaranteed to be within the specified limits to an LTPD of 20/3.
5. For high temp. operation (>60°C), logic power supply should not exceed 10V for accurate operation.

Recommended Die Attachment

Harris recommends epoxy die attach for mounting the HI0-562-6 chip.

7

HI0-1818A/1828A

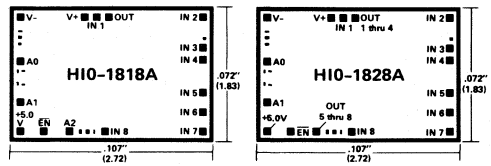
Low Resistance CMOS Analog Multiplexer
Single 8/Differential 4 Channel

Description

HI0-1818A/1828A are CMOS analog multiplexers employing dielectric isolation processing for high performance and reliability. The DI process yields low leakage currents and low parasitic capacitances resulting in extremely low static errors and high throughput rates. Low output leakage (0.1nA typ.) and low channel ON resistance (250Ω typ.) assure optimum performance in low level or current mode applications. These multiplexers are TTL/CMOS compatible.

HI0-1818A is a single ended 8 channel multiplexer while HI0-1828A is a differential 4 channel version.

Chip Layout and Dimensions



For Chip Geometries see Drawings 27, 28, page 7-53.

Specifications

ABSOLUTE MAXIMUM RATINGS

Analog Input Voltage	V^+_{SUPPLY} +2V	Supply Voltage Between Pads 14 and 15	40.0V
	V^-_{SUPPLY} -2V	Logic Supply Voltage, Pad 2	30.0V
Digital Input Voltage	V^-_{SUPPLY} to V^+_{SUPPLY}	Storage Temperature Range	-65°C to +150°C

ELECTRICAL SPECIFICATIONS

	PARAMETER	TEMPERATURE	HI0-1818A/28A-2 MINIMUM	HI0-1818A/28A-2 MAXIMUM	HI0-1818A/28A-6 MINIMUM	HI0-1818A/28A-6 MAXIMUM	UNITS
GUARANTEED CHARACTERISTICS Unless otherwise specified, Supplies = +15V, -15V.	ANALOG CHANNEL CHARACTERISTICS						
	V_S, Analog Signal Range	+25°C	-15	+15	-15	+15	V
		-55°C to +125°C	-15	+15			V
	R_{ON}, On Resistance (1)	+25°C		400		400	Ω
		-55°C to +125°C		500			Ω
	I_S (OFF), Off Input Leakage Current	+25°C		±50		±50	nA
		-55°C to +125°C		±50			nA
	I_D (OFF), Off Output Leakage Current						
	HI-1818A	+25°C		±250		±250	nA
		-55°C to +125°C		±250			nA
	HI-1828A	+25°C		±125		±125	nA
		-55°C to +125°C		±125			nA
	I_D (ON), On Channel Leakage Current						
	HI-1818A	+25°C		±250		±250	nA
		-55°C to +125°C		±250			nA
	HI-1828A	+25°C		±125		±125	nA
		-55°C to +125°C		±125			nA
	DIGITAL INPUT CHARACTERISTICS						
	V_{AL}, Input Low Threshold	+25°C		0.4		0.4	V
		-55°C to +125°C		0.4			V
	V_{AH}, Input High Threshold (2)	+25°C	4.0		4.0		V
		-55°C to +125°C	4.0				V
	I_A, Input Leakage Current	+25°C		1.0		1.0	μA
		-55°C to +125°C		1.0			μA
	POWER REQUIREMENTS						
	I+, Current	+25°C		0.5		1.0	mA
		-55°C to +125°C		0.5			mA
	I⁻, Current	+25°C		1.0		2.0	mA
		-55°C to +125°C		1.0			mA
	I_L, Current	+25°C		1.0		2.0	mA
		-55°C to +125°C		1.0			mA
TYPICAL CHARACTERISTICS	t_A, Access Time (3)	+25°C		350		350	ns
	t_{OPEN}, Break-Before Make Delay	+25°C		100		100	ns
	Settling Time (to 0.1%)	+25°C		1.08		1.08	μs
	(to 0.025%)	+25°C		2.8		2.8	μs

NOTES:
1. V_{OUT} = ±10V, I_{OUT} = -1mA.
2. To drive from DTL, TTL circuits, 1k pull-up resistors to +5.0V supply are recommended.
3. Time measured to 90% of final output level. V_{OUT} = 5.0V to -5.0V, Digital inputs = 0V to +4.0V.

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
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HIO-1840

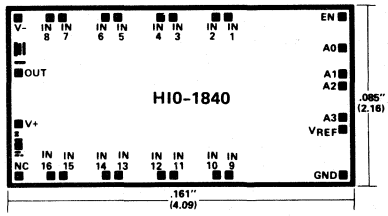
16 Channel CMOS Analog Multiplexer With High-Z Analog Input Protection

Description

HIO-1840 is a dielectrically isolated CMOS analog multiplexer featuring high-Z analog input protection. It is designed to provide a high input impedance to the analog source if device power fails (open) or the analog signal voltage exceeds the supply rails during powered operation. A high impedance exists between active and inactive devices preventing any interaction. Channel selection is controlled by a 4-bit binary address plus an enable-inhibit input for controlling the ON/OFF operation. All digital inputs have electro-static discharge protection.

HIO-1840 is a single ended 16 channel multiplexer.

Chip Layout and Dimensions



For Chip Geometries see Drawing 29, page 7-53.

Specifications

ABSOLUTE MAXIMUM RATINGS

Supply Voltage between Pads 1 and 27 +40V
V_{REF} to Ground +20V
Operating Temp. HIO-1840-2 -55°C to +125°C
Storage Temperature Range -65°C to +150°C

V_{EN}, V_A, Digital Input Overvoltage V_A { V+SUPPLY + 4V ; V-SUPPLY - 4V }
Analog Input Overvoltage V_S { V+SUPPLY +10V ; V-SUPPLY -10V }

ELECTRICAL SPECIFICATIONS

GUARANTEED CHARACTERISTICS Unless otherwise specified, Supplies = ±15V; V_{REF} = +5V; V_{AH} (Logic Level High) = 40V, V_{AL} (Logic Level Low) = +0.8V.

PARAMETER	TEMPERATURE	HIO-1840-2 MINIMUM	HIO-1840-2 MAXIMUM	UNITS
ANALOG CHAN. CHARACTERISTICS				
V_S, Analog Signal Range	-55°C to +125°C	-5	+15	V
R_{ON}, On Resistance (1) V_{IN} = +15V	-55°C to +125°C		1.0	kΩ
V_{IN} = -5V	-55°C to +125°C		5.0	kΩ
I_S (OFF), Off Input Leakage Current	-55°C to +125°C		±100	nA
I_S (OFF), with Power Off (2)	-55°C to +125°C		±100	nA
I_D (OFF), Off Output Leakage Current	-55°C to +125°C		±1000	nA
I_D(OFF) or I_S(OFF) with Input Overvoltage Applied (3)	-55°C to +125°C		±1000	nA
I_D (ON), On Leakage Current	-55°C to +125 °C		±1000	nA
DIGITAL INPUT CHARACTERISTICS				
V_{AL}, Input Low Threshold (TTL Drive)	-55°C to +125°C		0.8	V
V_{AH}, Input High Threshold (TTL Drive)(4)	-55°C to +125°C	4.0		V
V_{AL} (MOS Drive) (5)	+25°C		0.8	V
V_{AH} (MOS Drive) (5)	+25°C	6.0		V
I_A, Input Leakage Current (High or Low)	-55°C to +125°C		1.0	μA
SWITCHING CHARACTERISTICS				
t_A, Access Time	+25°C		1000	ns
t_{OPEN}, Break Before Make Delay	+25°C	20		ns
t_{ON}, Enable Delay (ON)	+25°C		1000	ns
t_{OFF} (EN), Enable Delay (OFF)	+25°C		1000	ns
POWER REQUIREMENTS				
P_D, Power Dissipation (6,7)	+25°C		15	mW
I^+, Current (6)	-55°C to +125°C		0.5	mA
I^-, Current (6)	-55°C to +125°C		0.5	mA
I^+, Standby (7)	-55°C to +125°C		0.5	mA
I^-, Standby (7)	-55°C to +125°C		0.5	mA

TYPICAL CHARACTERISTICS

t_A, Access Time	+25°C	500	ns
t_{OPEN}, Break Before Make Delay	+25°C	80	ns
t_{ON} (EN), Enable Delay (ON)	+25°C	300	ns
t_{OFF} (EN), Enable Delay (OFF)	+25°C	300	ns
Settling Time (to 0.1%)	+25°C	1.2	μs
(to 0.025%)	+25°C	4.1	μs
Off Isolation (8)	+25°C	65	dB

NOTES:
1. I_{OUT} = 1mA.
2. All supplies (V^+, V^-, +5V) and digital inputs (A_{0-3}, EN) opened. Analog input ±10V.
3. Analog overvoltage = ±20V.
4. To drive from DTL/TTL circuits 1k pull-up resistors to +5.0V supply are recommended.
5. V_{REF} = +10V.
6. V_{EN} = 0.8V.
7. V_{EN} = 4.0V.
8. V_{EN} = 4.0V, R_L = 1k, C_L = 7pF, V_S = 3Vrms, f = 500kHz.

7

HA0-2420/2425

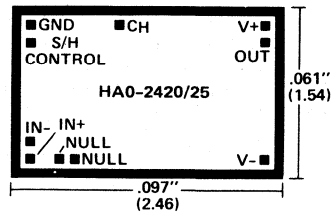
Fast Sample And Hold

Description

HA0-2420 and HA0-2425 are high performance sample and hold circuits consisting of an operational amplifier whose output is in series with an ultra-low leakage analog switch and a MOSFET input unity gain amplifier. With an external holding capacitor connected to the switch output, a versatile high performance sample and hold or track and hold circuit is formed.

Accuracy to better than 0.01% is achievable over the temperature range. Fast acquisition is coupled with superior droop characteristics, even at high temperatures. High slew rate, wide bandwidth, and low acquisition time produce excellent dynamic characteristics.

Chip Layout and Dimensions



For Chip Geometries see Drawing 30, page 7-53.

Specifications

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Between Pads 5 and 9	40V	Operating Temperature Range	
Differential Input Voltage	± 30V	HA0-2420-2	$-55^{0}C \leq T_A \leq +125^{0}C$
Digital Input Voltage (Pad 14)	+8V, -15V	HA0-2420-6	$0^{0}C \leq T_A \leq 75^{0}C$
Output Current	Short Circuit Protected	Storage Temperature Range	$65^{0}C \leq T_A \leq 150^{0}C$

ELECTRICAL SPECIFICATIONS

GUARANTEED CHARACTERISTICS Unless otherwise specified, Supplies = +15, -15; C_H = 1000pF; Digital Input V_{IL} = +0.8V (Sample), V_{IH} = +2.0V (Hold)

GUARANTEED CHARACTERISTICS	TEMPERATURE	HA0-2420-2 MINIMUM	HA0-2420-2 MAXIMUM	HA0-2425-6 MINIMUM	HA0-2425-6 MAXIMUM	UNITS
INPUT CHARACTERISTICS						
Offset Voltage	+25°C		4		6	mV
	0°C to +125°C		6			mV
Bias Current	+25°C		200		200	nA
	0°C to +125°C		400			nA
Offset Current	+25°C		50		50	nA
	0°C to +125°C		100			nA
Common Mode Range	+25°C	± 10		± 10		V
	0°C to +125°C	± 10				V
TRANSFER CHARACTERISTICS						
Large Signal Voltage Gain (1, 4)	+25°C	25K		25K		V/V
	0°C to +125°C	25K				V/V
Common Mode Rejection (2)	+25°C	80		74		dB
	0°C to +125°C	80				dB
OUTPUT CHARACTERISTICS						
Output Voltage Swing (1)	+25°C	± 10		± 10		V
	0°C to +125°C	+ 10				V
Output Current	+25°C	± 10		± 10		mA
DIGITAL INPUT CHARACTERISTICS						
Digital Input Current (V_{IN} = 0V)	+25°C		0.8		0.8	mA
	0°C to +125°C		0.8			mA
Digital Input Current (V_{IN} = +5.0V)	+25°C		20		20	μA
	0°C to +125°C		20			μA
Digital Input Voltage (Low)	+25°C		0.8		0.8	V
	0°C to +125°C		0.8			V
Digital Input Voltage (High)	+25°C	2.0		2.0		V
	0°C to +125°C	2.0				V
SAMPLE/HOLD CHARACTERISTICS						
Drift Current	+25°C		1.0		1.0	nA
	0°C to +125°C		10			nA
Charge Transfer	+25°C		20		20	pc
POWER SUPPLY CHARACTERISTICS						
Supply Current	+25°C		5.0		5.0	mA
Power Supply Rejection Ratio	+25°C		80		74	dB
	0°C to +125°C		80			dB

TYPICAL CHARACTERISTICS

Input Resistance	+25°C	10	10		MΩ
Gain Bandwidth Product (3)	+25°C	2	2		MHz
Full Power Bandwidth (3, 4)	+25°C	70	70		kHz
Rise Time (3, 5)	+25°C	100	100		ns
Overshoot (3, 5)	+25°C	20	20		%
Slew Rate (3, 6)	+25°C	5	5		V/μs
Acquisition Time (to 0.1%, 10V Step)	+25°C	4	4		μs
(to .01%, 10V Step)	+25°C	5	5		μs
Aperture Delay	+25°C	50	50		ns
Aperture Uncertainty	+25°C	5	5		ns

NOTES:
1. R_L = 2kΩ.
2. V_{CM} = ± 10VDC.
3. A_V = +1, R_L = 2kΩ, C_L = 50pF.
4. V_{OUT} = 20V peak to peak.
5. V_{OUT} = 400mV peak to peak.
6. V_{OUT} = 10.0V peak to peak.

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
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HC0-55516/55532

All Digital Continuously Variable Slope Delta Modulator (CVSD)

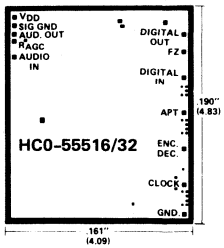
Description

HC0-55516 and HC0-55532 are half duplex modulator/demodulator CMOS integrated circuits used to convert voice signals into serial NRZ digital data, and to reconvert that data into voice. The conversion is by delta modulation, using the continuously variable slope (CVSD) method of companding.

While signals are compatible with other CVSD circuits, internal design is unique. The analog loop filters have been replaced by digital filters, using very low power, and requiring no external timing components.

The HC0-55516 is optimized for a 16K bits/sec data rate usable down to 9K bits/sec, while the HC0-55532 is optimized for 32K bits/sec, usable up to 64K bits/sec.

Chip Layout and Dimensions



For Chip Geometries see Drawing 31, page 7-54.

Specifications

ABSOLUTE MAXIMUM RATINGS

Voltage at any pad	-3.0V to V_{DD} +0.3V	Operating Temperature Range	
Maximum V_{DD} Voltage	+7.0V	HC0-55516/32-6	0°C to +75°C
Operating V_{DD} Range	+5.0V to +7.0V	Storage Temperature Range	-65°C to +150°C

ELECTRICAL SPECIFICATIONS

V_{DD} = 6.0V, Bit Rate = 16kb/s for HC-55516, Bit Rate = 32kb/s for HC-55532.

PARAMETER	TEMPERATURE	HC0-55516/32-6 MINIMUM	HC0-55516/32-6 TYPICAL	HC0-55516/32-6 MAXIMUM	UNITS
Audio Input Voltage (4)	+25°C		0.5	1.4	Vrms
Audio Output Voltage (5)	+25°C		0.5	1.4	Vrms
Audio Input Impedance (6)	+25°C		100		kΩ
Audio Output Impedance (7)	+25°C		100		kΩ
Transfer Gain (8)	+25°C	-0.5		+0.5	dB
Supply Voltage	+25°C	+5.0		+7.0	V
Supply Current	+25°C		1.0		mA
Digital "1" Input (2)	+25°C		4.5		V
Digital "0" Input (2)	+25°C		1.5		V
Digital "1" Output (3)	+25°C		5.5		V
Digital "0" Output (3)	+25°C		0.5		V
Step Size Ratio 55516 (10)	+25°C		24		dB
55532 (10)	+25°C		18		dB
Resolution 55516 (11)	+25°C		0.1		%
55532 (11)	+25°C		0.2		%
Minimum Step Size 55516 (12)	+25°C		0.2		%
55532 (12)	+25°C		0.4		%
Quieting Pattern Amplitude 55516 (15)	+25°C		12		mV (p - p)
55532 (15)	+25°C		24		mV (p - p)
AGC Treshold (16)	+25°C		0.5		F.S.
Clamping Threshold (17)	+25°C		0.75		F.S.
AC CHARACTERISTICS					
Clock Bit Rate (1)	+25°C	0		64	kb/s
Clock Duty Cycle	+25°C	30		70	%
Syllabic Time Constant (9)	+25°C		4.0		mS
L. P. Filter Time Constant 55516 (9)	+25°C		0.94		mS
55532 (9)	+25°C		0.47		mS
Signal/Noise Ratio	+25°C			Table 1	

See NOTES on following page.

7

NOTES:

1. There is one NRZ data bit per clock period. Clock must be phased with digital data such that a positive clock transition occurs in the middle of each received data bit; i.e., the transmitter and receiver clock are in phase.

2. Logic inputs are CMOS compatible at supply voltage and are diode protected. Digital data input is NRZ at clock rate.

3. Logic outputs are CMOS compatible at supply voltage and withstand short-circuits to V_{DD} or ground. Digital data output is NRZ and changes with negative clock transitions.

4. Recommended voice input range for best voice performance.

5. May be used for side-tone in encode mode.

6. Should be externally AC coupled. Presents 100 Kilohms in series with $V_{DD}/2$.

7. Presents 100 Kilohms in series with recovered audio voltage. Zero-signal references is $V_{DD}/2$.

8. Unloaded, for linear signals.

9. Note that filter time constants are inversely proportional to clock rate.

10. Step size compression ratio of the syllabic filter is defined as the ratio of the filter output, with an equal 1-0 bit density input to the filter, to its minimum output.

11. Minimum quantization voltage level expressed as a percentage of supply voltage.

12. The minimum step size between levels is twice the resolution.

13. For large signal amplitudes or high frequencies, the encoder may become slope-overloaded. Figure 1 shows the frequency response at various signal levels,measured with a 3kHz low-pass filter having a 130dB/octave roll-off to -50dB. See Table II.

14. Table I shows the SNR under various conditions, using the output filter described in 13 (above) at a bit rate of 16Kb/s. See Table II.

15. The "quieting" pattern or idle-channel audio output steps at one-half the bit rate, changing state on negative clock transitions.

16. A logic "0" will appear at the AGC output pin when the recovered signal reaches one-half of full-scale value (positive or negative).

17. The recovered signal will be clamped, and the computation will be inhibited, when the recovered signal reaches three-quarters of full-scale value, and will unclamp when it falls below this value (positive or negative).

TABLE I

INPUT FREQUENCY Hz	INPUT AMPLITUDE mV rms	OUTPUT SNR dB MIN.
300	1400	20
300	45	15
1000	500	14
1000	16	9

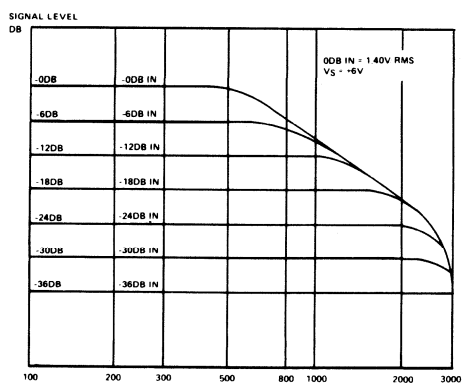


Figure 1 – Transfer Function for CVSD at 16KB

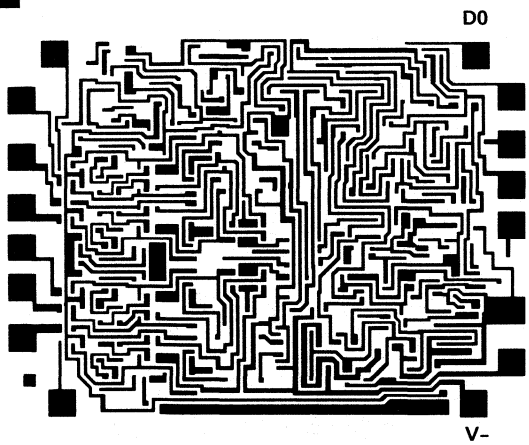
TABLE II

INPUT FILTER FREQUENCY RESPONSE		OUTPUT FILTER FREQUENCY RESPONSE	
FREQUENCY	RELATIVE OUTPUT	FREQUENCY	RELATIVE OUTPUT
100Hz	0±0.5dB	100Hz to 1500Hz	0±1.5dB
200Hz	0±0.1dB	1500Hz to 3000Hz	0±2.5dB
1000Hz	0±0.1dB	3800Hz to 100KHz	Less Than -45dB
3000Hz	-3±0.5dB		
9000Hz	-20±2.0dB		

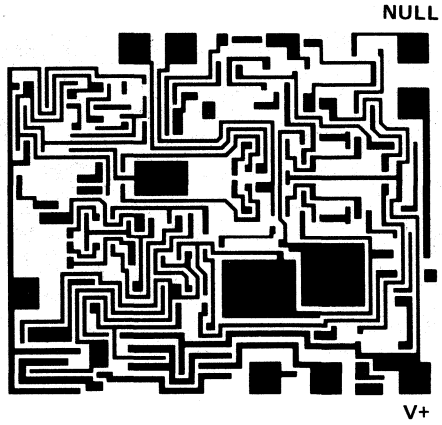
	Drawing No.		Drawing No.
HA0-2400/05	1	HI0-5047	17
HA0-2502/05	2	HI0-5049	18
HA0-2512/15	3	HI0-5051	19
HA0-2522/25	4	HI0-506	20
HA0-2602/05	5	HI0-507	21
HA0-2622/25	6	HI0-506A	22
HA0-2650/55	7	HI0-507A	23
HA0-2700/05	8	HI0-508A	24
HA0-2720/25	9	HI0-509A	25
HA0-2730/35	10	HI0-562	26
HA0-4602/05	11	HI0-1818A	27
HA0-4622/25	12	HI0-1828A	28
HA0-4741	13	HI0-1840	29
HI0-200	14	HA0-2420/25	30
HI0-201	15	HC0-55516/32	31
HI0-5046	16		

NOTE: All chip geometries are top view.

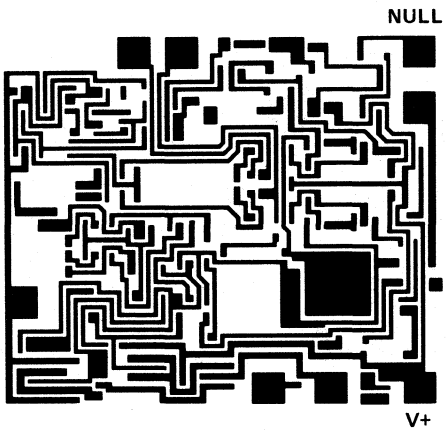
1 HA0-2400/05



2 HA0-2502/05



3 HA0-2512/15



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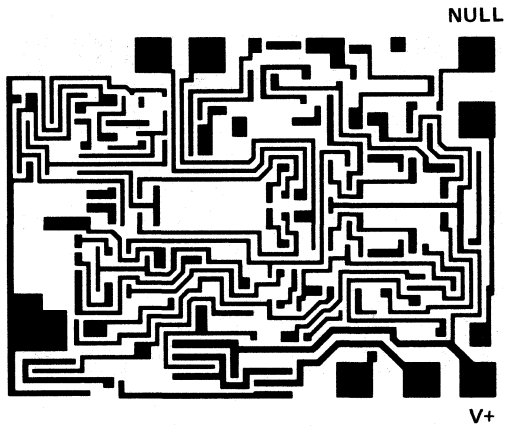

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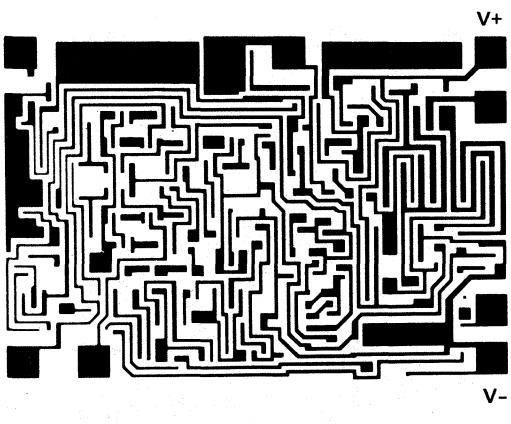

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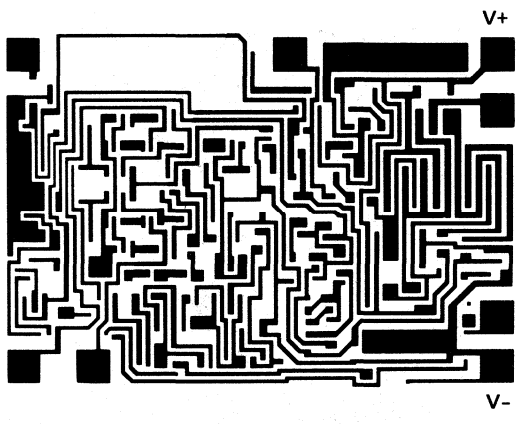

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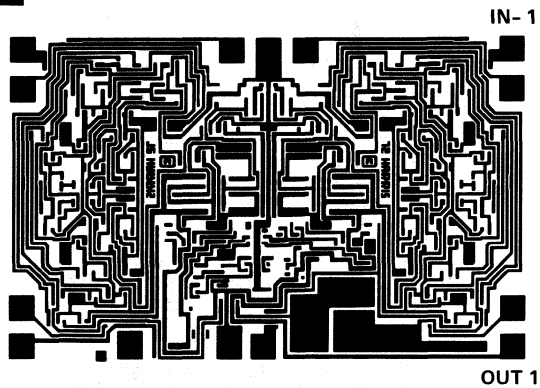
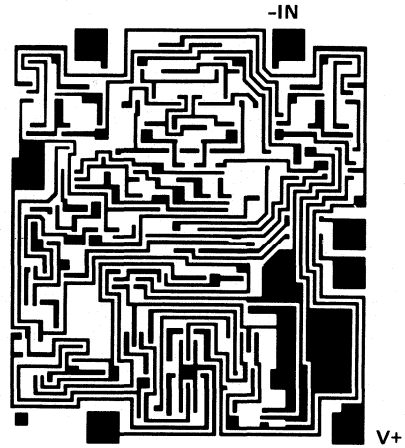
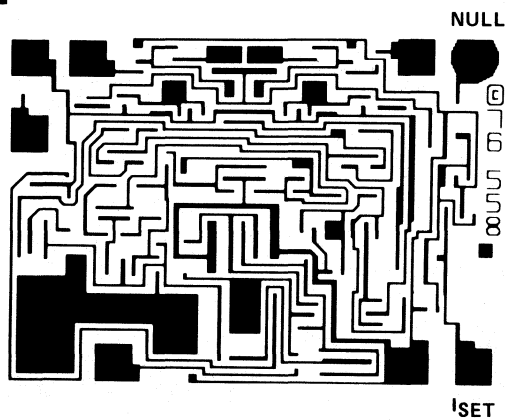


8 HA0-2700/05



9 HA0-2720/25



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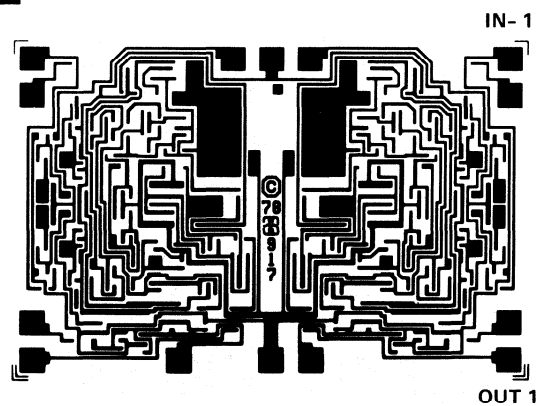

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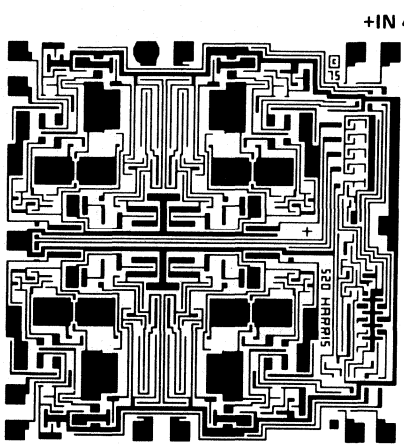
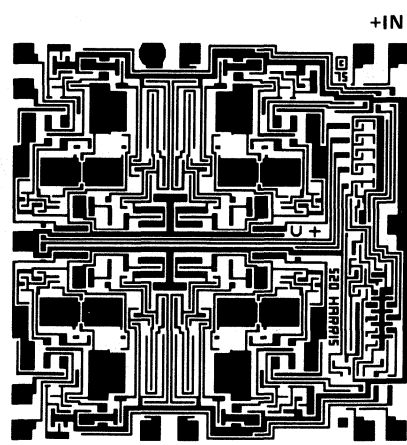
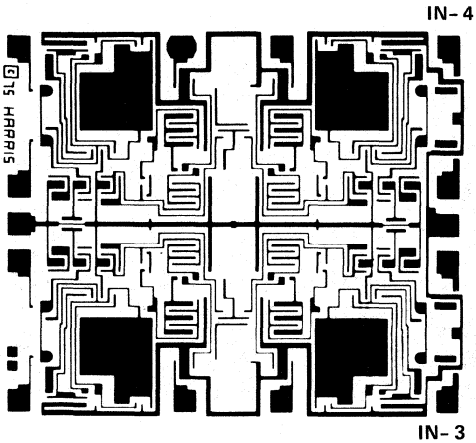


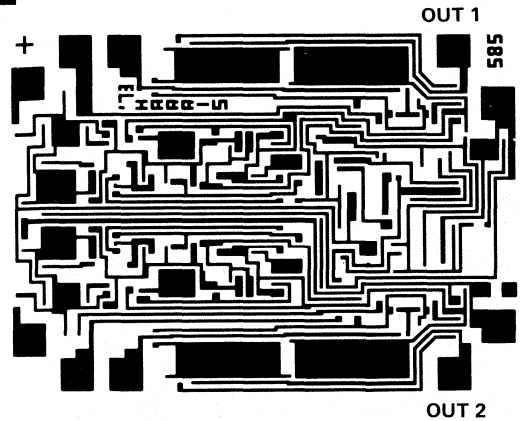
12 HA0-4622/25



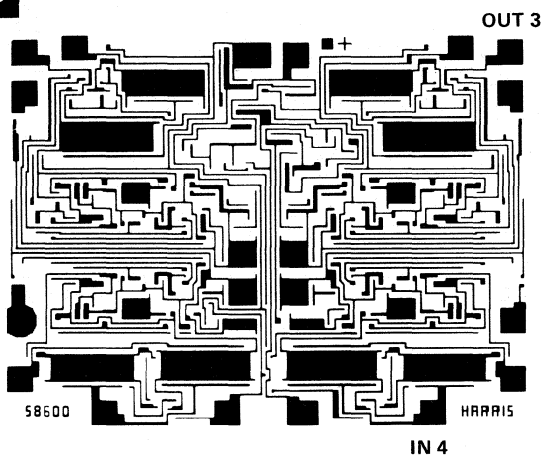
13 HA0-4741



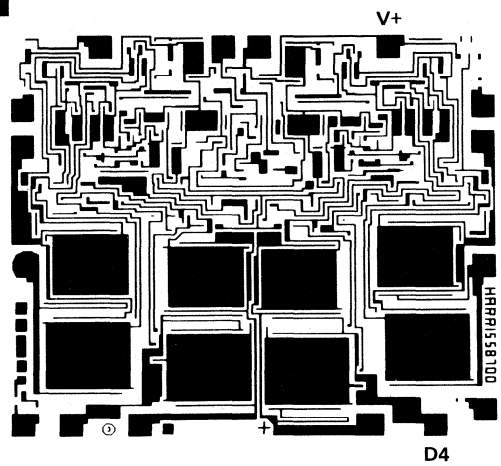
14 HI0-200



15 HI0-201



16 HI0-5046



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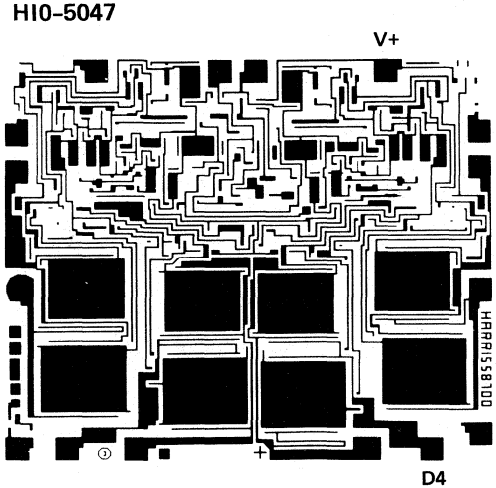

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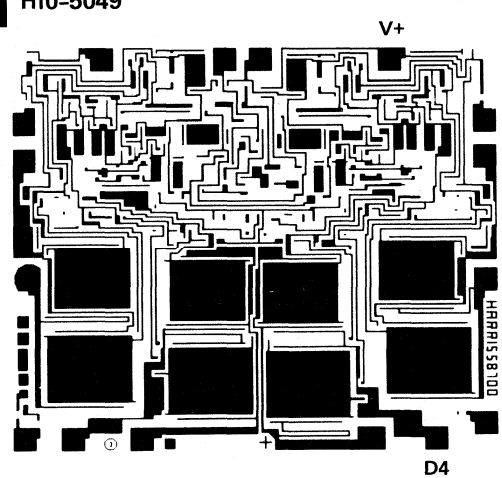

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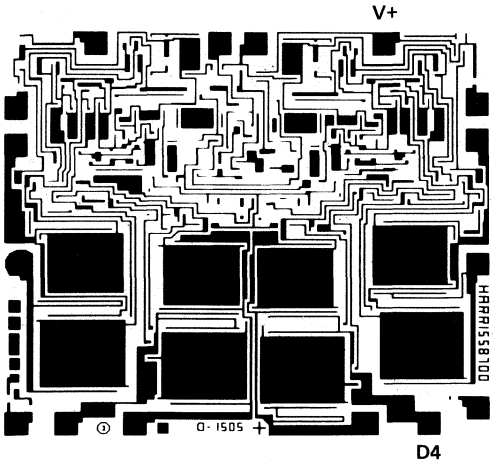

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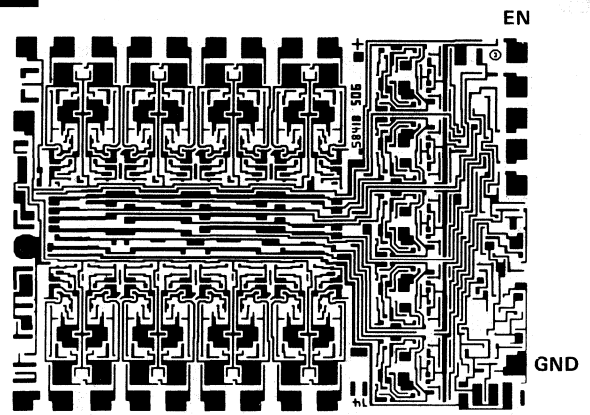
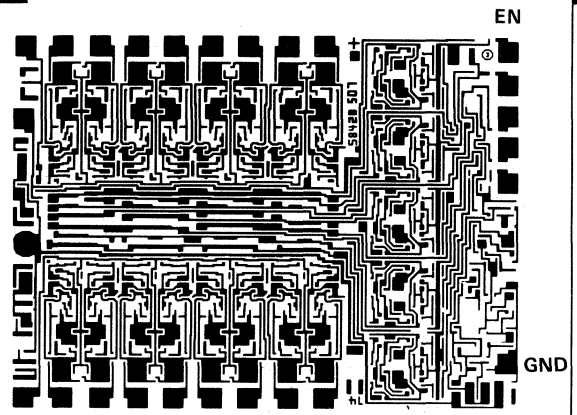
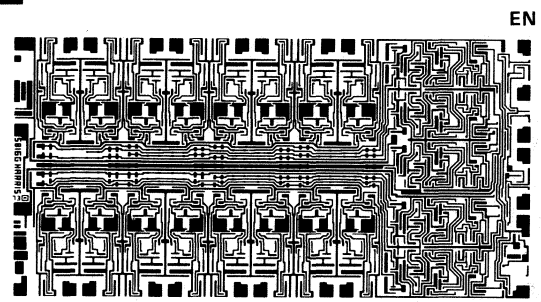


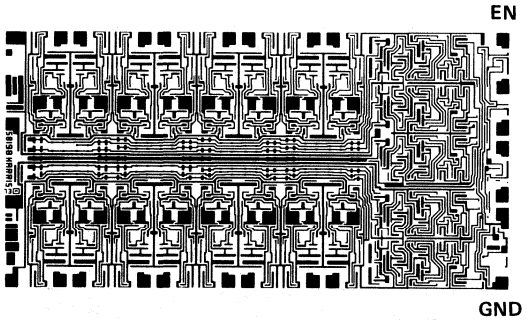
21 HI0-507



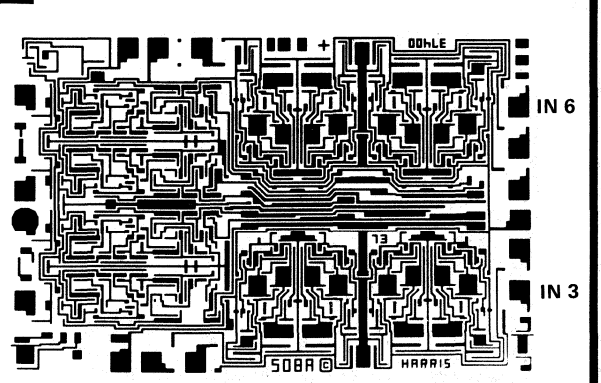
22 HI0-506A



23 HI0-507A



24 HI0-508A



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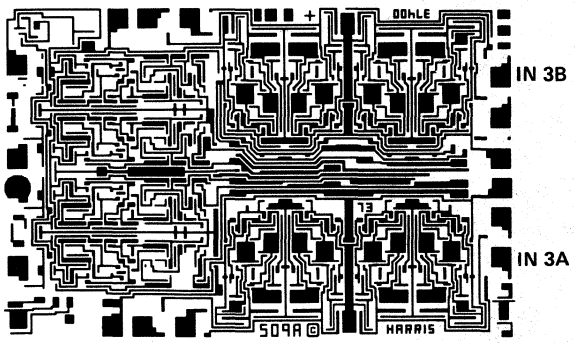
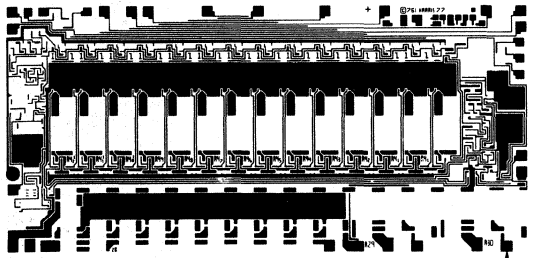
25 HI0-509A



26 HI0-562

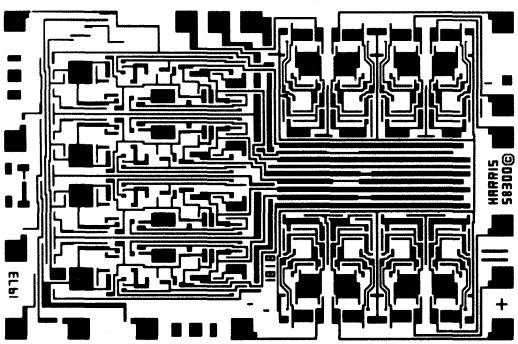
BIT 11



20V SPAN RESISTOR

27 HI0-1818A

IN 2



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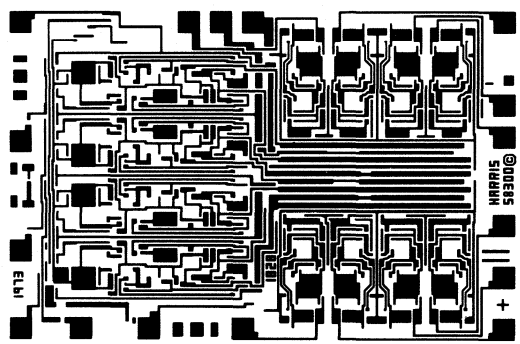
28 HI0-1828A

IN 2



IN 7

29 HI0-1840

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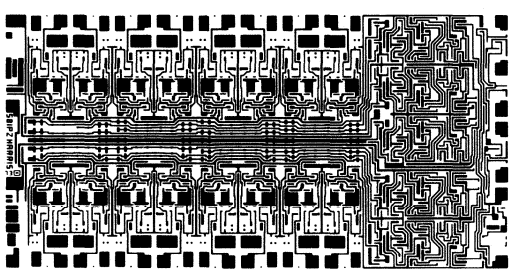
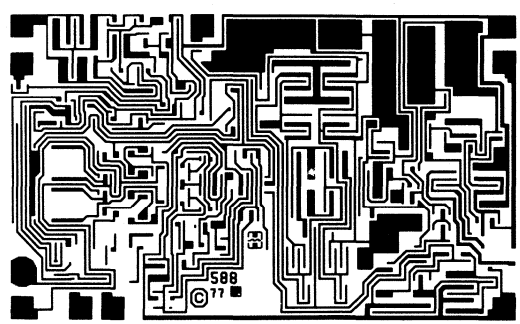


GND

30 HA0-2420/25

V+



V-

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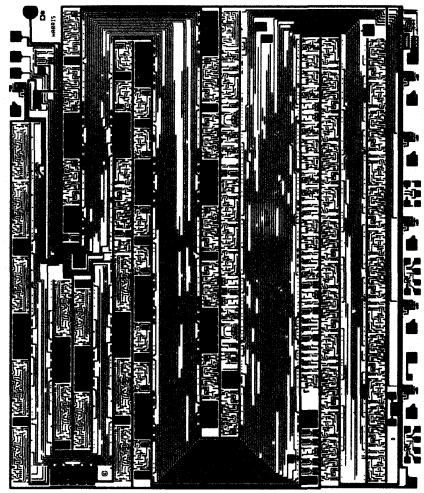

DIGITAL OUT
GND

Harris
Quality and Reliability Programs

DASH 8 Program

MIL-STD-883
OFF-THE-SHELF DELIVERY

MIL-STD-883/MIL-M-38510 MIL-Q-9858A

INTRODUCTION

STATEMENT OF SCOPE

This section establishes the detail requirements for Harris' Circuits screened and tested under the Product Assurance Program.

The Harris DASH 8 Devices pass the screening requirements of the latest issue of MIL-STD-883, Method 5004, Class B, and the requirements as specified in this document. Included in this Section are the quality standards and screening methods for commercial parts which must perform reliably in the field.

APPLICABLE DOCUMENTS

The following Military documents form a part of this section to the extent referenced herein and provide the foundation for Harris Products Assurance Program.

MIL-M-38510	"General Specification of Microcircuits"
MIL-STD-883	"Test Methods and Procedures for Microelectronics"
NASA Publication 200-3	"Inspection System Provisions"

Harris maintains a Product Assurance Program (PAP) using MIL-M-38510 as a guide. Harris Product Assurance Program assures compliance with the requirements and quality standards of control drawings and the requirements of this specification.

The DASH 8 Program will also be found useful by those Harris customers who must generate their own procurement specifications. Use of the enclosed Harris Standard Test Tables, Test Parameters, and Burn-In Circuits will aid in reducing specification negotiation time.

PRODUCT ASSURANCE AT HARRIS

Our Product Assurance Department strives to assure that the quality and reliability of products shipped to customers is of a high quality level and consistent with customer requirements. During product processing, there are several independent visual and electrical checks performed by Quality Assurance personnel.

Prior to shipment, a final inspection is performed at Quality Assurance Plant Clearance to insure that all requirements of the purchase order and customer specifications are met. The system and procedures used and implemented are in accordance with MIL-M-38510, MIL-STD-883, MIL-C-45662 and MIL-I-45208.

The Harris Semiconductor Reliability and Quality Manual which is available upon request, describes the total function and policies of the organization to assure product reliability and quality.

HARRIS SEMICONDUCTOR DASH 8 PRODUCT FLOW
MIL-M-38510/MIL-STD-883, METHOD 5004 CLASS B

100% SCREENING PROCEDURE

	SCREEN	MIL-STD-883 METHOD/COND.
1	Internal Visual	2010 Cond. B.
2	Stabilization Bake	1008 Cond. C (24 hrs. minimum)
3	Temperature Cycling	1010 Cond. C
4	Constant Acceleration	2001 Cond. E; Y1 plane
5	Seal: (A) Fine (B) Gross	1014 Cond. A or B 1014 Cond. C
6	Initial Electrical	Harris Specifications
7	Burn-In Test	1015, 160 hrs. @ 125°C (or equivalent) (Burn-In circuits enclosed)
8	Final Electrical 100% go-no-go	Tested at Worst Case Operating Conditions
9	External Visual	2009 Sample Inspection
10	Lot Acceptance	Table I, Group A Elect. Tests

Note:

Traceability: All devices are assigned date code identification that provides traceability back to the inspection lot.

Branding: All devices are branded with the HX-XXXX-8 and EIA date code.

Aged Products: Product that has been held for more than 24 months will be reinspected prior to shipment to group A inspection requirements.

Additional Requirements: Attributes data will be supplied on Group A Lot Acceptance upon request.

Generic data from Harris' Reliability Add-On Program is available upon request. The objective of Harris Reliability Add-On Program is to provide a continuous life and environmental monitor for all products families in manufacturing. This program provides life test performance results to fullfill reliability data requirements and to verify package integrity. The Reliability Add-On Program is supplemental to customer funded Lot Qualification.

For customers desiring Lot Qualification, Harris Semiconductor will perform Group A, B, C and D inspections to MIL-STD-883, Method 5005 as defined herein for an additional charge.

DASH 7 Program

HIGH RELIABILITY COMMERCIAL PRODUCTS OFF-THE-SHELF DELIVERY

INTRODUCTION

The HARRIS DASH 7 High Reliability Commercial Products program extends HARRIS processing for Hi-Rel military components to standard commercial products to provide improved levels of quality and reliability. DASH 7 is offered on Linear and Data Acquisition products in hermetic cans and dual-in-line packages.

DASH 7 uses procedures and documents described in the DASH 8 military products program with minor modifications applicable to commercial devices.

The DASH 7 program is designed to reduce field service costs and incoming test requirements on commercial parts.

Information on availability and cost of DASH 7 processing can be obtained through HARRIS sales representatives.

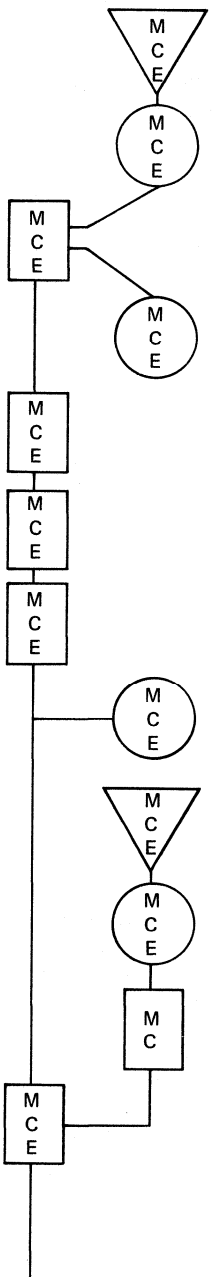
HARRIS SEMICONDUCTOR DASH 7 PRODUCT FLOW
MIL-M-38510/MIL-STD-883, METHOD 5004 CLASS B
EXCEPT: T_A = 0°C TO +75°C & BURN-IN = 96 HRS

100% SCREENING PROCEDURE

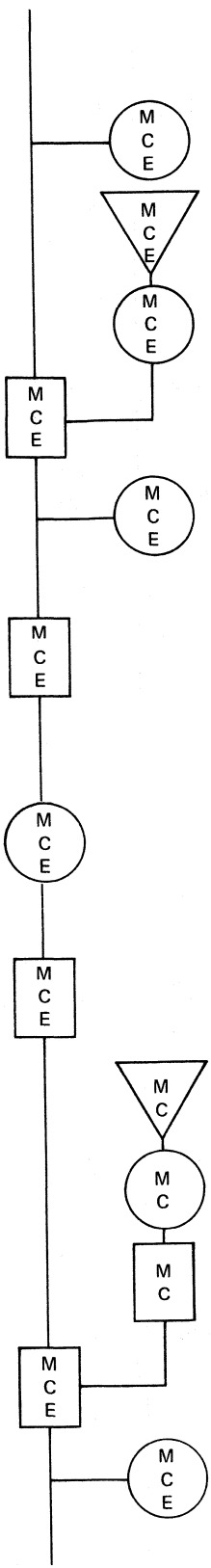
	SCREEN	MIL-STD-883 METHOD/COND.
1	Internal Visual	2010 Cond. B.
2	Stabilization Bake	1080 Cond. C (24 hrs minimum)
3	Temperature Cycling	1001 Cond. C
4	Constant Acceleration	2001 Cond. E; Y1 plane
5	Seal: Ⓐ Fine Ⓑ Gross	1014 Cond. A or B 1014 Cond. C2, no vacuum pre-cond. Step 2.
6	Initial Electrical	Harris Specifications
7	Burn-In Test	1015, 96 hrs. @ 125°C (or equivalent) (Burn-In circuits enclosed)
8	Final Electrical 100% go-no-go	Tested at worst case operating condition Functional tests per Table 1
9	External Visual	2009 Sample Inspection
10	Lot Acceptance	Table 1, Group A Elect. Tests.

Branding: All devices are branded with the HX-XXXX-7 and EIA date code.

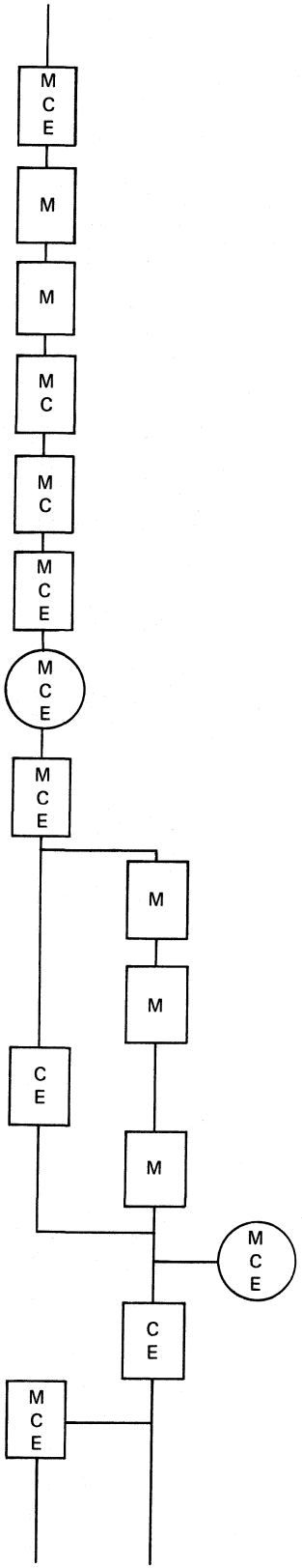
Standard Products Screening and Inspection Procedure



OPER. SEQ.	OPER. DESCRIPTION	PRODUCT CATEGORIES		
		MIL (M)	COMM (C)	EPOXY (E)
	Incoming Material Silicon and Chemical Procurement.	X	X	X
	Q.C. Incoming Inspection. Materials are Inspected for Conformance to Specified Requirements.	X	X	X
	Manufacturing Wafer Fabrication	X	X	X
	QC • DIH_2O & Gas Monitor • SEM Process Control • Wafer Process Control	X	X	X
	Manufacturing, Wafer Electrical Probe (100%)	X	X	X
	Manufacturing, Wafer Scribe, Break (100%)	X	X	X
	Manufacturing Dice Screen (100%)	X	X	X
	QA Dice Inspection Control	X	X	X
	Preform Procurement	X	X	N/A
	Package Procurement	X	X	N/A
	Leadframe Procurement			X
	Epoxy Compound Procurement			X
	Q.C. Preform Inspection	X	X	N/A
	Q.C. Package Inspection	X	X	N/A
	Q.C. Leadframe Inspection			X
	Manufacturing Package Clean	X	X	N/A
	Manufacturing Die Mounting	X	X	X



QA Die Mount Control (continuous sampling) • Visual Die Inspection	X	X	X
Bond Wire Procurement	X	X	X
Q.C. Wire Inspection (receiving)	X	X	X
Manufacturing Wire Bonding	X Al	X Al	X Au
QA Bond Control (continuous sampling) • Visual Die & Bond Inspection • Wire and Pull Test	X	X	X
Manufacturing Pre-Seal Screen (100%)	MS883 Method 2010 Cond. A or B	MS883 Method 2010 HS Mod. Cond. B	MS883 Method 2010 HS Mod. Cond. B
QA Pre-Seal Inspection Lot Acceptance	MS883 Method 2010 Cond. A or B	MS883 Method 2010 HS Mod. Cond. B	MS883 Method 2010 HS Mod. Cond. B
Preseal Bake Per MS-883, Method 1008, Cond. C	8 hr.	4 hr.	4 hr.
Package Lid Procurement	X	X	N/A
Package Lid Inspection	X	X	N/A
Package Lid Clean	X	X	N/A
Package Seal/Encapsulation	X	X	X
QA Package Seal/Encapsulated Control (continuous sampling)	X	X	X



Stabilization Bake MS-883, Method 1008, Cond. C.	24 hr.	8 hr.	8 hr.
Temperature Cycle, MS-883, Method 1010, Cond. C,	X	N/A	N/A
Centrifuge, MS-883, Method 1010, (Y1) Plane 30 KG's min.	100%	N/A	N/A
Fine Leak, MS-883, Method 1014	100%	Sample	N/A
Gross Leak, MS-883, Method 1014	100%	Sample	N/A
Frame Removal & Loading Units In Carriers/Sticks	X	X	X
Final QA Lot Inspection, MS-883 Method 1014 • Fine & Gross Leak • Visual/Mechanical Inspection	X	X	X
Group A Initial Tests Table 1	X	X	X
Brand Device Type/Date Code Serialize, If Applicable	X	N/A	N/A
Burn-In (100%), MS-883, Method 1015	Classes A/B Products	N/A	N/A
Group A Final Test (100%)	X	N/A	N/A
QA Acceptance Elec. Testing • Visual/Mechanical Method 2009 Lot Sampling	X	X	X
Brand Devices Type/Date Code	N/A	X	X
Controlled Inventory	X	X	X

M C E	Package for Shipment	X	X	X
M C E	Quality Conformance Inspection Group B/C/D Testing, MS-883, Method 5005, Periodically or by Customer P.O. Request	X	X	X
M C E	QA Plant Clearance • Final Visual of Marking and Physical Quantity, Conformation of Product by Inspection or Sample Test	X	X	X
M C E	Ship to Customer	X	X	X

HARRIS Commercial Grade Products

This product is processed on the same wafer fabrication lines, to the same thorough specification and rigid controls as HI-Rel parts. At wafer electrical probe the product may be categorized for electrical performance, such as temperature range of operation or maximum output (see specific product data sheet for grading details) by utilizing multiple colored inks. Defective die are inked with red ink, but, for example, die meeting the commercial temperature range electrical specifications may be inked with green ink.

The die are then visually inspected and sorted after die separation to a modified Class B visual criteria. They are then assembled in packages on a controlled assembly line. The ink used to categorize product performance, such as the green ink, might not be removed from the commercial grade die. This ink has been chemically characterized as inert and reliability verification confirms there is no effect on performance or operating life of the parts.

Harris invites any interested customer to review our assembly flow and facilities for information, quality survey, or certification.

Table I — Group A Electrical Tests[1.]

SUBGROUP[2.]	DASH 8 & 2 LTPD * MIL-PRODUCT	LTPD* COMM. PRODUCT
Subgroup 1 Static Test at 25°C	5	5
Subgroup 2 Static Test at Maximum Rated Operating Temperature	7	–
Subgroup 3 Static Tests at Minimum Rated Operating Temperature	7	–
Subgroup 4 Dynamic Tests at 25°C	5	5
Subgroup 5 Functional Tests at 25°C	5	5
Subgroup 6 Functional Tests at Maximum and Minimum Rated Operating Temperatures	10	15
Subgroup 7 Switching Tests at 25°C	7	10

1. The specific parameters to be included for tests in each subgroup shall be as specified in the applicable procurement document or specification sheet. Where no parameters have been identified in a particular subgroup or test within a subgroup, no Group A testing is required for that subgroup or test to satisfy Group A requirements.
2. A single sample may be used for all subgroup testing. Where the required size exceeds the lot size, 100% inspection shall be allowed.

* Groups A, B, C and D sampling plans are based on standard LTPD tables of MIL-M-38510. Typically, the sample size chosen is based on 1 reject allowed. If necessary, the sample size will be increased once to the quantity not exceeding an acceptance number of 2.

Table II — Group B Tests (Lot Related)[1.]

TEST	MIL-STD-883 METHOD	MIL-STD-883 CONDITION	LTPD*
Subgroup 1 Physical Dimensions	2016		2 Devices (No Failures)
Subgroup 2 Resistance to Solvents	2015		4 Devices (No Failures)
Subgroup 3 Solderability [3]	2003	Soldering Temperature of 260 ± 10°C	15
Subgroup 4 Internal Visual and Mechanical	2014	Failure Criteria from Design and Construction Requirements of Applicable Procurement Document.	1 Device (No Failures)
Subgroup 5 Bond Strength[2] (1) Thermocompression (2) Ultrasonic or Wedge (3) Beam Lead	2011	(1) Test Condition C or D (2) Test Condition C or D (3) Test Condition H	15

NOTES:

1. Electrical reject devices from the same inspection lot may be used for all subgroups when end point measurements are not required.
2. Test samples for bond strength may, at the manufacturer's option unless otherwise specified be randomly selected immediately following internal visual (precap) inspection specified in method 5004, prior to sealing.
3. All devices submitted for solderability test must have been through the temperature/time exposure specified for burn-in. The LTPD for solderability test applies to the number of leads inspected except in no case shall less than 3 devices be used to provide the number of leads required.
4. Generic data from Harris Reliability Add-On Program in the form of Reliability Bulletins are available upon request.

* Reference Note – Table 1*

Table III — Group C (Die Related Tests)

TEST	MIL-STD-883 METHOD	MIL-STD-883 CONDITION	LTPD*
Subgroup 1			
Operating Life Test	1005	Test Condition to be specified (1000 Hrs)	5
End Point Electrical Parameters		Table I — Subgroup 1	
Subgroup 2			
Temperature Cycling	1010	Test Condition C	15
Constant Acceleration	2001	Test Condition E Y_1 Axis	
Seal	1014	As Applicable	
(a) Fine			
(b) Gross 2.			
Visual Examination	1.		
End Point Electrical Parameters		Table I — Subgroup 1	

NOTES:

1. Visual examination shall be in accordance with method 1010.
2. When fluorocarbon gross leak testing is utilized, test condition C_2 shall apply as minimum.
3. Generic data from Harris Reliability Add-On Program in the form of Reliability Bulletins are available upon request.

* Reference Note - Table 1 *

Table IV — Group D (Package Related Tests)

TEST	MIL-STD-883 METHOD	MIL-STD-883 CONDITION	LTPD*
Subgroup 1			
Physical Dimensions	2016		15
Subgroup 2 [4.]			
Lead Integrity	2004	Test Condition B2 (Lead Fatigue)	15
Seal	1014	As Applicable	
(a) Fine			
(b) Gross [6.]			
Subgroup 3 [1.]			
Thermal Shock	1011	Test Condition B as a Minimum, 15 Cycles Minimum.	15
Temperature Cycling	1010	Test Condition C, 100 Cycles Minimum	
Moisture Resistance	1004	Omit Initial/Conditioning and Vibration	
Seal	1014	As Applicable	
(a) Fine			
(b) Gross [6.]			
Visual Examination	2.		
End Point Electrical Parameters		Table I — Subgroup 1	
Subgroup 4 [1.]			
Mechanical Shock	2002	Test Condition B	15
Vibration Variable Frequency	2007	Test Condition A	
Constant Acceleration	2001	Test Condition E	
Seal	1014	As Applicable	
(a) Fine			
(b) Gross [6.]			
Visual Examination	3.		
End Point Electrical Parameters		Table I — Subgroup 1	
Subgroup 5 [4.]			
Salt Atmosphere	1009	Test Condition A	15
Seal			
(a) Fine			
(b) Gross			
Visual Examination			

NOTES:

1. Devices used in subgroup 3, "Thermal and Moisture Resistance" may be used in subgroup 4, "Mechanical".
2. Visual examination shall be in accordance with method 1004.
3. Visual examination shall be performed in accordance with method 2007 for evidence of defects or damage to case, leads, or seals resulting from testing (not fixturing). Such damages shall constitute a failure.
4. Electrical reject devices from that same inspection lot may be used for samples.
5. Visual examination shall be in accordance with paragraph 3.3.1 for method 1009.
6. When fluorocarbon gross leak testing is utilized, test condition C_2 shall apply as minimum.
7. Generic data from Harris Reliability Add-On Program in the form of Reliability Bulletins are available upon request.

* Reference Note - Table 1 *

Moisture Sensor Chip

Harris Semiconductor manufactures a device designed to make in-situ measurements on internal water vapor content of hermetic enclosures. It is particularly suited for determining moisture content in integrated circuits and hybrid packages as required by most military programs. Specifications and operating information for this device is provided on the succeeding pages.

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HIO-55001-6

Moisture Sensor Chip

FEATURES

- ACCURACY IS NOMINALLY ±20% OF THE ACTUAL AMOUNT OF WATER PRESENT
- REPEATABILITY OF READINGS ±2°C
- NO SPECIAL PRE-CONDITIONING REQUIRED
- USEFUL FOR PACKAGE ASSEMBLY PROCESSING TEMPERATURES UP TO 500°C

APPLICATION

The HI-55001 can be used to make an in-situ determination of internal water vapor content of hermetic enclosures, particularly integrated circuit packages. The moisture sensor may be utilized for packaging technology improvement[1] and for assembly lot process control. Applied in a relatively simple correlation experiment, it is eligible for DESC certification as a sensing device for supplying package moisture data per the requirements of MIL-STD-883 method 1018 procedure 3.

DESCRIPTION

The HI-55001 is an integrated circuit moisture sensing element for use in determination of internal water vapor content of hermetic cavities.

The HI-55001 has four independent moisture sensing patterns on chip. Packages of up to one cubic centimeter cavity volume will require use of only one of the quad cells available. For internal cavity volumes in excess of one cubic centimeter, additional cells may be bonded out in parallel to increase the moisture capture area. Paralleling may be achieved by either internal or external package interconnection.

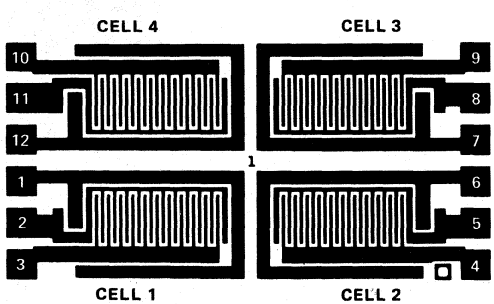
Performance of the HI-55001 has been extensively studied.[2] Correlation experiments with mass spectrometer measurements have been carried out by DESC certified laboratories. The range of useful measurement has been determined to be from < 200ppmV to at least 25000 ppmV. While mass spectrometry is the reference method for cavity moisture content measurement, there is currently no primary reference method or calibration technique for assuring absolute accuracy of any measurement method. Accuracy and range of useful measurement are therefore approximations based on an extensive program of dual moisture determinations. Data from both HI-55001 in-situ measurements and from mass spectrometer determinations per MIL-STD-883 method 1018 procedure 1 were used to establish the correlation noted above.

Note that in general the chip may be stored, handled and processed into the test package in the same manner as any conventional integrated circuit.

- Dry nitrogen storage should be utilized.
- Conventional wire bonding and die attach techniques are acceptable.
- **The sensor top surface is not glassivated. Care must be taken not to contact this surface to avoid contamination and mechanical damage.**

NOTE:
1. Lowry, R.K., VanLeeuwen, C.J., Kennimer, B.L., and Miller, L.A., "A Reliable Dry Ceramic Dual In-Line Package", International Reliability Physics Symposium, San Diego, California, April 19, 1978.
2. Lowry, R.K., Miller, L.A., Jonas, A.W., and Bird, J.M., "Characteristics of a Surface Conductivity Moisture Monitor for Hermetic Integrated Circuit Packages", International Reliability Physics Symposium, San Francisco, California, April 25, 1979.

CHIP LAYOUT



The HI-55001 has four electrically identical moisture sensing cells on chip. The user may apply any one cell or parallel combination of cells in a moisture measuring experiment. The individual cells are accessed as follows: Cell 1 – pads 2 & 3; Cell 2 – pads 4 & 5; Cell 3 – pads 8 & 9; Cell 4 – pads 10 & 11 respectively.

Chip Size: 95 mils by 50 mils.

8

EQUIPMENT REQUIRED

Moisture sensing element installed in the package type to be analyzed.

Fluid bath temperature chamber/insulating container.

Keithley Model 602.*

X-Y Recorder HP-7004B.*

60V DC Power Supply HP-6128A.*

Thermocouple Cromel/Alumel.

Thermometer CMS – 10°C to +260°C; FISHER –#15-030 -50°C to +50°C.*

Immersion Heater.

CO_2 or LN_2 supply.

3M Fluorinert Ⓡ FC-43*.

General Electric RTV sealant/adhesive. (#106 Hi. Temp.).*

* or equivalent

CONSTRUCTION OF TEMPERATURE CHAMBER

The fluid bath temperature chamber is constructed of double sided copper clad glass board to a dimension of W5" x L5" x H6". The detachable top should be bolted to the container via tie down nuts soldered on at least two opposing corners. The use of copper clad board affords ease of sealing the chamber against fluid leakage in addition to providing shielding from external fields.

The cooling coil is constructed by winding ten coil turns using 3/8" OD copper tubing. Two holes are drilled on opposite sides of the fluid container to accept the inlet and outlet of the coil. The coil is secured by soldering the inlet and outlet to the copper clad board. The inlet side of the tubing must be provided with adequate fixturing to enable connection to a CO_2 or LN_2 source. The chamber, when in use should be inside of an insulating container for economy of coolant usage.

SAMPLE PREPARATION

Install moisture sensing element in package to be analyzed.

Wire bond moisture sensor cell pads to package pins and seal package using routine processing methods.

Perform fine and gross leak to determine proper hermeticity.

Special considerations need to be addressed when evaluating metal lidded or capped packages because of their tendency to allow water condensation onto the metal surfaces before that of the moisture sensor. RTV (thermal insulating) sealant/adhesive should be applied to the following package types then subjected to a 10 minute 100°C curing bake:

- Can type packages: coat circumference and top with sealant/adhesive.
- Flat metal lid packages: coat lid surface with sealant/adhesive.
- All hybrid packages: coat entire lid surface with sealant/adhesive.
- Ceramic packages: no preparation is needed.

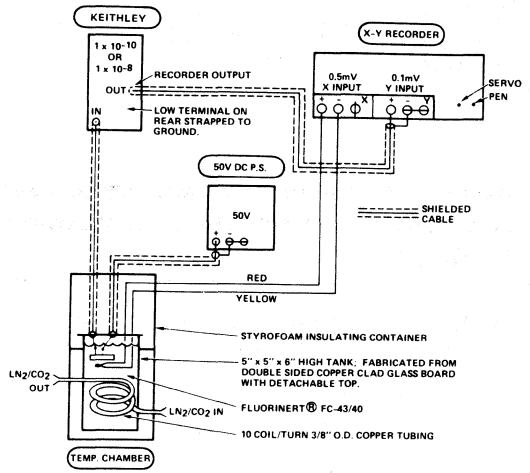
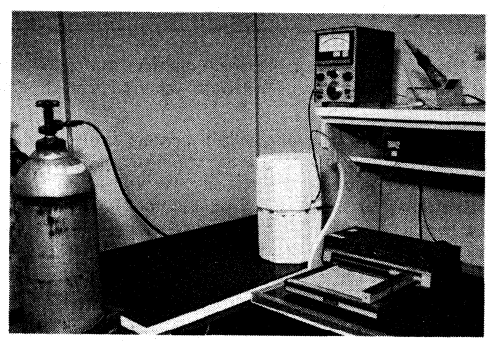
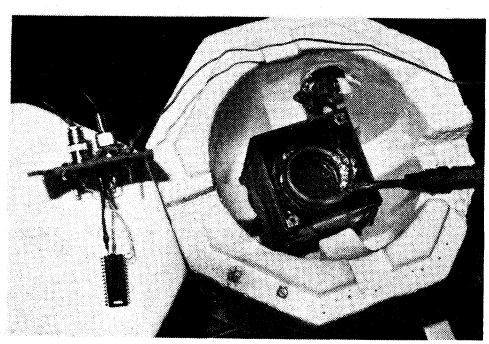


Figure 1 – Measurement Apparatus



Test Setup – This photograph shows the complete test setup for implementation of a moisture measurement.



Temperature Chamber – This photograph illustrates the configuration of the fluid bath temperature chamber. The test device is positioned in the center of the cooling coil below the fluid level when the cover is attached to the base.

CALIBRATION

Calibrate thermocouple using the X-input of recorder and position pen to secure convenient Y-position.

Insert thermocouple into bath along with the thermometer.

Heat bath with immersion heater to +100°C.

Drop pen recorder on the X-axis momentarily and record reading of thermometer.

Turn on CO_2/LN_2 and repeat above at 10°C intervals down to -40°C.

MEASUREMENT

Solder the test device (with the moisture sensing element installed) to the two leads of the underside of the bath chamber lid.

Adjust thermocouple to close proximity to the underside of the test device.

Heat the bath to +100°C with immersion heater while monitoring the fluid temperature with the thermometer.

Remove heater and thermometer and secure lid to container with screws.

Install insulating top. Turn Servo on.

Check the X-axis to verify that the temperature point will correspond to +100°C.

Turn on power supply, set 50V and adjust Keithley scale (1×10^{-8} to 1×10^{-10} to give the least deflection. 10^{-10} or 10^{-9} at start, then as possible dew point is attained 10^{-8} may be required for Y peak).

Drop pen.

Turn on CO_2/LN_2 and chill the bath down to -40°C over a time period of not less than 0.25 hours.

An example measurement is as follows: A Y-axis peak is detected at -27°C. For a package cavity pressure of 0.5 atmosphere, this translates to moisture content of 1000 ppmV on the nomograph.

If no Y-axis peak is noted over the range +100°C to -40°C, it is desirable to corroborate the data by two methods.

- Run one or more additional package samples from the same package/sealing run, expecting correlating test results.
- De-lid the test sample and examine for anomalies such as scratched open metal or an open bond, or bonding to the wrong package/moisture sensor pads.

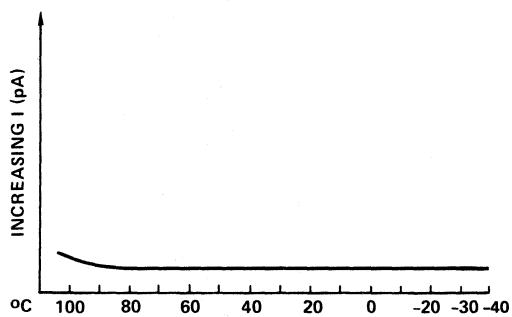


Figure 2 — Shows no moisture peak down to -40°C. This indicates a moisture content of less than 320 ppmV for a cavity pressure of 0.41 atmosphere.

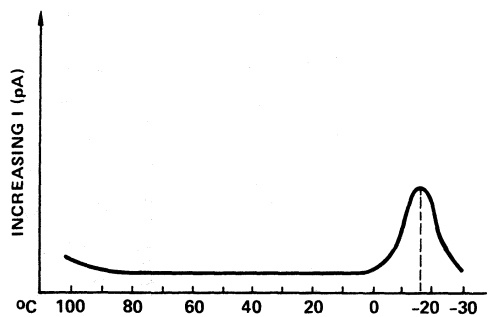


Figure 3 — Shows a moisture peak at approximately -18°C for a package cavity pressure of 0.45 atmosphere. This translates to approximately 2800 ppmV moisture.

8

USE OF THE NOMOGRAPH

From the temperature of the peak current and the pressure of the sealed cavity (reasonably estimated from Gay Lussac's law: $P \propto T$, V constant), the nomograph in Figure 4 will yield package moisture content in parts per million by volume.

As an example, assume the package in Figure 3 (moisture peak at -18°C) was sealed at a temperature of 300°C; the internal cavity pressure can then be calculated using the formula:

$$\frac{P_1}{T_1} = \frac{P_2}{T_2} \text{ or } \frac{1}{300+273^{\circ}C} = \frac{P_2}{(-18)+273^{\circ}C} \text{ or } \frac{1}{573^{\circ}C} = \frac{P_2}{255^{\circ}C}$$

Solving for P_2 ; $P_2 = 0.45$ atmosphere.

$^*P_1$ = Pressure at time of seal (1 atmosphere unless vacuum sealed.

P_2 = Unknown pressure.

T_1 = Temperature (absolute) at time of seal.

T_2 = Temperature of conductivity peak maximum.

With the internal cavity pressure and the temperature of the conductivity maximum known, the nomograph in Figure 4 will yield the internal moisture ppm by V.

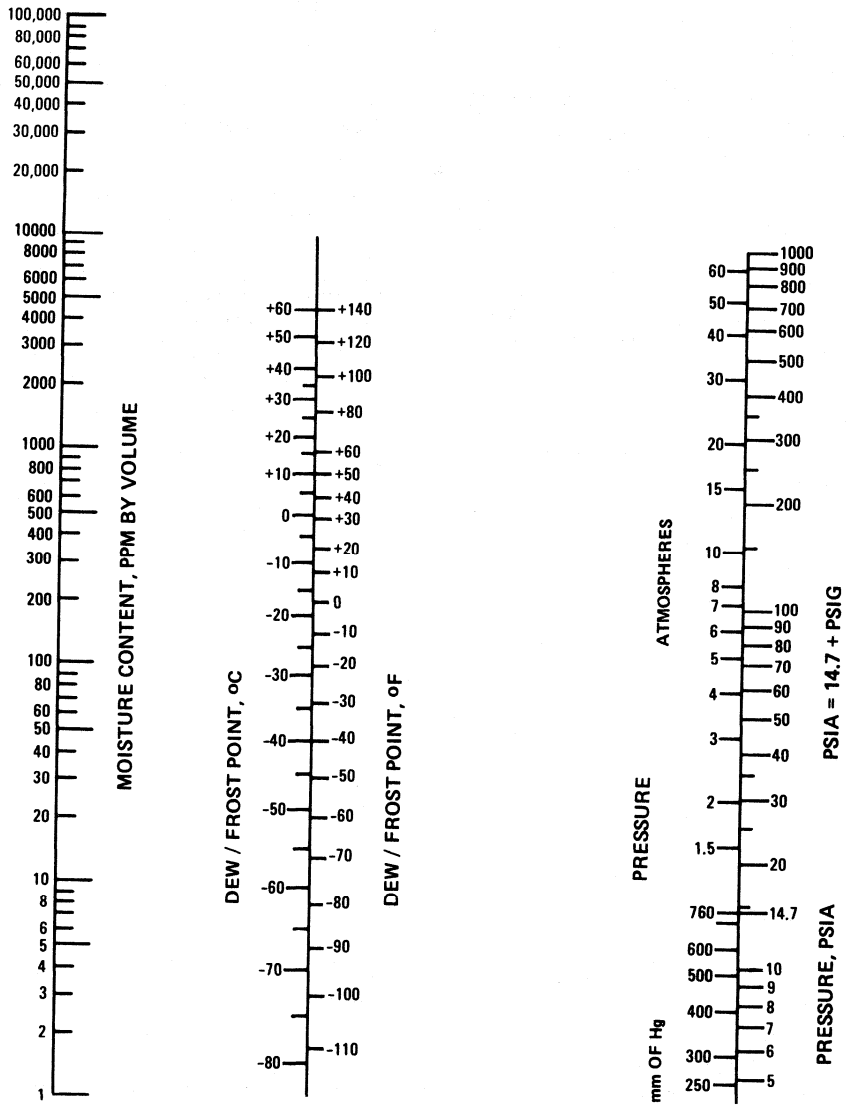


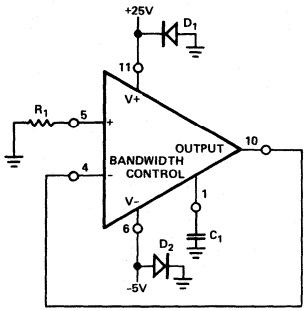
Figure 4 – Nomograph for Dewpoints & ppm as a Function of P

Burn-In Circuit Index

		DRAWING NO.
HA-909/911	Low Noise, Operational Amplifier	1, 2
HA-1600/02/05	Precision Voltage Reference	3
HA-1610/1615	10V Precision Voltage Reference	4
HA-2400/04/05	PRAM, Four Channel Operational Amplifier	5
HA-2420/25	Sample & Hold	6
HA-2500/02/05	Precision High Slew Rate Operational Amplifier	2
HA-2507/17/27	Epoxy Packaged, High Slew Rate Op Amp	7
HA-2510/12/15	High Slew Rate Operational Amplifier	2
HA-2520/22/25	High Slew Rate Uncompensated Op Amp	2
HA-2530/35	Wide Band High Slew Inverting Amplifier	8
HA-2600/02/05	High Performance Operational Amplifier	2
HA-2607/27	Epoxy Packaged, High Slew Rate Op Amp	7
HA-2620/22/25	Very Wide Band, Uncompensated Op Amp	2, 9
HA-2630/35	High Performance Current Booster	10
HA-2640/45	High Voltage Operational Amplifier	2
HA-2650/55	Dual High Performance Op Amp	11, 12
HA-2700/04/05	Low Power, High Performance Op Amp	13, 14
HA-2720/25	Low Power, Current Programmable Op Amp	15
HA-2730/35	Dual Low Power, Current Programmable Op Amp	16
HA-2900/04/05	Chopper Stabilized Operational Amplifier	17
HA-4602/05	Quad High Performance Op Amp	18
HA-4622/25	Wide Band High Performance Quad Op Amp	19
HA-4741	Quad Operational Amplifier	18
HA-4900/05	Quad Precision Comparator	20
HA-4920/25	High Speed Quad Comparator	20
HA-4950	Precision High Speed Comparator	21
HA-5100/05	Wide Band, JFET Input, Operational Amplifier	22
HA-5110/15	Wide Band, JFET Input, Uncompensated Op Amp	22
HA-5190/95	Wide Band Fast Settling Op Amp	23, 24
HC-55516/32	Delta Modulator (CVSD)	25
HI-200	Dual SPST Switch	26, 27
HI-201	Quad SPST Switch	28
HI-506	16/Dual 8 Channel Multiplexer	29
HI-506A	Overvoltage Protected 16/Dual 8 Channel Mux	29
HI-507	16/Dual 8 Channel Multiplexer	29
HI-507A	Overvoltage Protected 16/Dual 8 Channel Mux	29
HI-508A	Overvoltage Protected 8/Dual 4 Channel Mux	30
HI-509A	Overvoltage Protected 8/Dual 4 Channel Mux	31
HI-516	16 Channel/Dual 8 Channel CMOS High Speed Mux	32
HI-518	8 Channel/Dual 4 Channel CMOS High Speed Mux	33
HI-562	12 Bit, High Speed, Precision D/A Converter	34
HI-1080/85	8 Bit Precision D/A Converter	35
HI-1800A	Dual DPST Low Leakage Switch	36
HI-1818A	8/Dual 4 Channel Multiplexer	37
HI-1828A	8/Dual 4 Channel Multiplexer	38
HI-1840	Fail-Safe 16 Channel Multiplexer	29
HI-5040	Low Resistance SPST Switch	39
HI-5041	Low Resistance Dual SPST Switch	39
HI-5042	Low Resistance SPDT Switch	39
HI-5043	Low Resistance Dual SPDT Switch	39
HI-5044	Low Resistance SPDT Switch	39
HI-5045	Low Resistance SPDT Switch	39

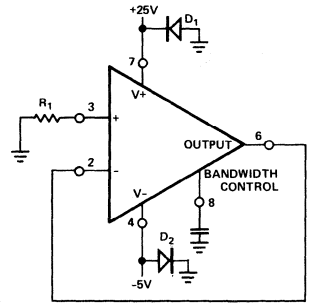
Burn-In Circuits

1 HA-909/911 TO-86 FLAT PACK



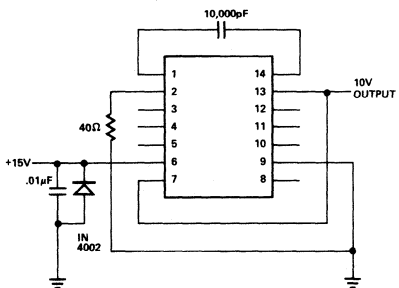
NOTES:
T_A = +125°C
R_1 = 1Megohm
C_1 = 0.01μF, 100V

2 HA-909/911, HA-2500/02/05, HA-2510/12/15, HA-2520/22/25, HA-2600/02/05, HA-2620/22/25 HA-2640/45 TO-99

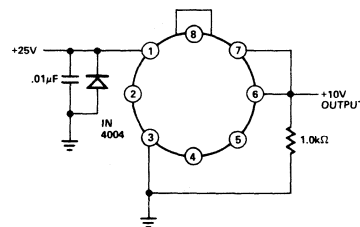


NOTES:
T_A = +125°C
R_1 = 1Megohm
C_1 = 0.01μF, 100V
*V_{SUPPLY} = ±40V

3 HA-1600/02/05 14 LEAD DIP

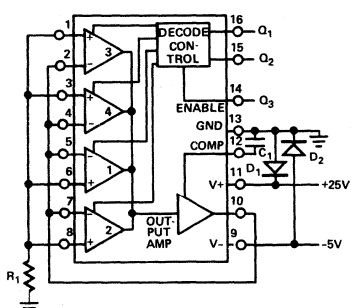


4 HA-1610/15 TO-99



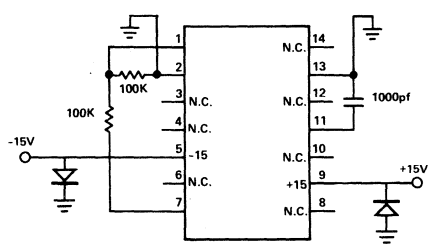
NOTE:
Each device draws ~12mA ~ Junction Temp. 156°C

5 HA-2400/04/05 16 LEAD CERDIP



NOTES:
T_A = +125°C
R_1 = 100kΩ
C_1 = 910pF, 50V
D_1, D_2 = IN4002
FREQ., Q_1 = 100kHz; Q_2 = 50kHz; Q_3 = 25kHz

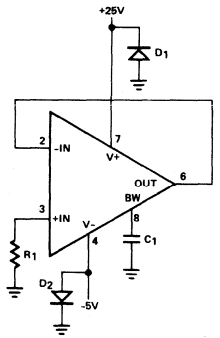
6 HA-2420/25 14 LEAD CERDIP



NOTE:
T_A = +125°C

8

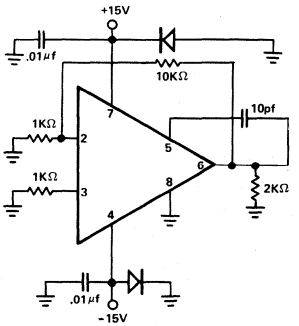
7 HA-2507/17/27, HA-2607/27 — 8 PIN DIP



NOTES:

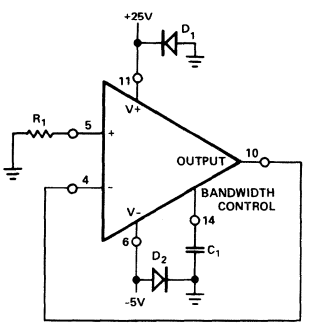
D_1, D_2 = IN4002 or similar	One Pair per Board
R_1 = 1MΩ 5% ¼ or ½ Watt	One per Socket
C_1 = 0.01μF. BV ≥ 30V	One per Socket

8 HA-2530/35 — TO-99



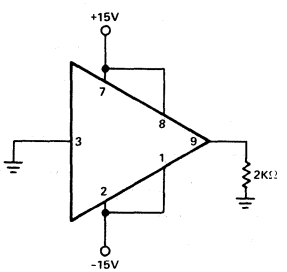
NOTE:
T_A = +125°C

9 HA-2620/22/25 — TO-116



NOTES:
T_A = +125°C
R_1 = 1Megohm
C_1 = 0.01μF, 100V

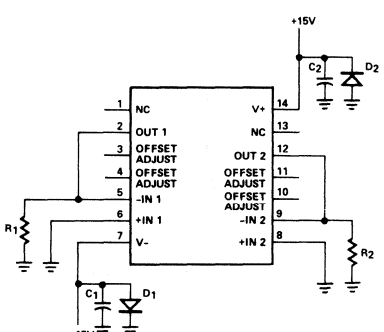
10 HA-2630/35 — TO-8



NOTE:
T_A = +125°C

8

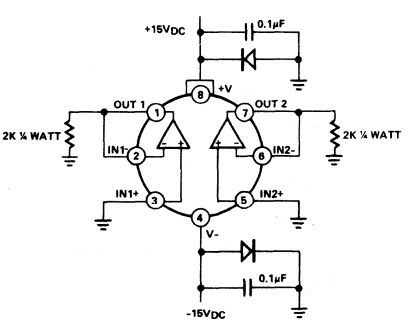
11 HA-2650/55, — TO-116



NOTES:

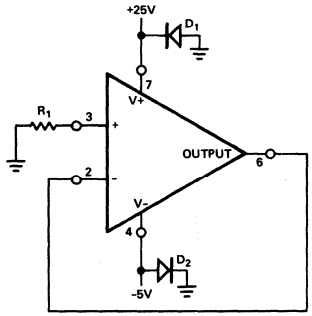
R_1, R_2 = 2kΩ ¼ or ½ Watt 5%	
C_1, C_2 = 0.1μF, V_{BR} ≥ 30V	One Set per Socket
D_1, D_2 = IN4002 or similar	One Set per Board

12 HA-2650/55 — TO-99



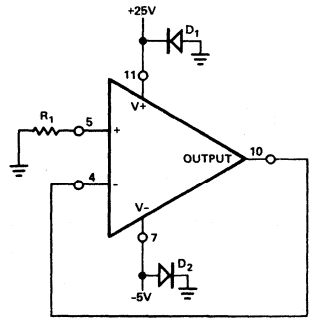
NOTES:
T_A = +125°C, Supplies = ± 15VDC
Resistors = 2kΩ ± 10% ¼ Watt
Capacitors = 0.01 to 0.1μF Nonelectrolytic

13 HA-2700/04/05 TO-99



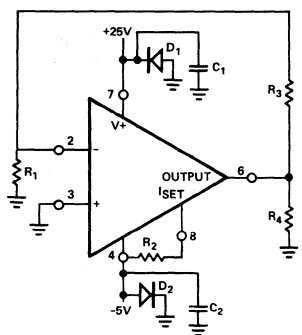
NOTES:
T_A = +125°C
R_1 = 1Megohm

14 HA-2700/04/05 TO-116



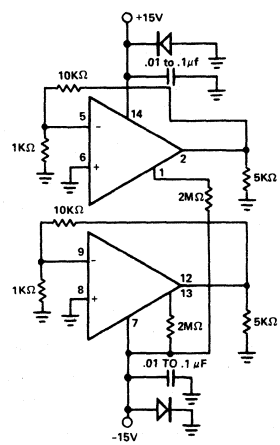
NOTES:
T_A = +125°C
R_1 = 1Megohm

15 HA-2720/25 TO-99



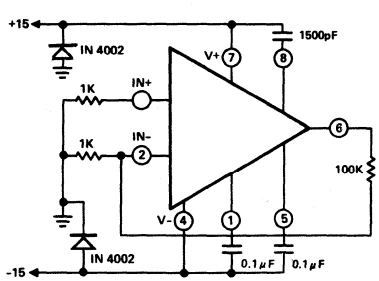
NOTES:
T_A = +125°C
C_1, C_2 = 0.01 to 0.1μF
R_1 = 1kΩ R_3 = 10kΩ
R_2 = 2MΩ R_4 = 5kΩ

16 HA-2730/35 TO-116



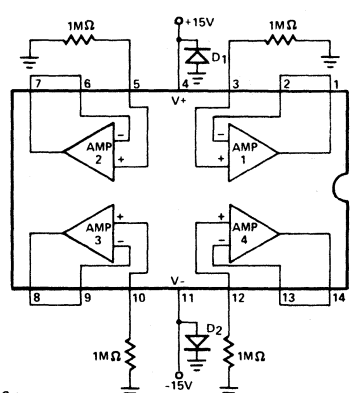
NOTE:
T_A = +125°C

17 HA-2900/04/05 TO-99



NOTES:
T_A = +125°C

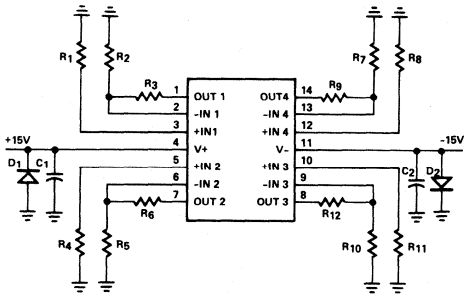
18 HA-4602/05, HA-4741 14 LEAD CERDIP



NOTES:
T_A = +125°C
D_1, D_2 = IN4002

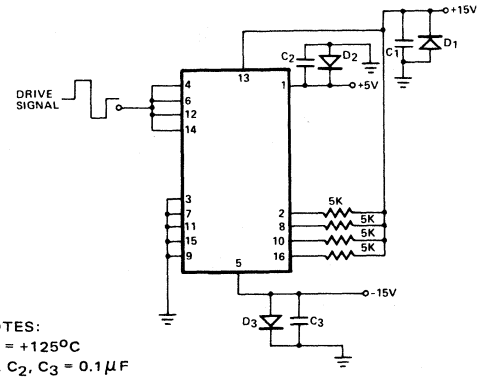
8

19 HA-4622/25 — 14 PIN DIP



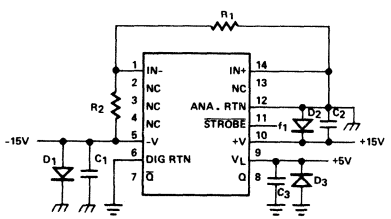
NOTES:
$R_1, R_2, R_4, R_5, R_7, R_8, R_{10}, R_{11} = 1k\Omega$ 5% ¼ or ½ Watt
$R_3, R_6, R_9, R_{12} = 10k\Omega$ 5% ¼ or ½ Watt
$C_1, C_2 = 0.1\mu F$, $V_{BR} \geq 30V$ } One per Socket
D_1, D_2 = IN4002 or similar } One per Board

20 HA-4900/05, HA-4920/25 — 16 PIN CERDIP



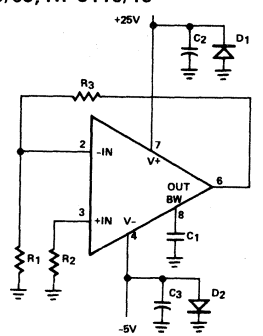
NOTES:
$T_A = +125^oC$
$C_1, C_2, C_3 = 0.1\mu F$
D_1, D_2, D_3 = IN4002
DRIVE SIGNAL FREQ. = 2000Hz
DRIVE SIGNAL AMP = $\pm 0.6V$

21 HA-4950 — 14 PIN DIP



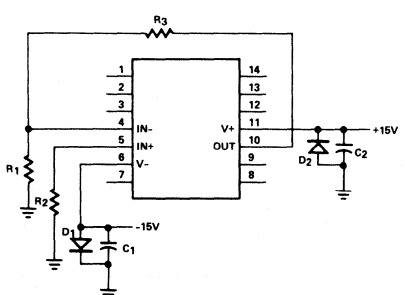
NOTES:
$R_1 = 1k\Omega$
$R_2 = 50k\Omega$ } 5% ¼ or ½ Watt
D_1 = IN4002 or similar
D_2 = IN4002 or similar } One Set per Board
D_3 = IN4002 or similar
$C_1, C_2, C_3 = 0.1\mu F$ } One Set per Socket Breakdown Voltage $\geq 30V$
f_1 = 100kHz TTL Levels (50% Duty Cycle)

22 HI-5100/05, HI-5110/15 — TO-99



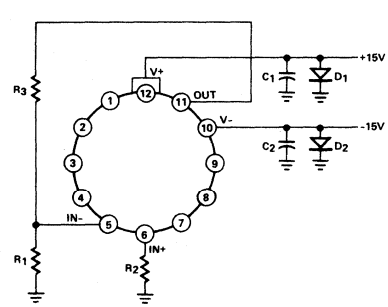
NOTES:
$R_1, R_2 = 10k\Omega$ ¼ or ½ Watt 5%
$R_3 = 100k\Omega$ ¼ or ½ Watt 5%
$C_1 = 0.01\mu F$, $V_{BR} \geq 30V$ } One Set per Socket
$C_2, C_3 = 0.1\mu F$, $V_{BR} \geq 30V$
D_1, D_2 = IN4002 or similar } One Set per Board

23 HA-5190/95 — 14 PIN DIP



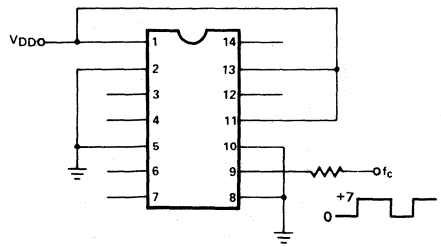
NOTES:
$R_1, R_2 = 1k\Omega$ ¼ or ½ Watt 5%
$R_3 = 10k\Omega$ ¼ or ½ Watt 5%
$C_1, C_2 = 0.1\mu F$, $V_{BR} \geq 30V$
D_1, D_2 = IN4002 or similar

24 HA-5190/95 — TO-8



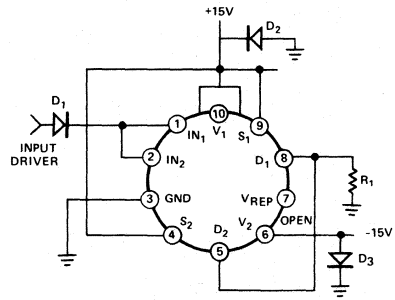
NOTES:
$R_1, R_2 = 1k\Omega$ ¼ or ½ Watt 5%
$R_3 = 10k\Omega$ ¼ or ½ Watt 5%
$C_1, C_2 = 0.1\mu F$, $V_{BR} \geq 30V$ } One per Socket
D_1, D_2 = IN4002 or similar } One per Board

25 HC-55516/32 — 14 LEAD DIP



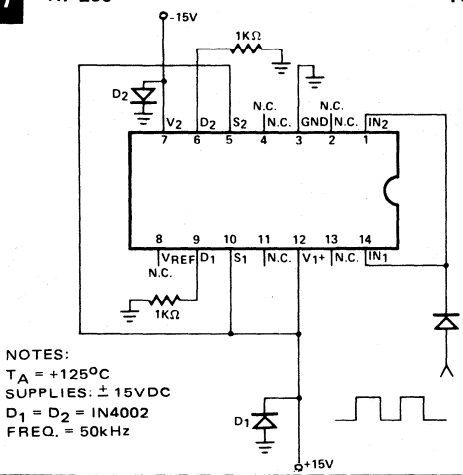
NOTES:
T_A = +125°C
V_{DD} = +7.0V
f_c = 16kHz

26 HI-200 — TO-100



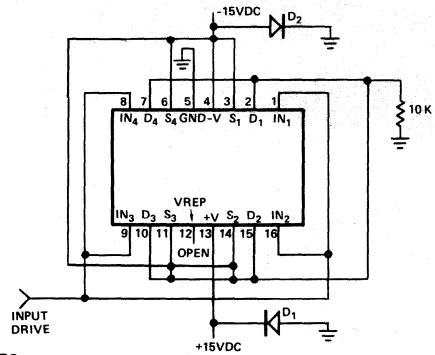
NOTES:
T_A = +125°C
R_1 = 10kΩ
D_1, D_2, D_3 = IN4002
FREQ. = 100kHz

27 HI-200 — TO-116



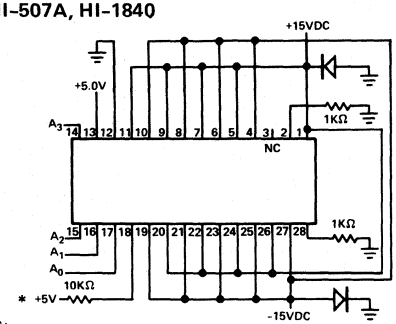
NOTES:
T_A = +125°C
SUPPLIES: ± 15VDC
D_1 = D_2 = IN4002
FREQ. = 50kHz

28 HI-201 — 16 LEAD CERDIP



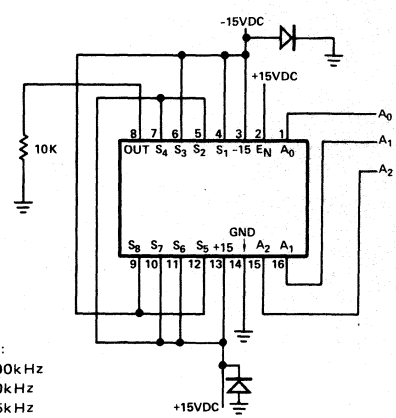
NOTES:
T_A = +125°C
D_1, D_2 = IN4002
FREQ. = 100kHz

29 HI-506, HI-506A, HI-507, HI-507A, HI-1840 — 28 LEAD CERDIP



NOTES:
A_0 = 100kHz
A_1 = 50kHz
A_2 = 25kHz
A_3 = 12.5kHz
* Pin 18 grounded for HI-1840

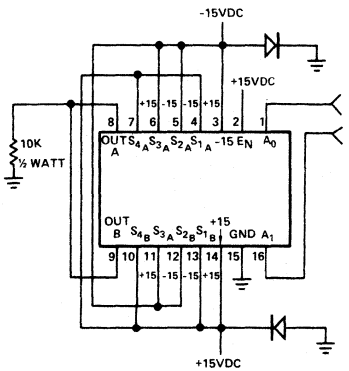
30 HI-508A — 16 LEAD CERDIP



NOTES:
A_0 = 100kHz
A_1 = 50kHz
A_2 = 25kHz
TEMP: +125°C

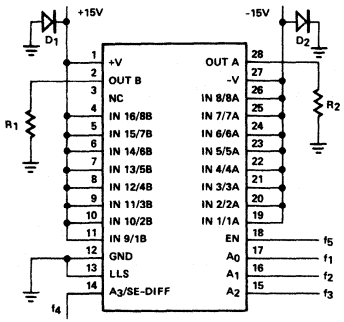
8

31 HI-509A — 16 LEAD CERDIP



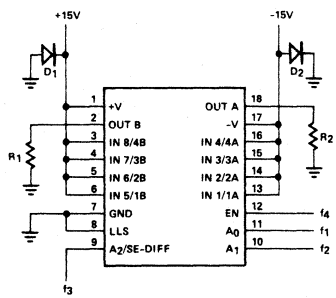
NOTES:
A_0 = 100kHz
A_1 = 50kHz
TEMP: +125°C

32 HI-516 — 28 PIN CERDIP



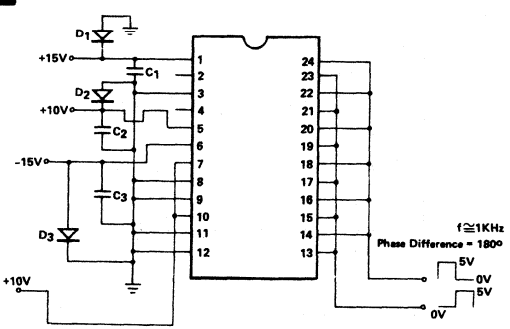
NOTES:
R_1, R_2 = 10kΩ 5% ¼ or ½ Watt
D_1, D_2 = IN4002 or similar } One Set per Board
TTL Levels
(50% Duty Cycle)
f_1 = 100kHz f_2 = 50kHz f_3 = 25kHz
f_4 = 12.5kHz f_5 = 6.25kHz

33 HI-518 — 18 PIN DIP



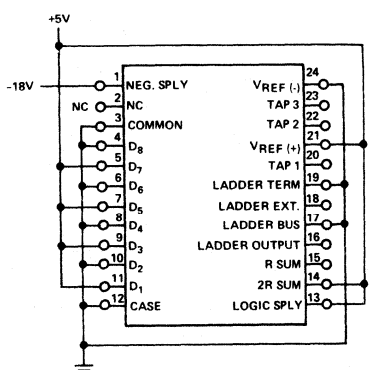
NOTES:
R_1, R_2 = 10kΩ 5% ¼ or ½ Watt
D_1, D_2 = IN4002 or similar } One set per Board
f_1 = 100kHz
f_2 = 50kHz } TTL Levels
f_3 = 25kHz } (50% Duty Cycle)
f_4 = 12.5kHz

34 HI-562 — 24 PIN DIP



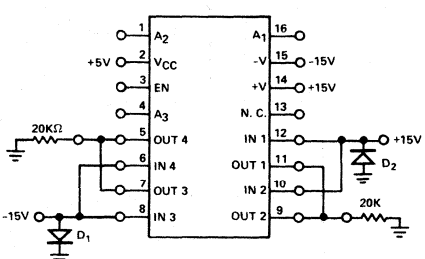
NOTES:
T_A = +125°C
D_1, D_2, D_3 = IN4002
C_1, C_2, C_3 = 0.01 μF

35 HI-1080/85 — 24 LEAD CERDIP



NOTE:
T_A = +125°C

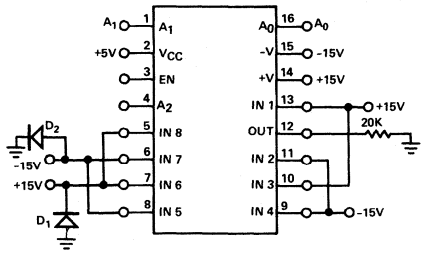
36 HI-1800A — 16 LEAD CERDIP



NOTES:
T_A = +125°C
A_1 = 100kHz
A_2 = 50kHz
A_3 = 25kHz
EN = 12.5kHz

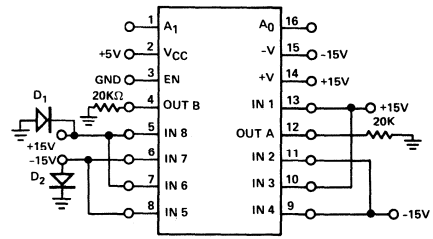
8

37 HI-1818A — 16 LEAD CERDIP



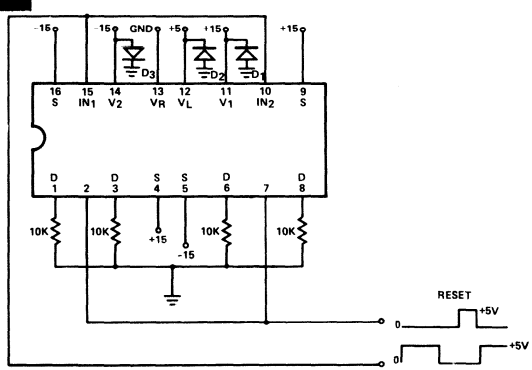
NOTES:
T_A = +125°C
A_0 = 100kHz
A_1 = 50kHz
A_2 = 25kHz
EN = 12.5kHz

38 HI-1828A — 16 LEAD CERDIP



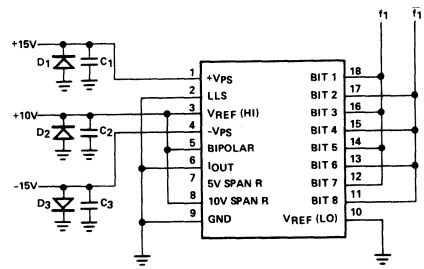
NOTES:
T_A = +125°C
A_0 = 100kHz
A_1 = 50kHz
EN = 25kHz

39 HI-5040 thru HI-5051 — 16 LEAD CERDIP



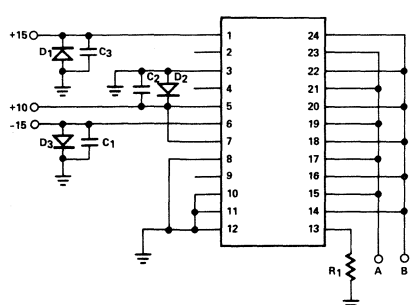
NOTES:
T_A = +125°C
D_1, D_2, D_3 = IN4004
F = 100kHz

40 HI-5618A/5618B — 18 PIN DIP



NOTES:
D_1, D_2, D_3 = IN4002 or similar } One Set per Board
C_1, C_2, C_3 = 0.1 μF } One Set per Socket
Breakdown Voltage $\geq$30V
f_1 = 1MHz TTL Level (50% Duty Cycle)

41 HI-5610 — 24 LEAD DIP



NOTES:
R_1 = 50kΩ
D_2, D_3, D_{11} = IN4002
C_2, C_3, C_{11} = 0.01μF

8

Packaging

Harris Package Selection Guide

PART NUMBER	PACKAGE CODE (SEE NOTE)			
		DIP		LEADLESS
	CAN	CERAMIC	PLASTIC	CHIP CARRIERS*
HA-909/911	2A			
HA-1600/02/05		4T		
HA-1610	2A	4Q		LA
HA-1615	2A	4Q		
HA-2400/2404/2405		5X		
HA-2420/2425		4U		LA
HA-2500/2502/2505	2A	1N		LA
HA-2507/2517/2527			3A	
HA-2510/2512/2515	2A	1N		LA
HA-2520/2522/2525	2A	1N		LA
HA-2530/2535	2A			
HA-2600/2602/2605	2A	1N		LA
HA-2607/2627			3A	
HA-2620/2622/2625	2A	IN,4U		LA
HA-2630/2635	6G			
HA-2640/2645	2A	1N		
HA-2650/2655	2A	4U	3A	LA
HA-2700/2704/2705	2A	4U		
HA-2720/2725	2A	1N		
HA-2730/2735		4D		
HA-2900/2904/2905	2E			
HA-4602/4605		4U		LA
HA-4622/4625		4U		
HA-4741		4U	3M	LA
HA-4900/4905		4Z		
HA-4920/4925		4Z		
HA-4950		4D		LA
HA-5100/5105	2A			
HA-5110/5115	2A			
HA-5190/5195	6G	4D		
HC-55516/55532		4Q		
HD-0165		4K		
HI-200	2D	4U	3M	LA
HI-201		4B	3C	LA
HI-506/507/506A/507A		1M	3P	LC
HI-508A, 509A		4B	3L	LA
HI-516		1M		
HI-518		4N		
HI-562		1H		LC
HI-1080/1085		4K		
HI-1800A		4B		LA
HI-1818A/1828A		4B	3C	LA
HI-1840		1M		
HI-5040 thru HI-5051		4B		
HI-5618A/5618B		5E	3D	LA
HI-5610		1H		
HI-5900		MB		

NOTE: "Package Code" references drawings on the following pages. Note that these do not correspond with the general package designations to be used in constructing the part number, which is explained in Ordering Information at the front of this book.

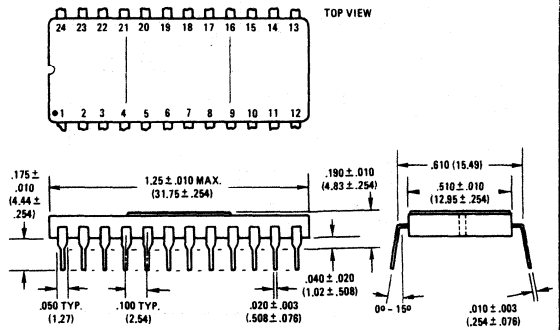
Code "3" plastic DIP packages are not available for military temperature range.

*Leadless Chip Carrier packages are available on the products indicated in the chart. Consult factory for information on ordering and availability.

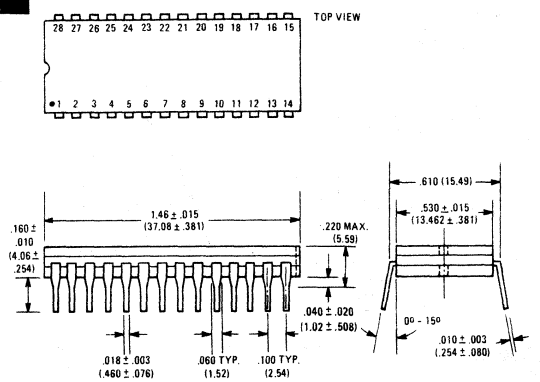
Package Dimensions

1. All dimensions in inches; millimeters are shown in parentheses.
2. All dimensions ±.010 (±0.25mm) unless otherwise shown.
3. Package codes are shown in black squares.

1H 24 LEAD DIP



1M 28 LEAD CERDIP



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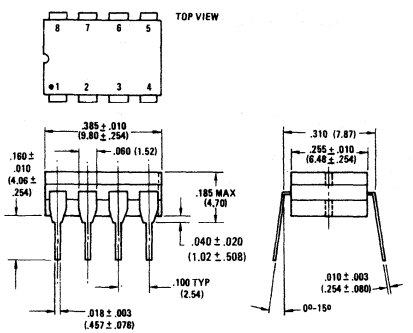
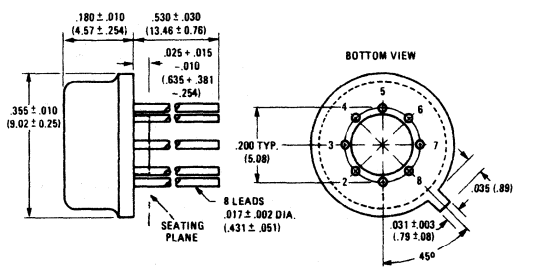


2A TO-99 (8 LEAD)



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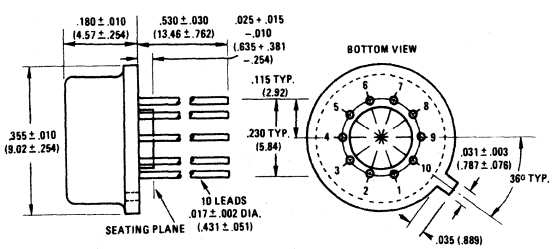

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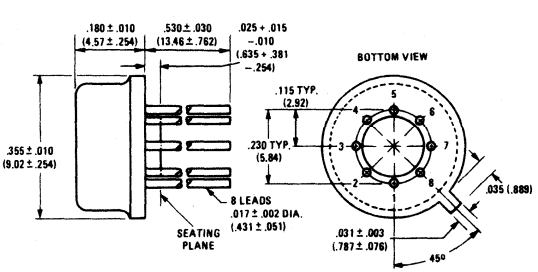

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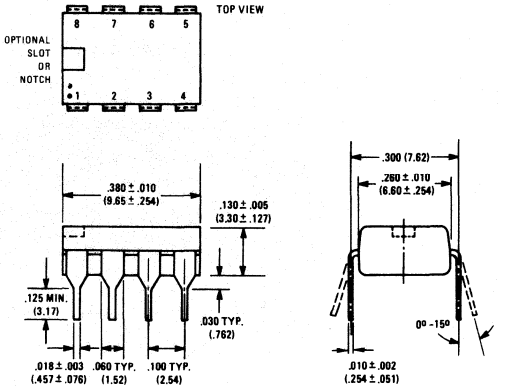
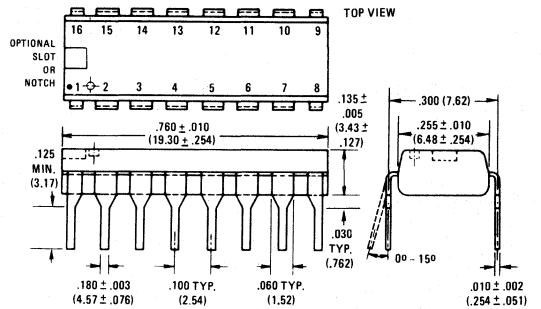
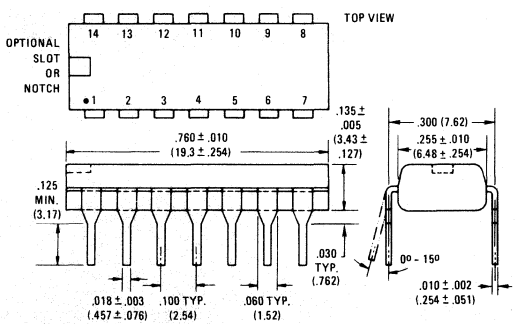
3A — 8 LEAD DIP EPOXY



3C 3L — 16 LEAD DIP EPOXY



3M 3R — 14 LEAD DIP EPOXY



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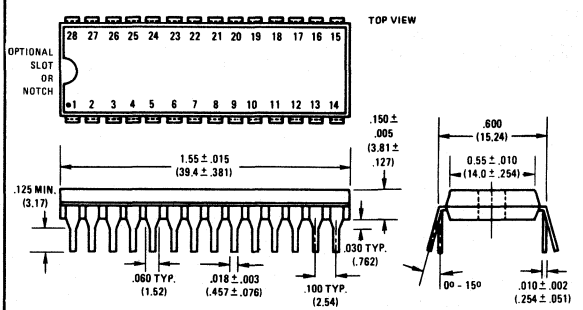
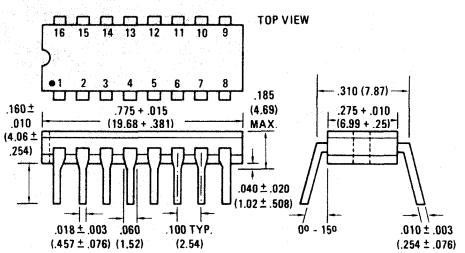


4B 4Z — 16 LEAD CERDIP



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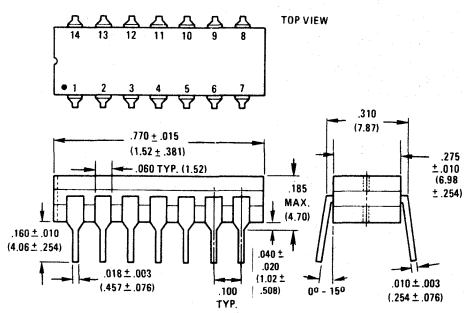

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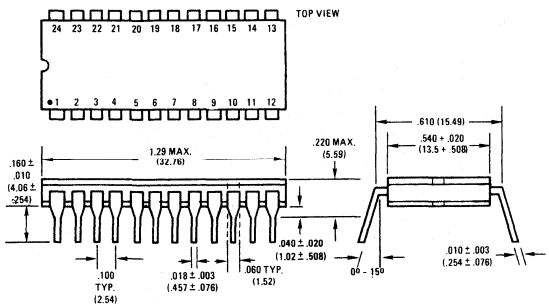
4K 24 LEAD CERDIP



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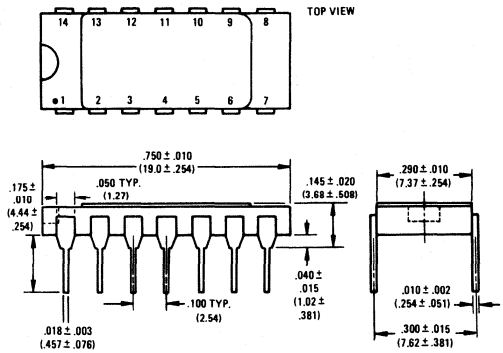

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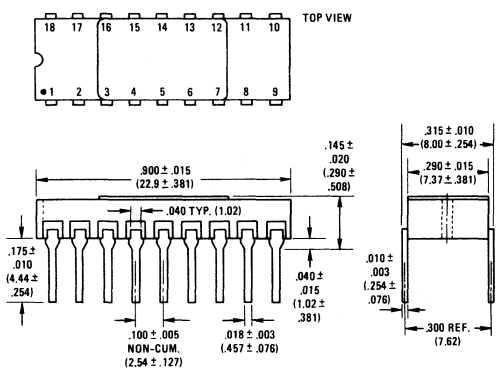
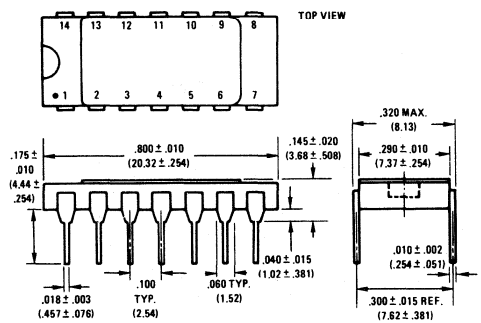


4T 14 LEAD BRAZED DIP



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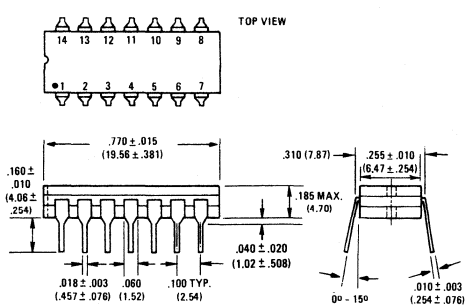

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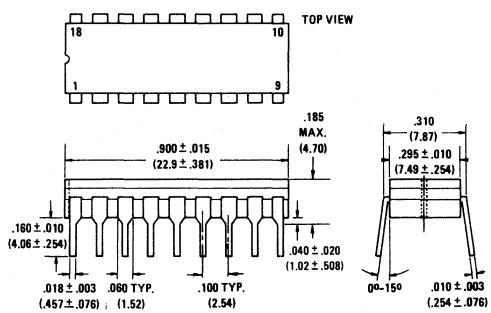

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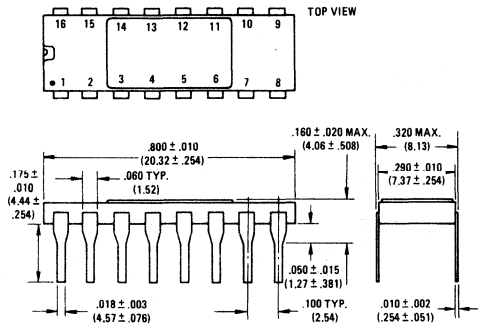
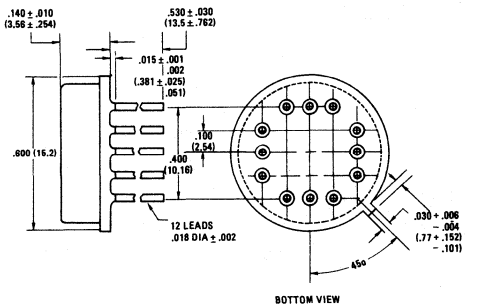
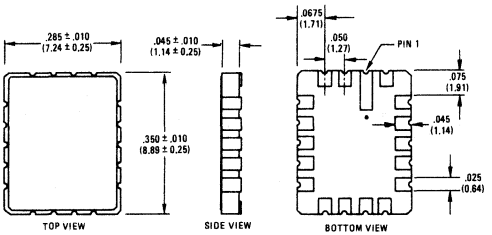
5X 16 LEAD SIDE BRAZE DIP



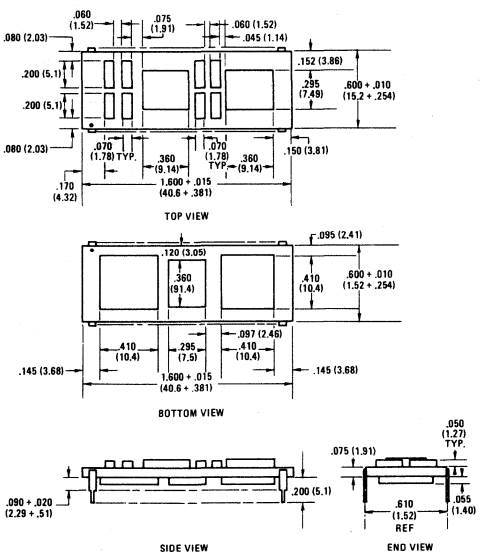
6G TO-8 LOW PROFILE CAP



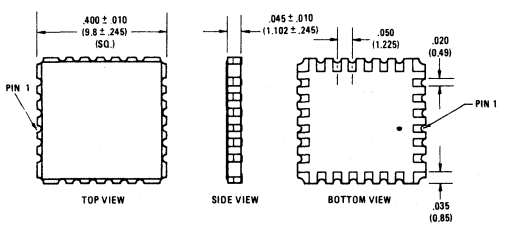
LA 18 LEAD CHIP CARRIER



MB 32 LEAD MODULE



LC 28 LEAD CHIP CARRIER



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